Topical Workshop on Electronics for Particle Physics - TWEPP 2019

Santiago de Compostela September 2-6, 2019

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CPPM - Aix-Marseille Univ, France

Introduction

- The TWEPP workshop is covering the aspects of :
  - electronics for particle physics experiments, and accelerator instrumentation of general interest to users
- The purpose of the workshop is :
  - to present results and original concepts for electronic research and development relevant to LHC experiments
  - to review the status of electronics for the LHC experiments
  - to identify and encourage common efforts for the development of electronics
  - to promote information exchange and collaboration in the relevant engineering and physics communities
- Covered topics :
  - ASIC
  - Optoelectronics and Links
  - Packaging and Interconnects
  - Power, Grounding and Shielding
  - Production, Testing and Reliability
  - Programmable Logic, Design Tools and Methods
  - Systems, Planning, Installation, Commissioning and Running Experience
  - Radiation Tolerant Components and Systems

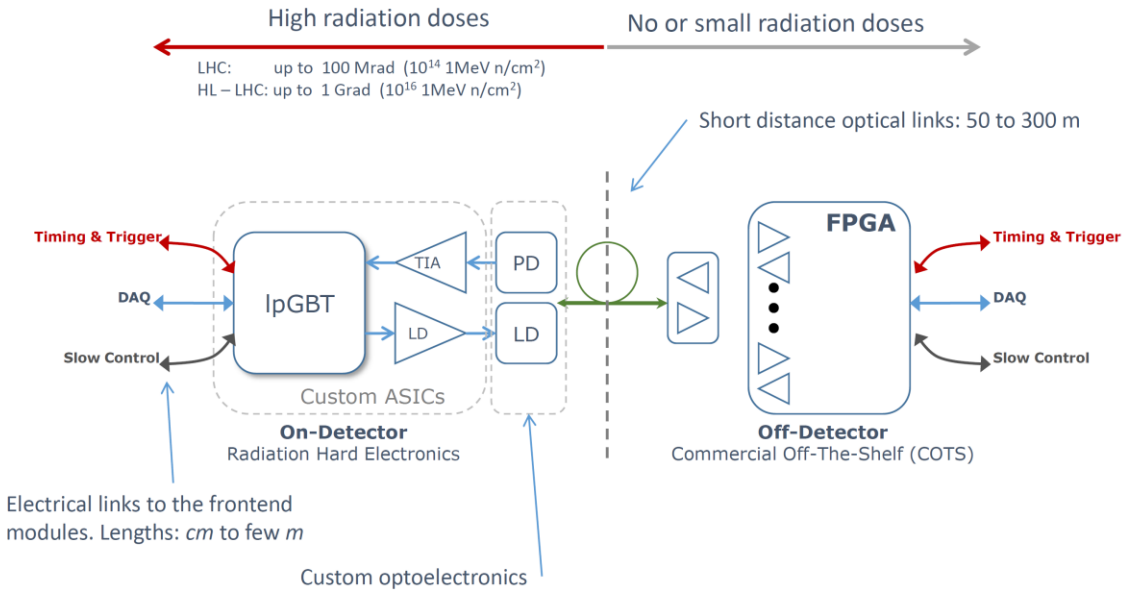
ASIC contributions

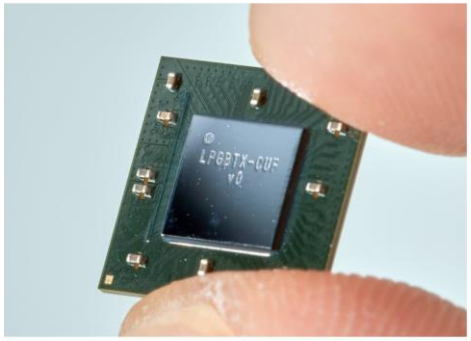
- 21 oral presentations
  - Data transfer lpGBT (7)
  - Readout Chips ROC (10)
    - Monolithic pixels ROC (4)
    - Readout chips for Timing Layers (3)
    - Other Readout chips - Fast data readout (3)
  - IP blocks: PLL/CDR, Monitoring ADC (3)
- 24 posters
  - Data Transfer (1)
  - Readout Chips ROC (10)
    - Monolithic pixels ROC (3)
    - Readout chips for Timing Layers (3)
    - Readout chips for MicroMegas detector
    - Fast readout data
  - ASICs for cryogenic environment
  - ASICs for Detector Control System (DCS) and monitoring

lpGBT project

1. Project description
2. CPPM contribution

lpGBT project





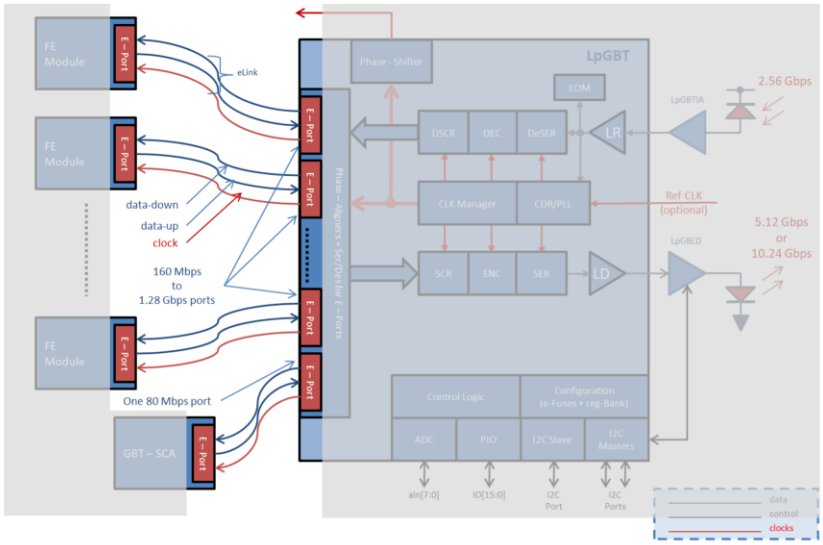
Pin count: 289 (17 x 17)
Pitch: 0.5 mm
Size: 9 mm x 9 mm x 1.25 mm

- More than a “Communications ASIC”
- Rates : **5.12 or 10.24 Gbps** (for uplinks) and **2.56 Gbps** (for downlinks)
- Enables the implementation of Radiation Tolerant Links : DAQ, Trigger, Slow control
  - Designed for radiation hardness
    - Total Ionizing Dose (TID): 200 Mrad
    - Extensive SEU protection (TMR)
- Implements Control and Monitoring Functions :
  - I2C Masters, 16 –bit General Purpose I/O port, Output reset pin, 10 –bit ADC (8 multiplexed inputs), 8 –bit voltage DAC, 8 –bit current DAC, Temperature sensor

The lpGBT: a radiation tolerant ASIC for Data, Timing, Trigger and Control Applications in HL-LHC, P.Moreira et al.

lpGBT communication

- The counting room
  - Optical fibre links
- The FE modules / ASICs
  - Electrical links (eLinks)
- The Number and Bandwidth of eLinks is programmable
- For Down eLinks
  - Bandwidth: 80/160/320 Mbps
  - Count: 16/8/4
- For Up eLinks



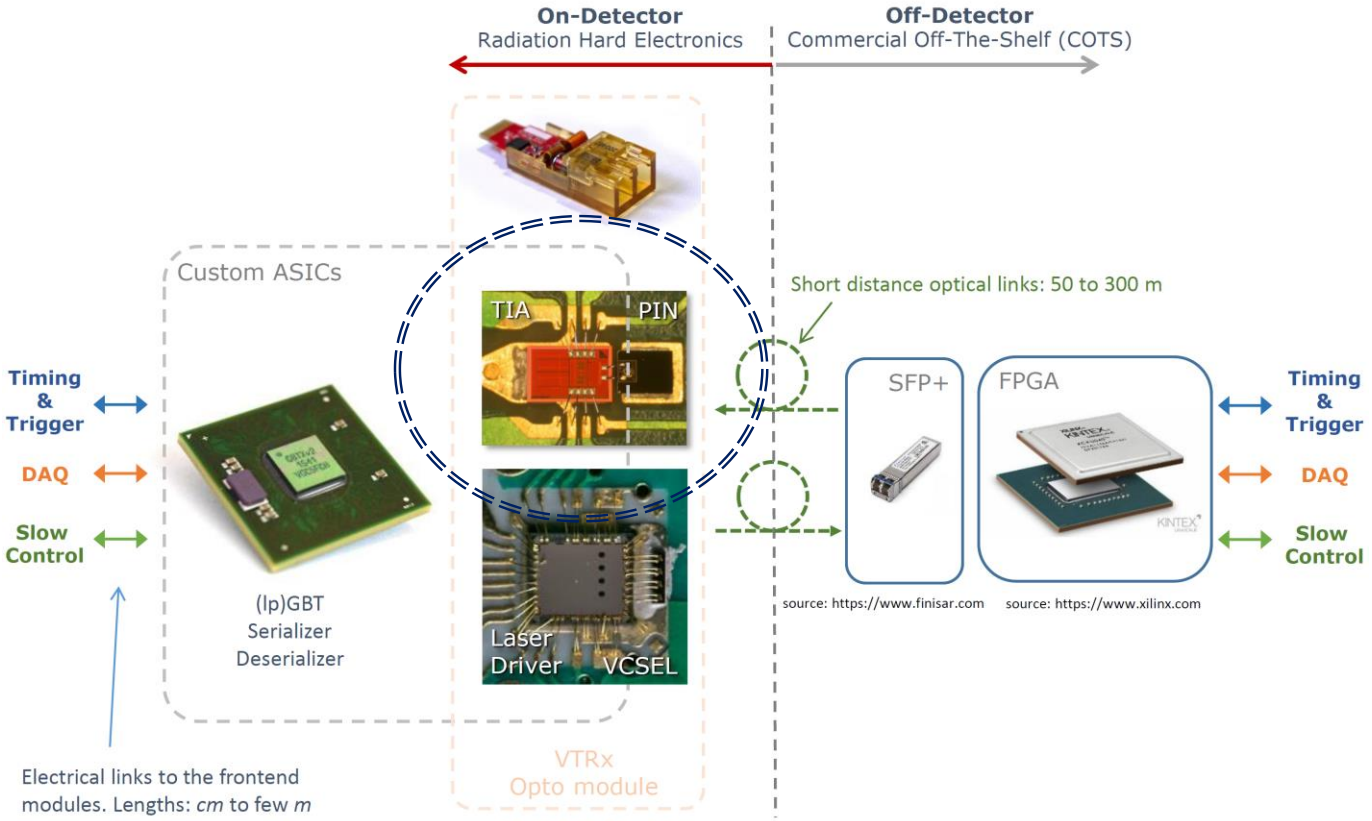
Input eLinks (uplink)												
uplink bandwidth [Gbps]	5.12						10.24					
FEC coding	FEC5			FEC12			FEC5			FEC12		
Bandwidth [Mbps]	160	320	640	160	320	640	320	640	1280	320	640	1280
Maximum number	28	14	7	24	12	6	28	14	7	24	12	6

Example of the RD53 FE chip
Control command : 320 Mbps
Output Data : 4 × 1.28 Gbps/s

5

The lpGBT: a radiation tolerant ASIC for Data, Timing, Trigger and Control Applications in HL-LHC, P.Moreira et al.

CPPM participation

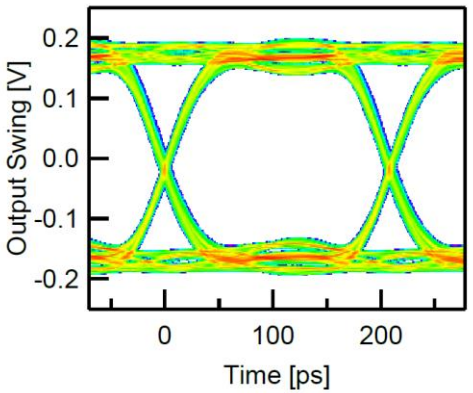


- GBTIA : 5 Gbps fully differential transimpedance amplifier
  - Designed for **photodiode capacitance values lower than 500 fF**
  - Sensitivity of −19 dBm with a BER of 10^{-12}
  - Radiation tolerant up to 200 Mrad
  - Wafer tests for production

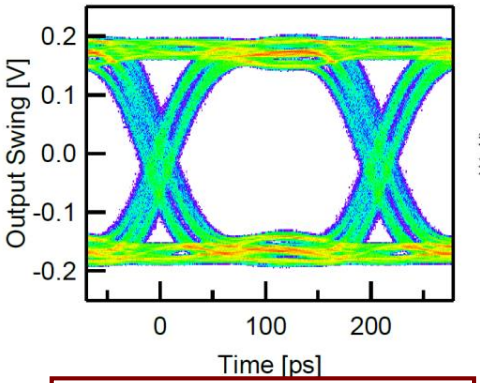
A 5-Gb/s Radiation-Tolerant CMOS Optical Receiver, Menouni, M. ; Tianzuo Xi ; Ping Gui ; Moreira, P IEEE TNS

GBTIA → lpGBTIA

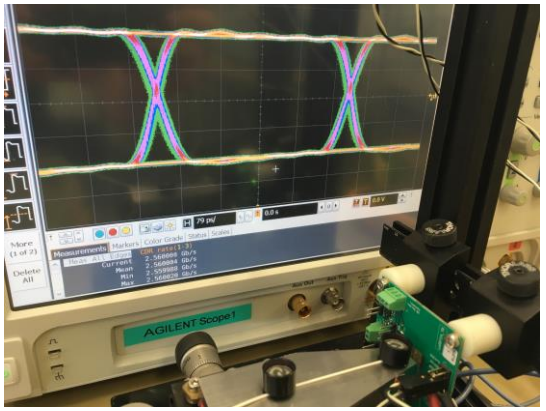
- InGaAs photodiode :
  - Advantage : Lower degradation of the responsivity with irradiation
  - Drawback : Strong increase of the junction capacitance with irradiation
- The GBTIA post-irradiation eye diagram shows a strong increase of the deterministic jitter
  - Jitter levels incompatible with the lpGBT applications, mainly for clock recovery
- lpGBTIA designed to cope with the InGaAs photodiode capacitance increase
  - Process CMOS 65nm
  - A constant output swing of 400 mV
  - For a power supply of 2.5 V the power consumption is 73 mW
  - For -6 dBm input :
  - Rise time = 30 ps
  - Total jitter = 0.15 UI @ BER = 10^{-12}



GBTIA : 2.56 Gbit/s
Pre-Irradiation



GBTIA : 2.56 Gbit/s
With Irradiated InGas photodiode



Eye diagram 2.56 Gbit/s
Optical power = -6 dBm
Differential

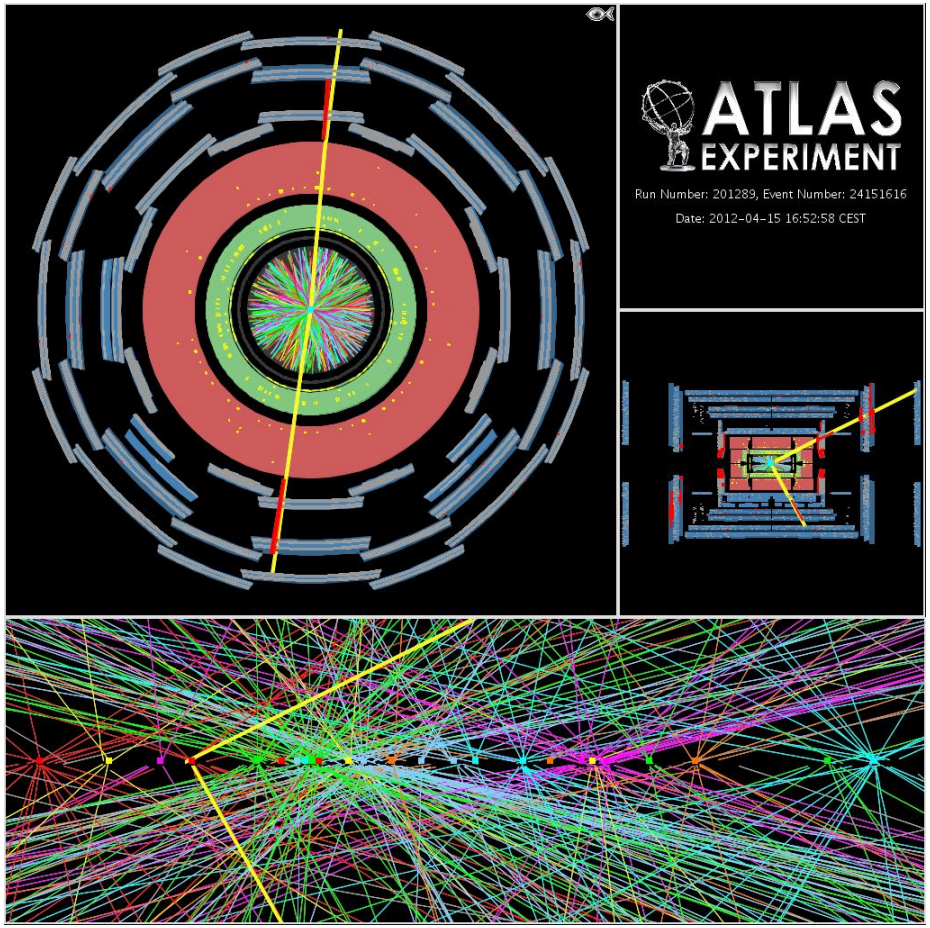
The lpGBTIA, a 2.5 Gbps Radiation-Tolerant Optical Receiver using InGaAs photodetector, M. Menouni et al.

Readout chips for Timing Layers

1. Pile up and detector requirements
2. HGTD detector and LGAD sensors
3. Readout chip architecture
4. Tests Results

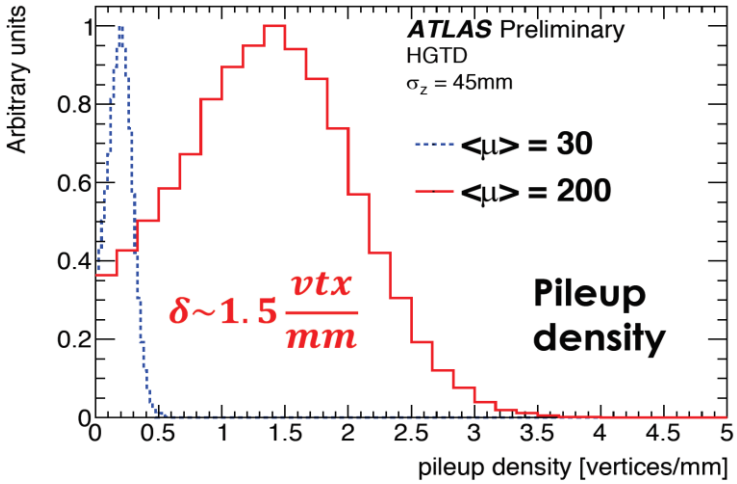
Pile Up in ATLAS

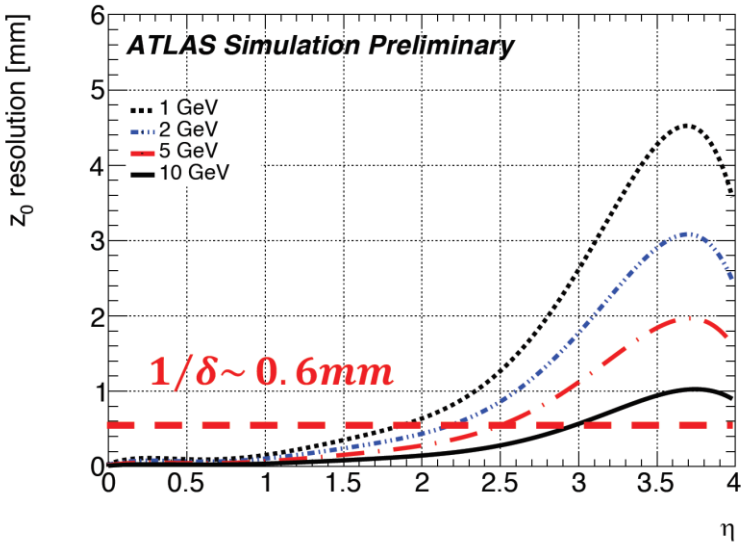
- Pile-up : interaction happening during the same bunch crossing as the relevant event
- Create tracks that could be associated by error to the event of interests
- Affect the signal reconstruction and can create fakes
- Increase of the instantaneous luminosity -> increase of the pile up
  - Run2 : **40 pile up** interaction in ATLAS (per bunch crossing)
  - HL-LHC : **200 pile up** interaction in ATLAS



Detector requirements

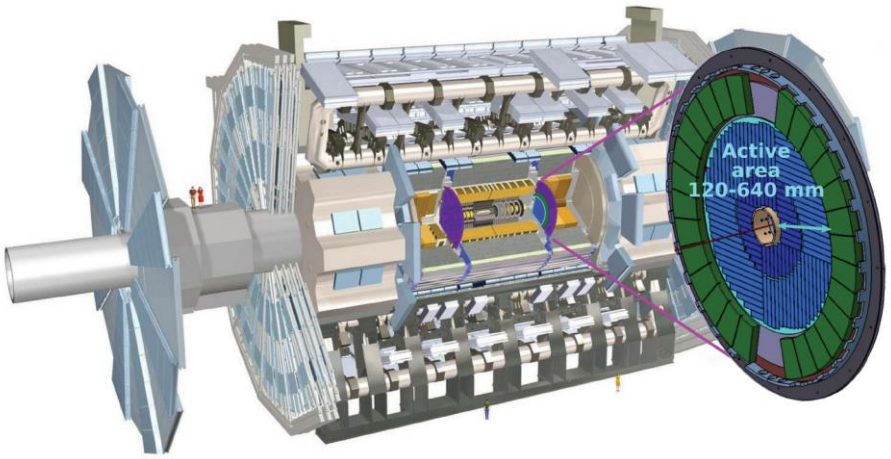
- Central region :
  - The tracker resolution in z0 is better than the typical distance between two vertices
  - The vertex reconstruction with ITk allows to separate vertices
- Forwards region : 2.4 < |η| < 4 (between 2° and 10° from the beam axis)
  - The z0 resolution becomes larger than the distance between two vertices
  - The association of tracks to vertices becomes ambiguous
  - **Exploiting the time measurement allows to separate these vertices**



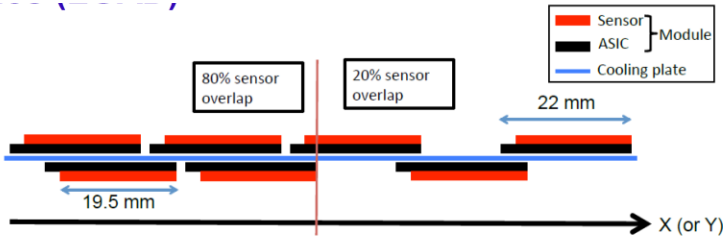


High Granularity Timing Detector - HGTD

- Geometry
  - Coverage: 2.4<|η|<4.0
  - Radial extension: 12 cm < R < 64 cm
  - z position: 3.5 m
  - Thickness in z: 7.5 cm
- Requirements
  - Excellent time resolution (30 ps/track)
  - radiation-hard
    - 3.7×10^{15} neq/cm^2 - 400 Mrad
- Low Gain Avalanche Detector (LGAD)
  - Pixel size: 1.3×1.3 mm^2
- 2 double planar layers per endcap
- Module
  - LGAD sensor
    - 450 PADs of 1.3 × 1.3 mm^2
  - 2 ASICs of 2 cm x 2 cm
    - 225 channels/ASIC
    - Bump bonded to sensor



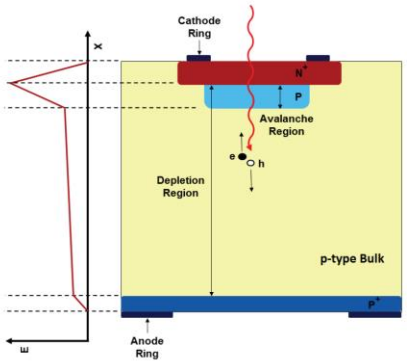
2 disks, 2 layers/disk
equipped on both sides with
Low Gain Avalanche Diodes



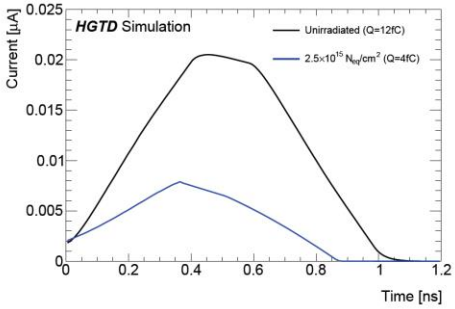
2

LGAD Sensor

- LGAD technology
  - n-on-p silicon detectors with extra highly-doped p-layer below the n-p junction
  - Create a high field which causes internal amplification
- The LGAD current, much larger than in a standard diode
  - Excellent time resolution for energy deposited by particles
- Timing precision
  - Large Signal
  - Low Noise
  - Short Rise Time



(a)



(b)

$$\sigma_t^2 = \sigma_{Landau}^2 + \sigma_{timeWalk}^2 + \sigma_{jitter}^2 + \sigma_{TDC}^2 + \sigma_{Clock}^2$$

e-h pairs density fluctuation

$$\alpha \frac{RiseTime}{S/N}$$

Readout ASICs

ALTIROC,
a 25 ps time resolution ASIC for ATLAS HGTD

N.Seguin-Moreau*[1], S. Conforti[1], C. de La Taille[1], P. Dinaucourt[1], G. Martin-Chassard[1], A. Dragone[2], B. Markovic[2], L. Ruckman[2], A. G. Schwartzman[2], D. Su[2], C. Agapopoulou[3], N. Makovec[3], S. Sacerdoti[3], L. Serin[3], D. Gong[4], J. Ye[4], W. Zhou[4]

TWEPP 2019

1 OMEGA Microelectronics 2 SLAC 3 LAL Laboratoire de l'Accélérateur Linéaire 4 SMU

IFAE Excelencia Severo Ochoa, BIST Barcelona Institute of Science and Technology — CNM Centro Nacional de Microelectrónica, IMB — Institute of High Energy Physics Chinese Academy of Sciences — LPC Particules Plasmas Univers application? Laboratoire de Physique de Clermont

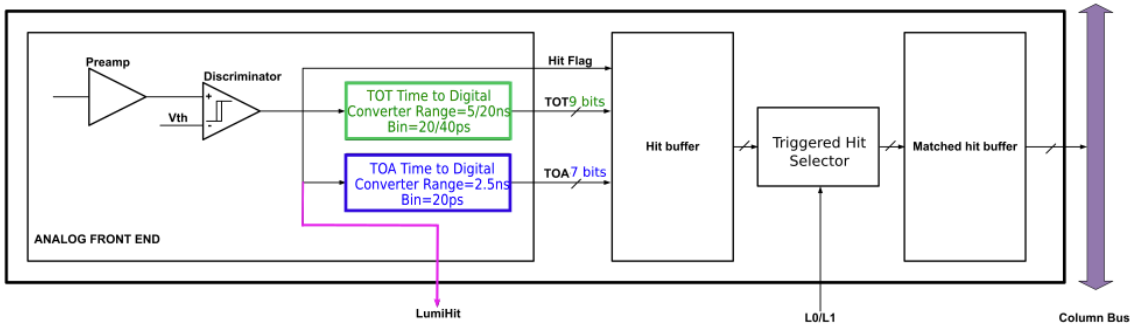
The ETROC Project: Precision Timing ASIC Development for LGAD-based CMS Endcap Timing Layer (ETL) Upgrade

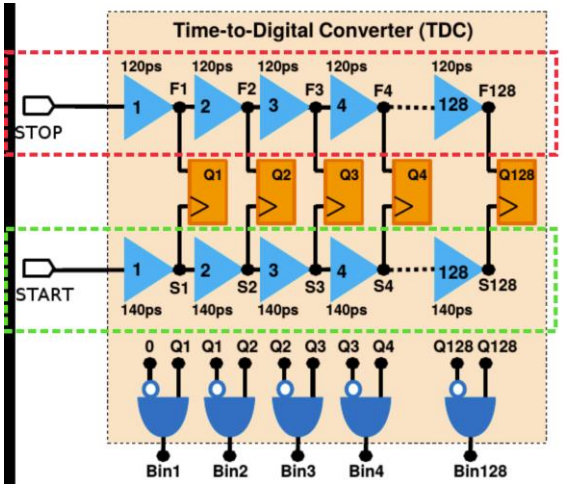
Tiehui Liu, Grzegorz Deptuch, Sergey Los, Sandeep Miryala, Jamieson Olsen, Luciano Ristori, Quan Sun, Jinyuan Wu
Fermi National Accelerator Laboratory, Batavia Illinois, USA
Datao Gong, Kent Liu, Tiankuan Liu, Hanhan Sun, Jingbo Ye, Li Zhang, Wei Zhang
SMU Physics, Dallas Texas, USA
Liang Fang, Tao Fu, Ping Gui, Xianshan Wen, Chi Zhang
SMU EE, Dallas Texas, USA
Siddhartha Joshi, Seda Ogrenci-Memik
Northwestern University, Evanston Illinois, USA
Sunil Dogra, Chang-Seong Moon, Jongho Lee
Kyungpook National University, Daegu, South Korea

KNU Kyungpook National University — Fermilab — Northwestern University

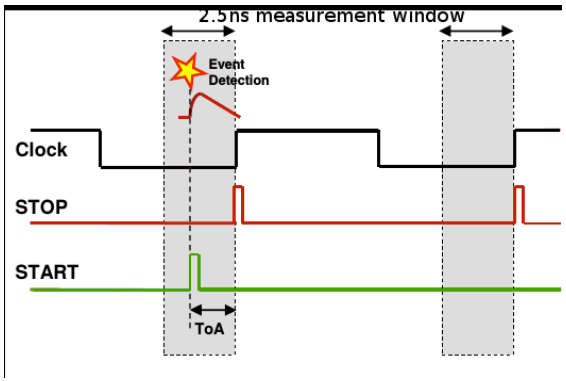
POSTER-19-119-E

Readout Chip architecture





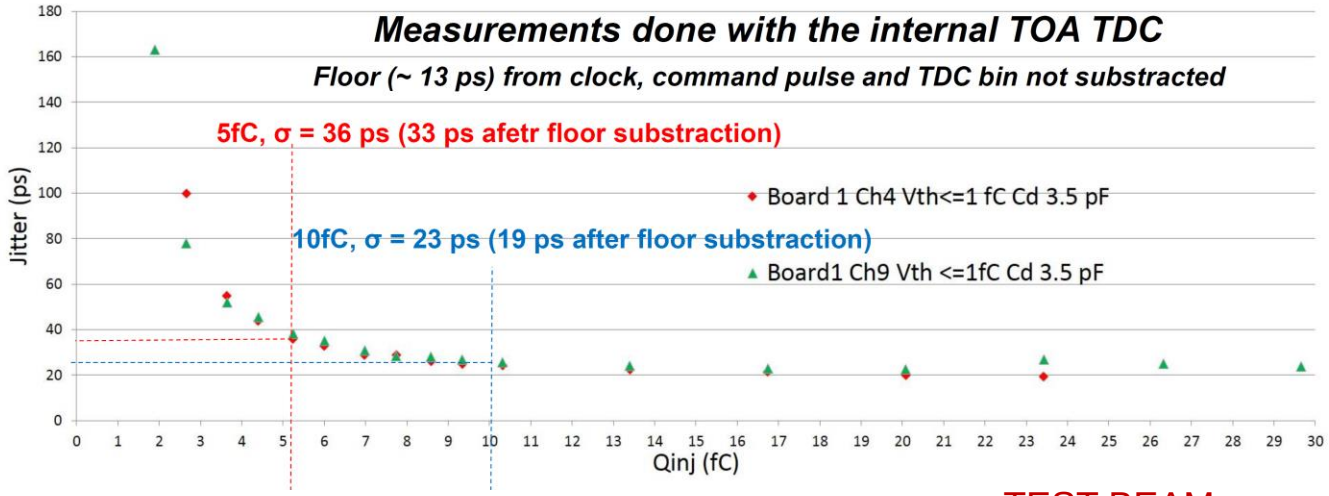
- A preamplifier followed by a discriminator
  - Time walk correction made with a Time over Threshold (TOT) architecture
  - Amplifier Bandwidth ~1 GHz (Current consumption ~ 1 mA)
- Two TDC (Time to Digital Converter) to provide :
  - Time of Arrival (TOA) measurement
    - Range of 2.5 ns and a bin of 20 ps (7 bits)
  - Time Over Threshold (TOT) measurement
    - Range of 20 ns and a bin of 40 ps (9 bits)
- One Local memory (SRAM)
  - Store the 17 bits of the time measurement (Hit data) until L0/L1 trigger (~ 1 MHz) => trigger latency = 35 µs



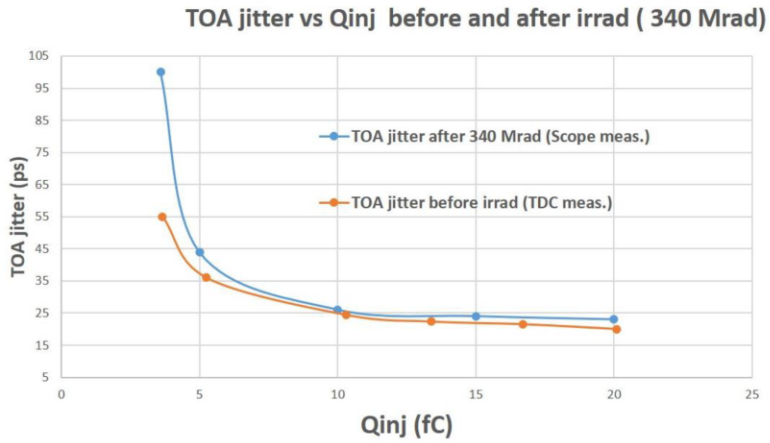
ALTIROC, a 25 ps time resolution ASIC for ATLAS HGTD, N.Seguin-Moreau et al.

Main Results

ALTIROC1_V1: Jitter vs Qinj measurement (Cd=3.5 pF)

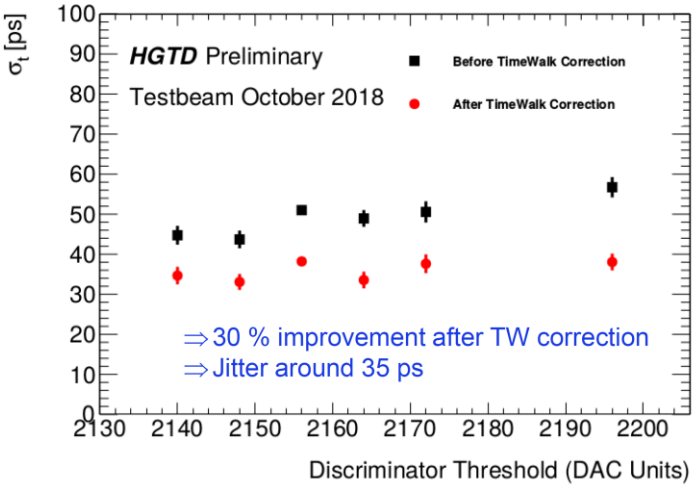


Irradiation tests with Altiroc1_V1



TEST BEAM measurements with Altiroc0_V2

(4 x1x1 mm2 LGAD array bump bonded to the ASIC)

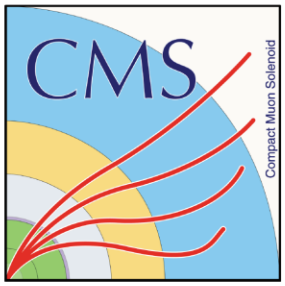


ALTIROC, a 25 ps time resolution ASIC for ATLAS HGTD, N.Seguin-Moreau et al.

Thank you for your attention

Main Results

Backup Slides



First experimental results on TOFHIR readout ASIC of the CMS Barrel Timing Layer

Tahereh Niknejad

Laboratory of Instrumentation and Experimental Particle Physics (LIP)

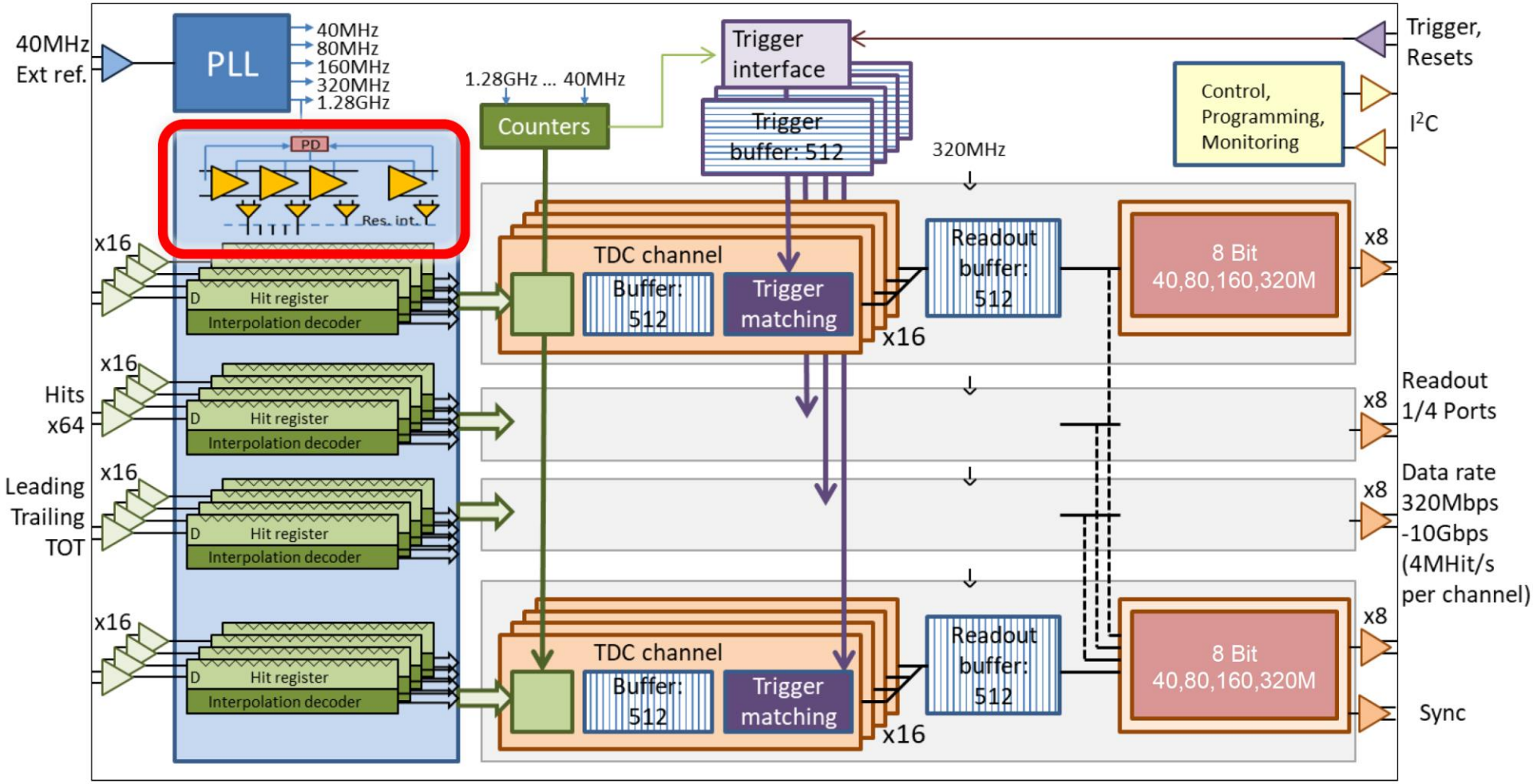
Other High resolution TDC

picoTDC:
A 3ps Bin Size 64 Channel TDC for HEP Experiments

Moritz Horstmann (CERN/CAEN)
Jorgen Christiansen, Jeffrey Prinzie (KU Leuven), Samuele Altruda

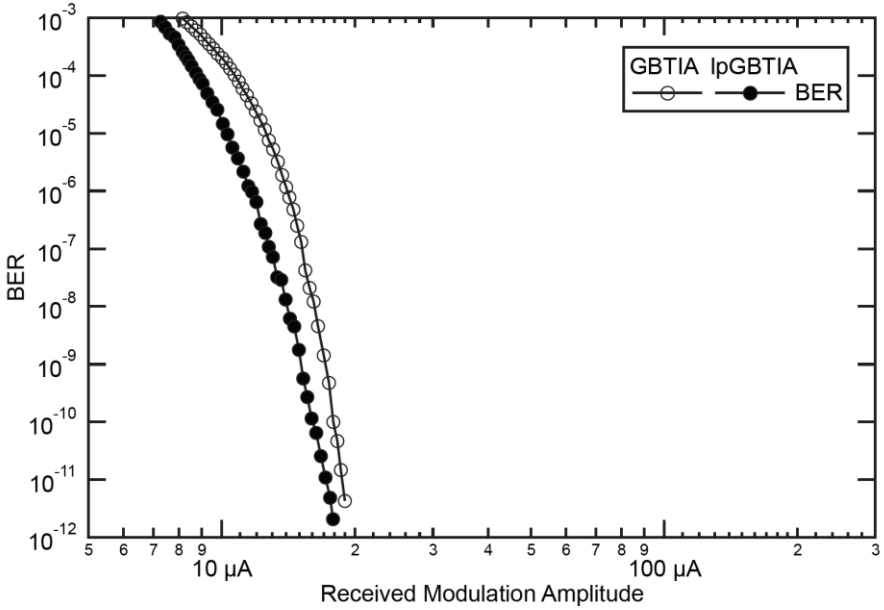
- [redacted]
- Size of the chip (including the seal-ring) = 1750µm x 461µm

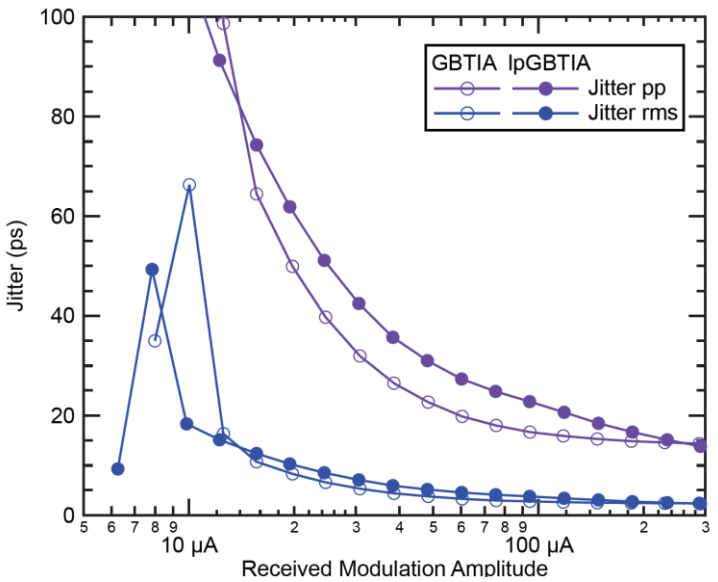
Pico TDC architecture

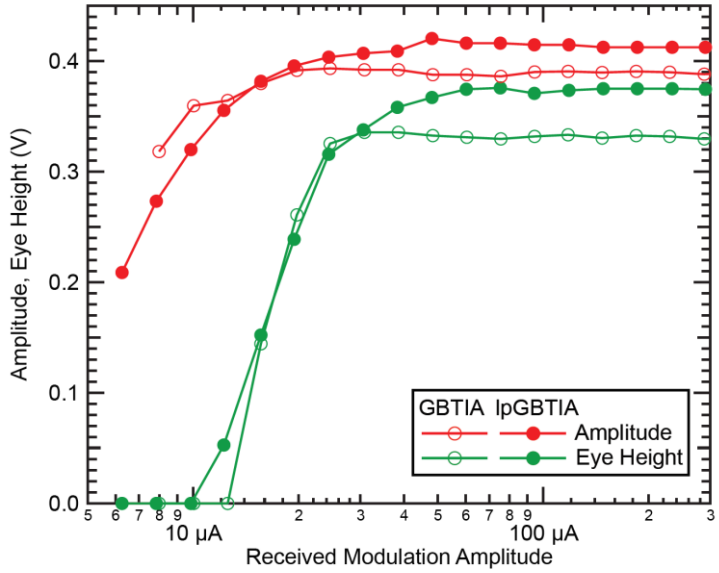


lpGBTIA design

lpGBTIA performance

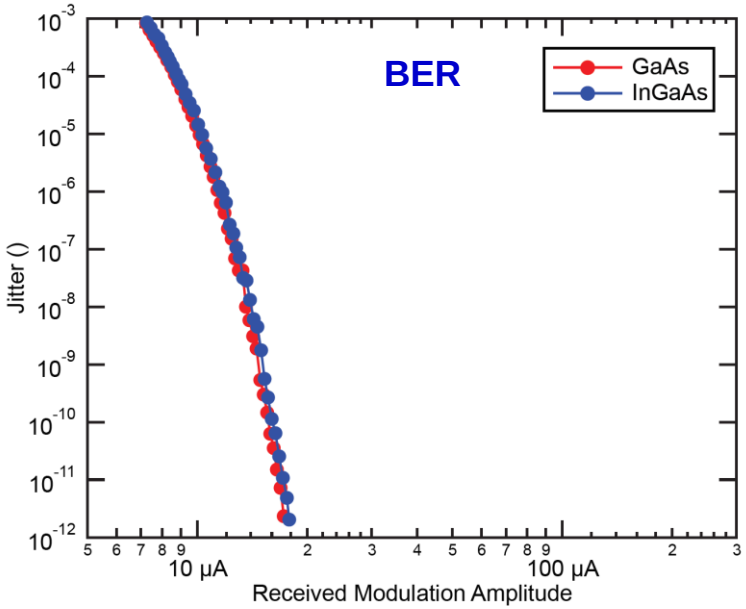


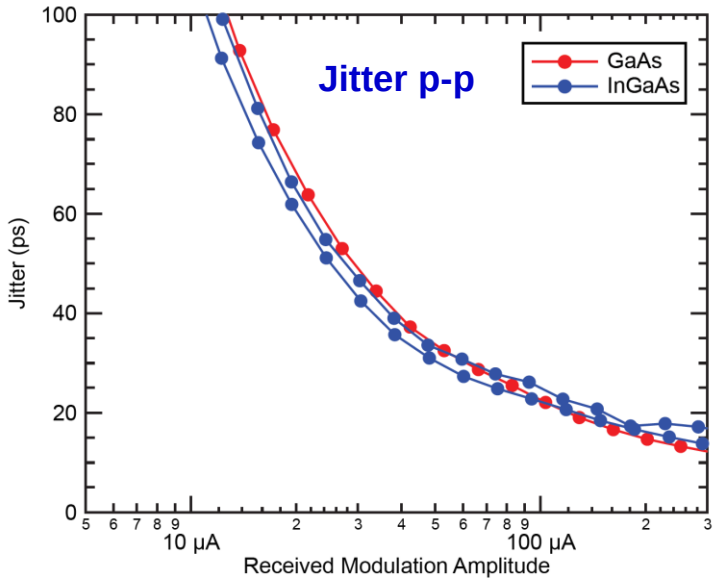


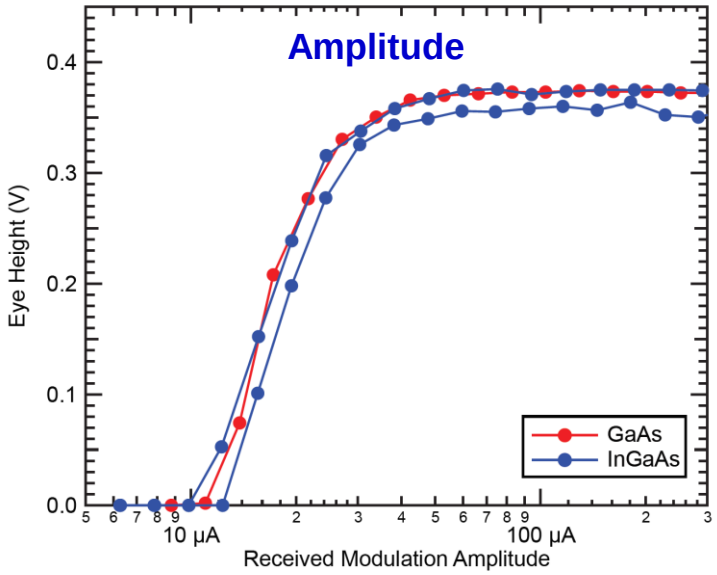


- Pre-irradiation results
- InGaAs photodiode capacitance <400 fF
- At 2.56 Gbps, the lpGBTIA is showing similar results as for the GBTIA receiver
  - Similar Sensitivity, Eye amplitude, Eye height
  - The measured Jitter is higher for the lpGBTIA due to non-50% crossing point

lpGBTIA performances



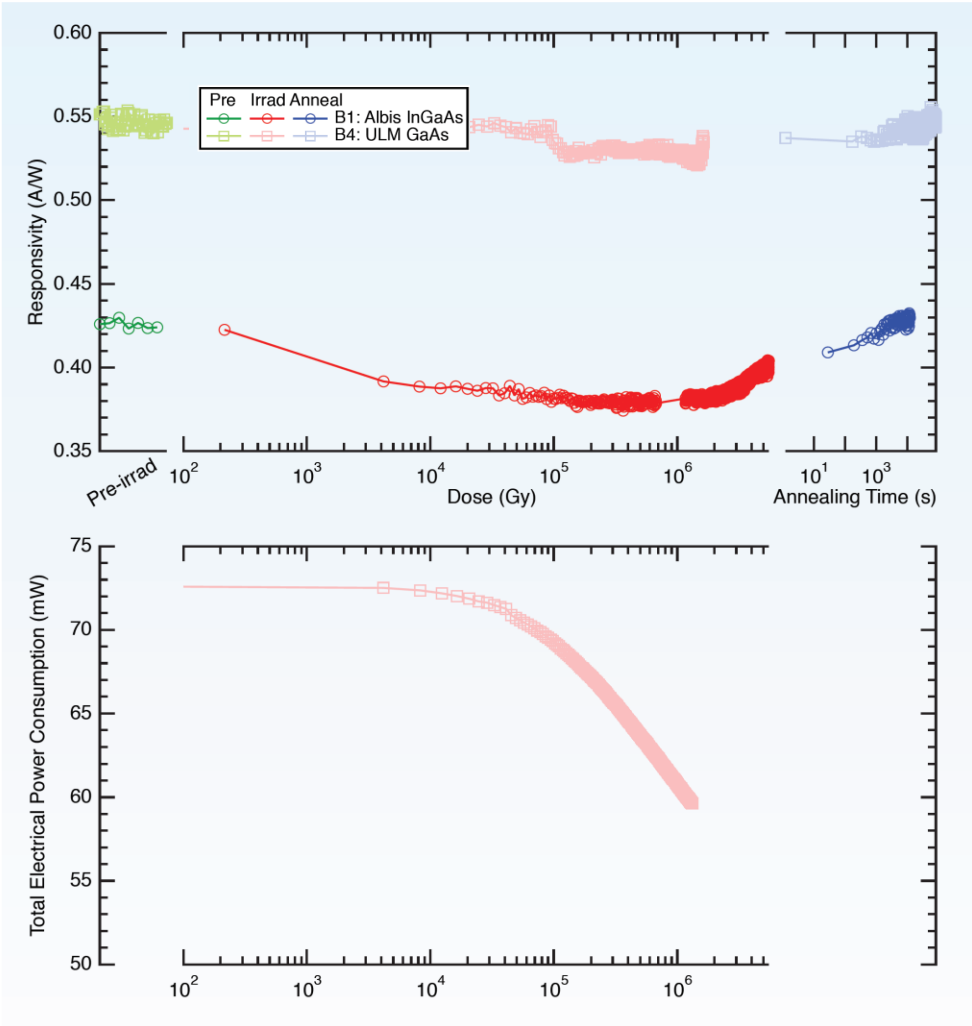




- Pre-irradiation results performances are very similar for receivers based on InGaAs or on GaAs photodiode
  - Negligible leakage current for both devices
  - Similar junction capacitance before irradiation (< 400 fF)

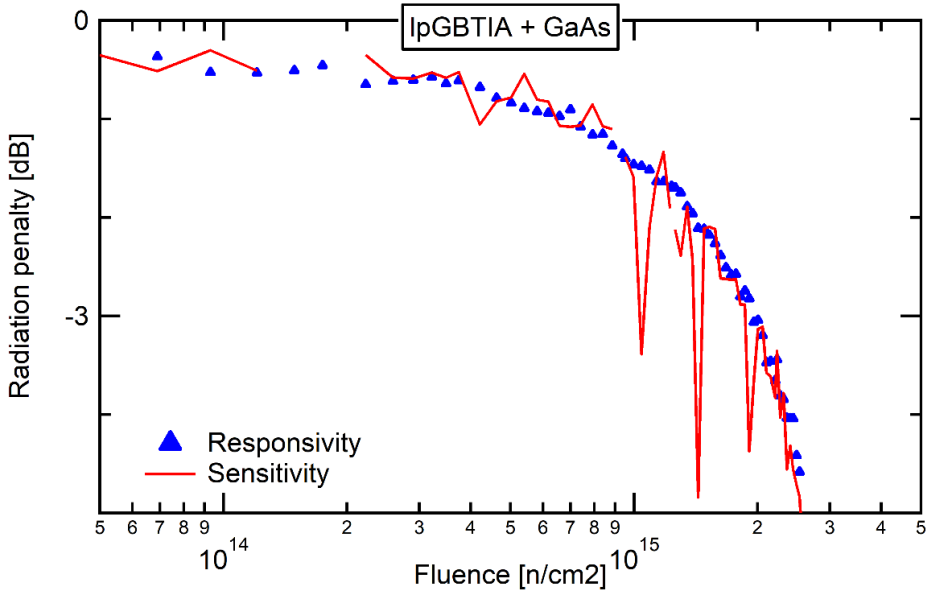
Xray Irradiation

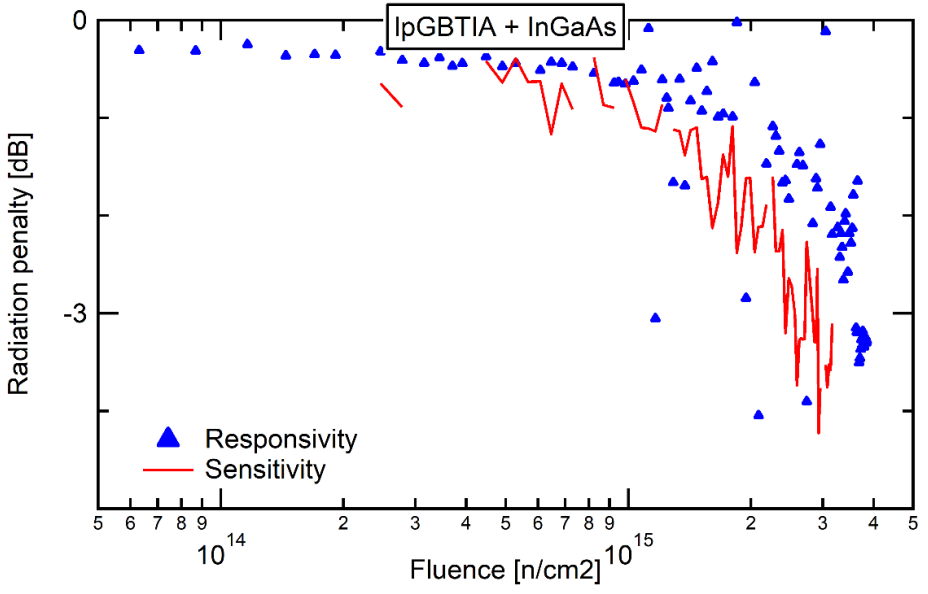
- 2 samples were measured
  - B1: Albis InGaAs photodiode tested up to 550 Mrad
  - B4: ULM GaAs photodiode tested up to 160 Mrad
- Dose rate : 9 Mrad/hour
- External power applied to both 2.5 V and 1.2 V pads
- The power consumption decreases with the TID
  - Thick oxide transistors used for 2.5V to 2V conversion
- The responsivity loss is < 15% for the InGaAs sample and recovers its initial value with annealing
- Sensitivity and jitter not affected
- Eye-parameters vs input optical power seems unchanged regarding the pre-irradiation values



Neutron Irradiation

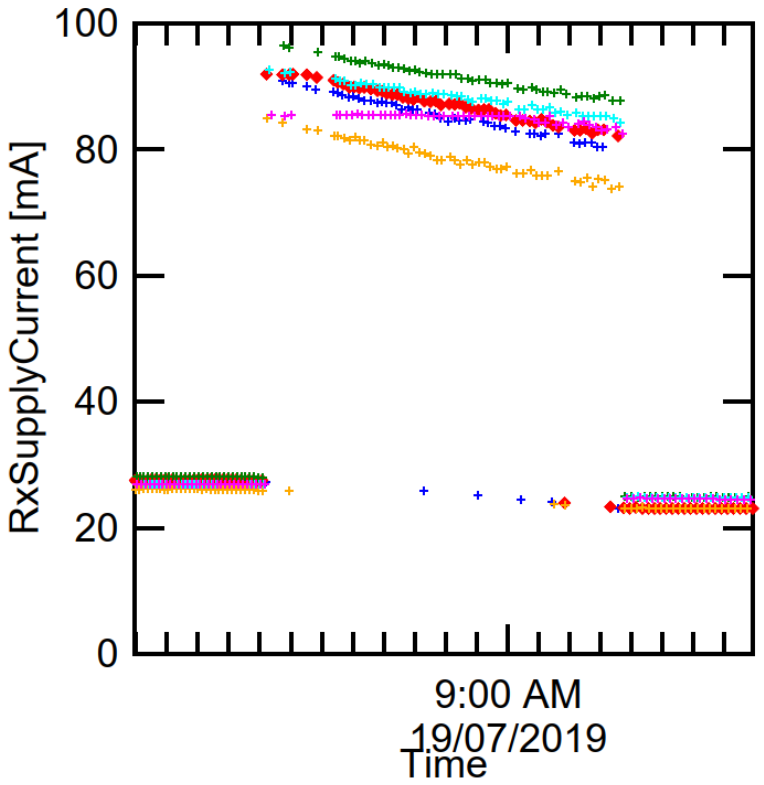
- Several samples exposed to 20 MeV neutrons at the Cyclotron of Louvain la Neuve (T2 beamline)
- Receiver based on InGaAs photodiode is showing better results than GaAs after irradiation in terms of sensitivity or responsivity
  - Validating the architecture choice





Unexpected

- During neutron irradiation, the supply currents increase by a factor of 3 when the beam was turned on
  - Chip remains operational with unaffected sensitivity, jitter and eye-characteristics
- Current returns to normal after a power cycle
- Behaviour not understood.
  - SEU Heavy-Ions test the coming week for further investigation
  - Possibly followed by two-photon testing to identify the “failing” mechanism



Conclusion and Perspectives

- The 2.56 Gbps lpGBTIA receiver is developed with the commercial 65 nm process
- The design maintains good performance coping well with the shift of the InGaAs photodiode parameters with irradiation
  - Leakage current and junction capacitance increase
- A new photodiode bias circuit is proposed and implemented in order to maintain the photodiode capacitance at a reasonable value
- The optical receiver based on the lpGBTIA and InGaAs photodiode was tested and showed good performance at 2.56 Gbps
- Several samples were irradiated with X-ray and 20 MeV neutrons
- Irradiation tests showed that the performances in terms of responsivity and sensitivity are still acceptable for $3x10^{15}$ n/cm2
- Increase of the power consumption while irradiated
  - Still to be understood
  - Heavy – Ions and Two-Photon SEU tests to be done soon

Thank you for your attention

Main measurements

- The main receiver side parameters are : responsivity and sensitivity
- Measured by attenuating the input signal with predefined steps and measuring :
  - The photocurrent level (RSSI signal)
  - The Bit Error Rate (BER)
  - The input optical power at each attenuation step
- The responsivity is derived from a linear fit of the photo current versus the input optical power
- The sensitivity is defined as the input optical modulation amplitude producing a BER of 10^{-9}
- The signal amplitude, the eye height and the Jitter are extracted from the measured eye diagram

Le chip GBTIA

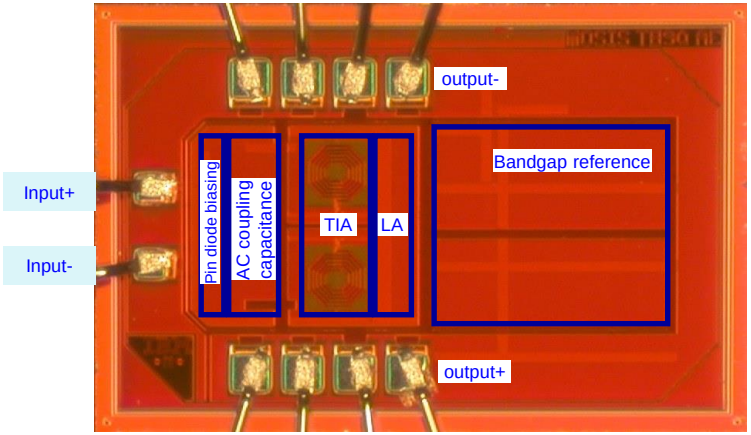
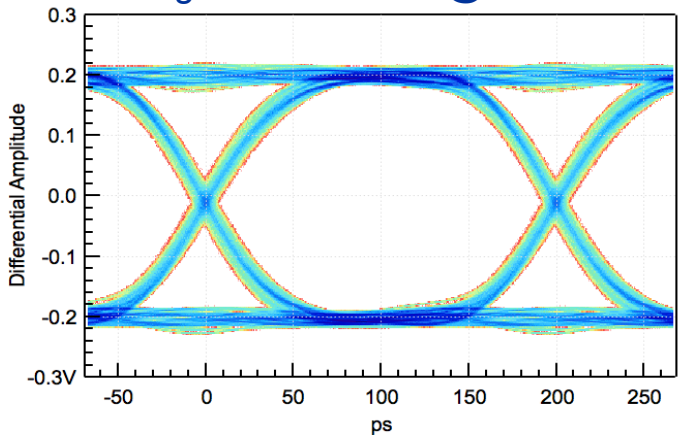


Diagramme de l'œil @ 5 Gb/s

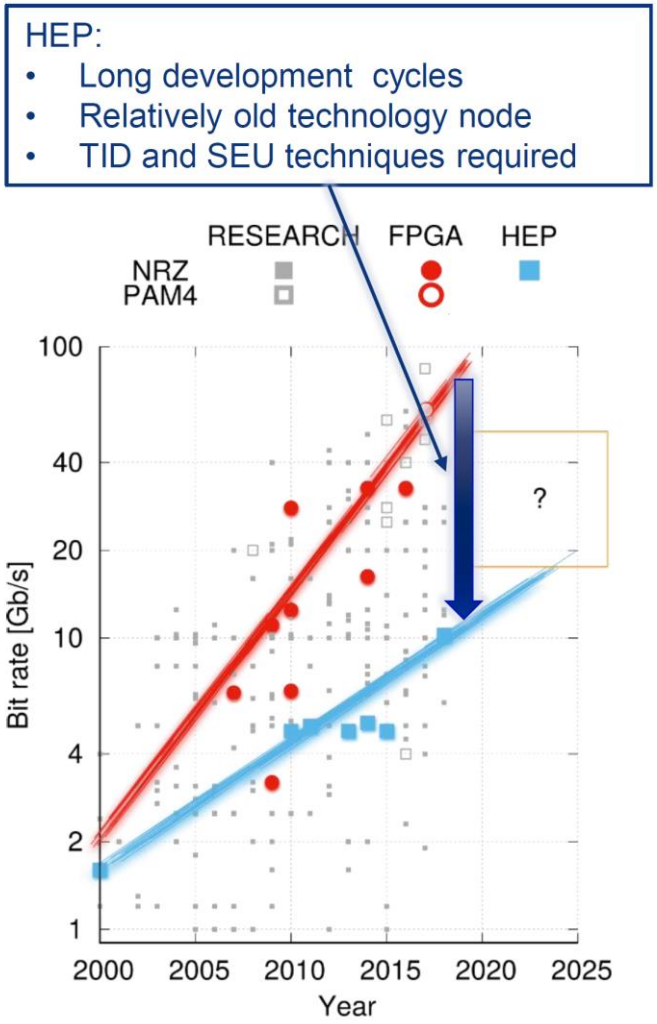


GBTIA-ROSA

- Process CMOS 0.13 µm.
  - ❑ n-MOSFET : f_T de l'ordre de 100–120 GHz
  - ❑ Taille du chip : 0.75 mm × 1.25 mm
- Excellentes performances
- 5 Gbits/s : sensibilité de -19 dBm pour BER=10^{-12}
- Consommation < 120 mW
- Tolérance aux radiations > 200 Mrad
- Nouveau design en 65 nm pour début 2018

Performances actuelles

- Performances des ASICs pour la physique des particules sont limitées :
  - Longs cycles de développement
  - Qualification pour la tolérance à la dose
  - Utilisation d'anciennes générations de process (accès et coût)
  - Techniques de design Circuit:
    - Tolérance à la TID et aux SEU
- Pour les R&D 2020 to 2025
  - Cibler 20 - 40 Gb/s
  - Compatibilité avec les performances des FPGA



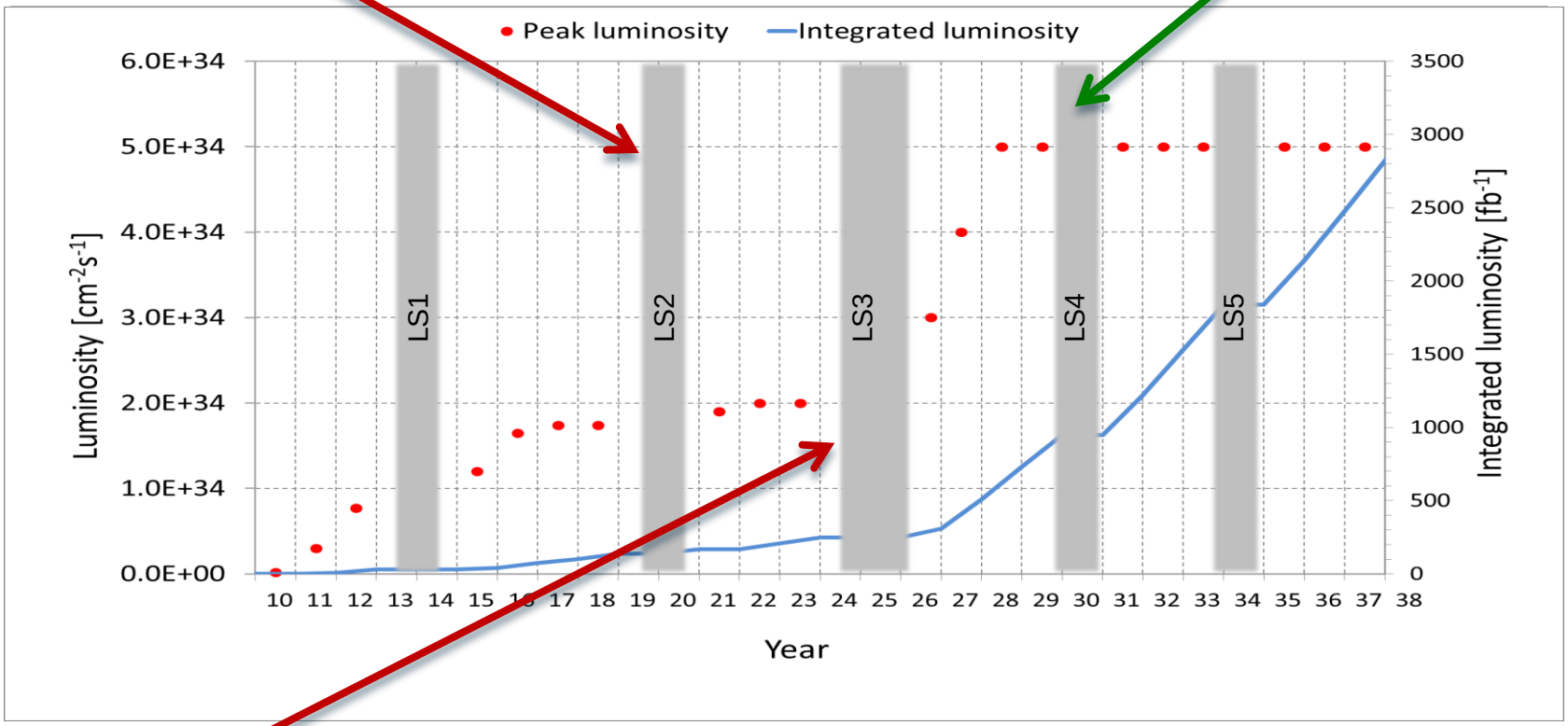
Futur developments

- Développements futurs de liens haute vitesse (optiques ou électriques) dépendent de :
  - Machine et des niveaux de radiation :
    - HL – LHC: > 100 Mrad
    - CLIC: < 1 Mrad
    - FCC: > 1Grad
  - Type du détecteur (Detectors à pixels, Calorimètres)
  - Vitesse requise pour la transmission
  - Puissance
- programme R&D (2020 – 2025) :
  - Upgrade HL-LHC (“LS4”)
  - Préparer la voie pour d’autres projets futurs (FCC, ...)
  - Quantité de données très importante
  - Environnement niveaux d’irradiation extrêmes

Planning du LHC

PHASE I Upgrade
ALICE, LHCb major upgrade
ATLAS, CMS ,minor upgrade

PHASE III Upgrade
R&D: 2020 - 2025

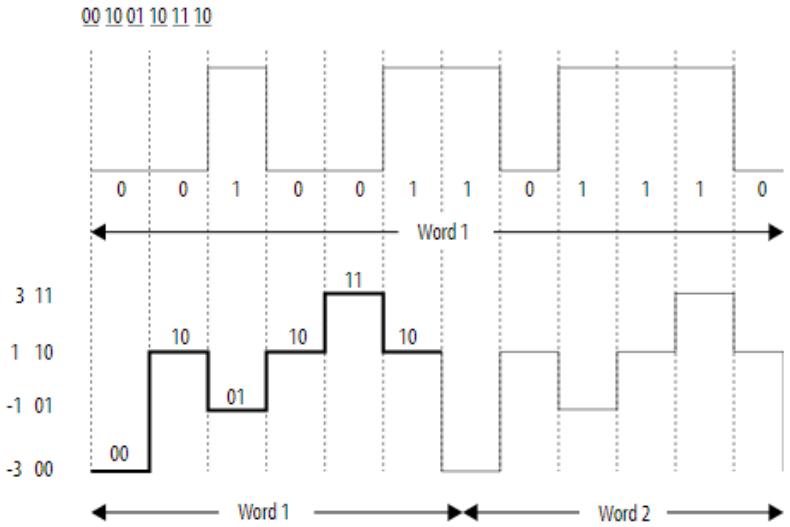


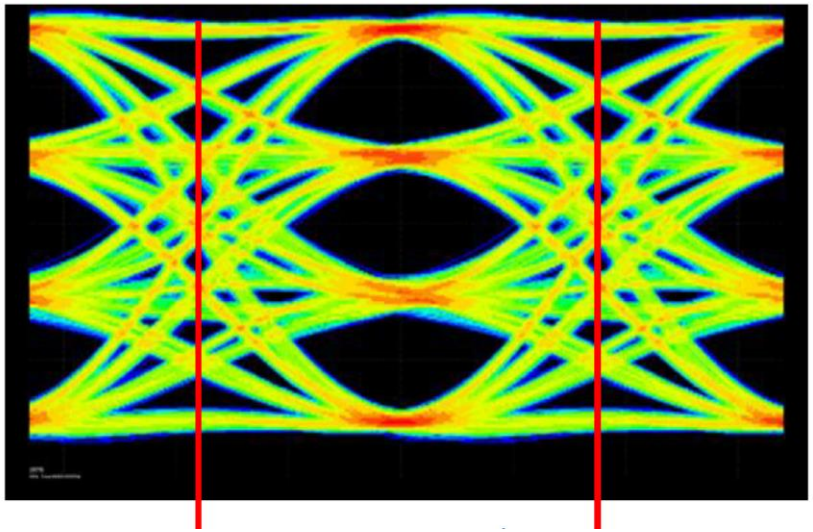
PHASE II Upgrade
ATLAS, CMS major upgrade

Radiation hardness

- Radiation hardness is the major technical challenge:
  - High-Speed CMOS Asics currently being used by the HEP community will not survive TID doses higher than **100 / 200 Mrad**
  - Experience in qualifying active optoelectronic components points to the exclusion of opto-devices for radiation environments exceeding **3×10^{15} n/cm2**
  - The radiation resistance is not changing with **new generations of optoelectronic components**
- Possible Solutions:
  - Explore new commercial IC technologies
    - Large qualification work
  - Explore new optoelectronic devices:
    - Optical modulators with external and remote laser source
  - Explore electrical links for extreme radiation environments:
    - Large bandwidths in low mass cables might be difficult to achieve (RD53)

New FPGA standard





- 58G PAM4 standardization:
- PAM-4 standard within the IEEE 802.3 Ethernet and Optical Internetworking Forum (OIF)
- Breaks through the physical limitations of data transmission at 50 Gps line rates
- Features next generation equalization technologies to minimize channel loss
- Supports chip-to-chip, direct-attach cable, and backplane communication

Proposition de Projet

- Vitesse de données est très corrélée au **nœud technologique**
- Utilisation de **Format de modulation de type PAM4** : Doubler la vitesse de donnée
- CERN commence à travailler dans cette direction
  - Process 28 nm ?
    - Qualification en TID dans le cadre du CERN
- Design de blocks génériques pour les futurs liens optiques/circuits à pixels
    - PLL & CDR
    - Serializers/DeSerializers
    - Laser / VCSEL Drivers
    - PIN – Receivers
    - ADCs + building block for PAM4 receivers): 56 GS/s (28 nm CMOS)
    - Drivers et recepteurs pour câbles électriques
- Travail peut être effectué en collaboration avec l'équipe du CERN