# A Proposal for the Timing Distribution System in Hyper-Kamiokande

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### Timing system requirements

Major requirements #1 clock

- Distribute 125MHz (62.5MHz?) clock to all the front-end electronics modules.
- Transmission via Multi-mode optical fiber
- Jitter have to be smaller than ~100ps.
- Reference clock is provided by an external GPS receiver. (10MHz?)
- Delay compensation scheme is necessary.
- However, fixed delay of a few ns is acceptable.
- Delay or phase change is not allowed even after the reset or power cycle.

### Timing system requirements

Major requirements #2 counter

- Distribute 32bit counter and auxiliary information to the frontend electronics modules.
- Counter is generated in the master module. Reset is requested by the DAQ system.
- Auxiliary information includes TDC reset, reset and FPGA firmware, i.e. distribution of the new firmware, etc.
- Each front-end electronics module sends back status information, like # of hits in 17 micro sec. (=TDC counter reset interval), status of the module, LV and HV monitor values etc.



From Yoshinari Hayato for WG4 presentation

## What Do We Need?

- The requirements calls for a bidirectional data exchange link
- The requested bandwidth seams low (not exactly defined yet)
- Extra bandwidth can be useful

The goal is to implement a synchronous, phase deterministic protocol with as large as possible bandwidth

# How Do We Implement it?

R&D already started!

Many solutions are under consideration but 2 of them seam promising

- CERN White Rabbit
- Custom solution

# How Many Nodes?

HK PMTs numerology :

- 8k large single PMT in the outer detector
- 20k large single PMT in the inner detector
- Up to 20K multi-PMT spheres in the inner detector

HK FE numerology :

Each Front-End gathers signals from 25 PMTs

- 320 FE for the outer detector
- 800 FE for the large PMTs inner detector
- 800 FE for the multi-PMTs inner detector

# **CERN White Rabbit**

Fully deterministic gigabit ethernet-based solution to distribute data and time

- Single master many slaves
- The master receives GPS's signals, generate a clock and distributes it
- Propagation delay actively compensated
- Synchronization requires very few bandwidth (~400 Bps)
- White Rabbit node can talk with standard ethernet nodes
- 18 ports white rabbit switches are "of-the-shelf"
- CERN distributes hardware and firmware design and support them

### CERN White Rabbit A possible architecture

### 8 links 8 links DAQ WR switch WR switch ... ... 25 25 25 25 8 8

### **Custom Solution**

#### Based on FPGA's ser-des fixed phase locking system

- Point-to-point
- Each master can receive GPS's signals or signal from clock fanout generate a clock and distributes it
- Synchronization doesn't require any data bandwidth
- Slave's clock phase delay is proportional to the signal propagation
- Custom FE link with tailored bandwidth
- DAQ link is standard (i.e. 10Gbps ethernet)
- Concentrator connections depends on the requested bandwidth
- Hardware and firmware design is custom

## **Custom Solution**

#### A possible architecture (assuming 1Gbps to FE)



### **Cost Estimation**

### Total cost is calculated adding 20% contingency and 20% spares

#### White Rabbit

- 28.000 large PMTs (inner + outer)
- (1.120/8) x 5.300 = 742.000 euro
- 4.000 multi-PMT
- (160/8) x 5.300 = 106.000 euro
- 20.000 multi-PMT
- (800/8) x 5.300 = 530.000 euro

#### TOTAL COST

- Baseline: 1.038.800 euro
- Extra 4.000 multiPMT: 148.400 euro
- Extra 20.000 multiPMT: 742.000 euro

### **Custom Solution**

- 28.000 large PMTs (inner + outer)
  (1.120/8) x 4.000 = 560.000 euro
- 4.000 multi-PMT
- (160/8) x 4.000 = 80.000 euro
- 20.000 multi-PMT
  (800/8) x 4.000 = 400.000 euro

#### TOTAL COST

- Baseline: 784.800 euro
- Extra 4.000 multiPMT: 112.400 euro
- Extra 20.000 multiPMT: 560.000 euro

# Summary

### White Rabbit

### Pros

- Very good timing distribution performances.
- Very reliable since is developed and supported by CERN.

#### Cons

• Higher price

### **Custom Solution**

#### Pros

- Link tailored to the experiment's needs.
- Lower price.

#### Cons

• Design process is time consuming and prone to delay.