SMART

A new electronic design @ GANIL/DELTA

Sfp connectivity and Microtca for Advanced Remote Trigger

Smooth Upgrade of CENTRUM and GTS towards a new time stamping system with trigger option

« Made in GANIL »

For all GANIL needs

and other collaborations AGATA, GRIT, …

if interested …

A bit of history …

Clock &
Event
Number
Transmitter
Receiver
Universal
Module
(VXI-C size)


Caen, Saclay, Bordeaux


Michigan, Texas,Indiana


Catania, Legnaro


Riken, JPARC


Daejeon

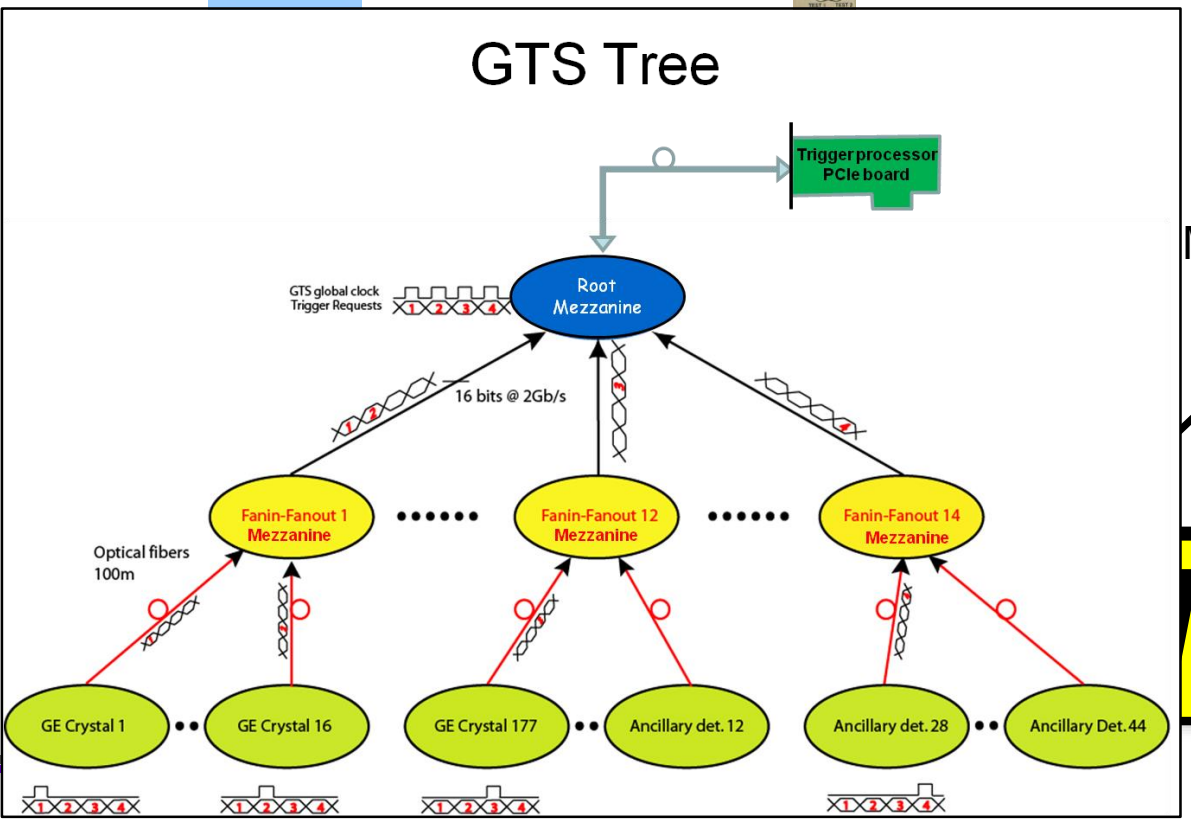

Leuven


Shanghai, Hong Kong, Lanzhou

2010

MUltiplicity Trigger ANd Time

GTS Tree



Slideshow plan

1. Present status / Motivations
2. Items retained / deleted
3. New elements
4. Global architecture
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6. Design strategy
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10. Two examples of possible SMART use in exiting systems
11. Conclusion

1 – Present status
Motivations

- ✓ Difficult to propose CENTRUM coupling for the next years
  coupling easy to use but VXI based without any trigger features

- ✓ GTS-V3: custom mezzanine with obsolete components

- ✓ Available quantity limited and dedicated to existing digitizers (numexo2)

- ✓ GTS/TP: Firmware with many files written or modified by a large number of engineers over the last 10 years and not always documented (→ reverse engineering)

- ✓ Need a powerful solution easy to use/deploy by GANIL
  or any other interested laboratory, all that in the mid term

- ✓ New solution should be used with any kind of FPGA based target board
  minimum requirements (1SFP connector or 1 AMC port + 1MGT)

2 – Items retained / deleted

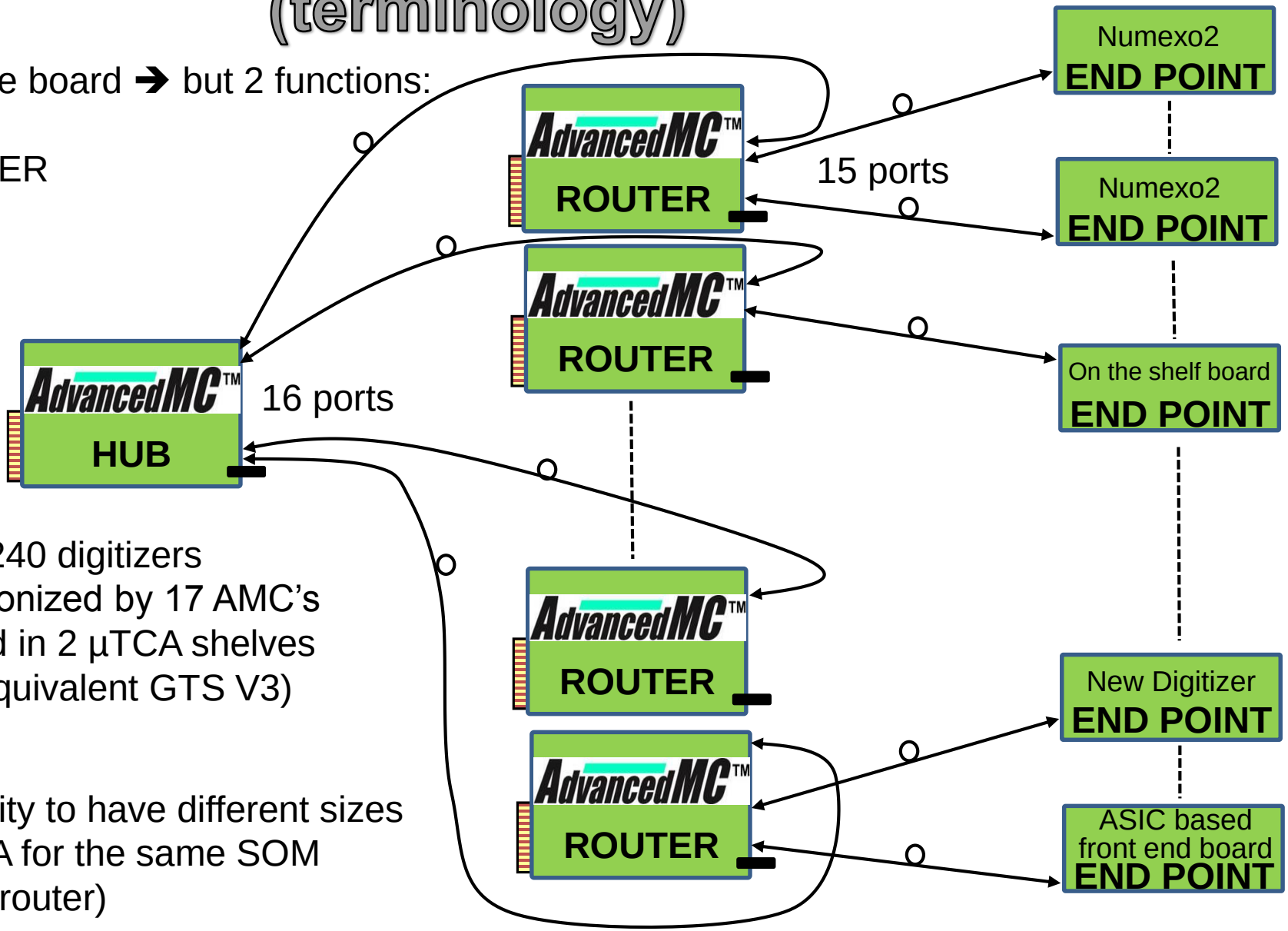
- ✓ Providing same key information:
  - ➔ TS 48 bits/10ns and 32 bit event number
- ✓ Unique 100 MHz clock for synchronization (CDR)
- ✓ Transmission @ 2Gbit/s with 8B/10B encoding towards digitizers and new boards to synchronize …
- ✓ Connectivity and data transmission media saved
  - ➔ SFP connectors, optical transceivers, fiber and/or copper cords
- ✓ Architecture foreseen, « sized » for trigger option
- ✓ Clock alignment managed by the new solution, able to handle boards without or with fine delay adjustment (like GTS LEAF with delay line & slow control)
- ✓ Internal GTS/Trigger processor protocol abandoned

3 – New elements

- ✓ Use of µTCA standard fully mastered by GANIL/DELTA (IN2P3 rec.)
  - ➔ Double / Full size AMC form factor (carrier) in “dual star” shelves
- ✓ Integration of «**S**ystem **O**n **M**odule » durable industrial solution as opposed to the kit reducing costs, engineering time and design errors
- ✓ Use of « lightweight » but robust protocol adapted to small packets of data that have to be transmitted efficiently
- ✓ Transmission @ 4Gbit/s - 8B/10B encoding between new boards (HUB/ROUTER), main alignment done in the FPGA
- ✓ Build with Xilinx Zynq FPGA (ARM processing/16 Multi Gigabit Transceivers) and the latest Xilinx Zynq UltraSCALE+ (32 MGT’s if AMC13)

4 – Global Architecture (terminology)

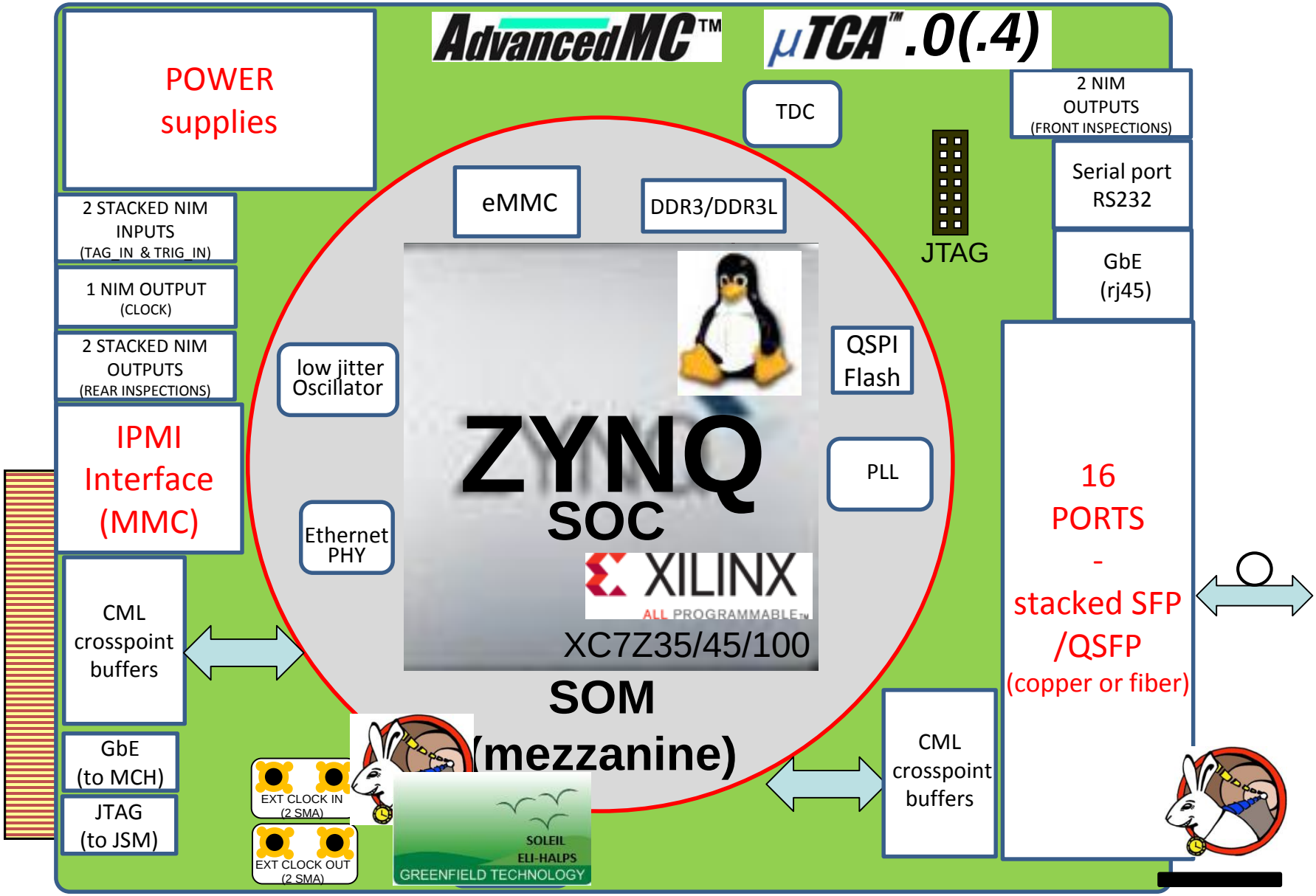
Only one board ➔ but 2 functions:
- HUB
- ROUTER



Up to 240 digitizers synchronized by 17 AMC's housed in 2 µTCA shelves (120 equivalent GTS V3)

Possibility to have different sizes of FPGA for the same SOM (hub or router)

5 – SMART draft AMC (H/R)

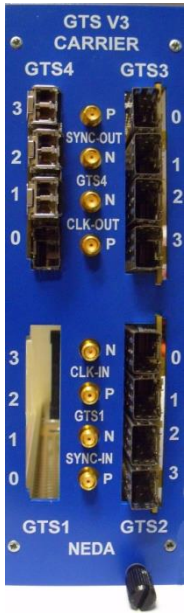


6 – Design strategy

Phase 1 - Phase 2 …

- ✓ AMC (hub/router)
  - ➔ Triggerless solution validation (CLOCK - TS/EVTNUM)
- ✓ AMC (hub)
  - ➔ Trigger option « de base » (functions/performances vs resources)
- ✓ If more important needs, AMC 13 development with «System On Module » based on UltraScale+ MPSOC for higher trigger level (GTS TP+ type, trigger on hit pattern with CPU/GPU, …etc.)
- ✓ In this case, porting of the initial solution at up to 480 synchronization/trigger links (2xPhase1)
- ✓ Specifications / Presentations / Documentation/ Support
- ✓ Mass production / Valorization

7 – Project summary



- ✓ System design fully mastered by GANIL/DELTA (HW/FW/eSW/GUI)
- ✓ 15 links/5000€ vs 9 links/9000 € (4 GTS/1NIM carrier)
- ✓ 2 years for this first coupling solution HUB/ROUTER prototype
- ✓ Keeping all existing connection elements
  (optical transceivers, fibers, …)
- ✓ Use of latest or ultra latest SOC FPGA in order to guarantee
  a 15/20 years durability
- ✓ Open system also addressed to future developments/external labs
- ✓ DELTA project (a minimum of 5 people involved…)

8 – Phase 1

From few links

4 ports (TX/RX) - QSFP↔ 4SFP
Copper (TurboTwin): 3m (~100€)
Fiber (OM3): 300m (~300/400€)

Up to 240 links of coupling/trigger …

First examples of use in terms of « Physics » channels number:

-3200 ch. Based on a 16 ch. DIGITIZER (NUMEXO2 type)

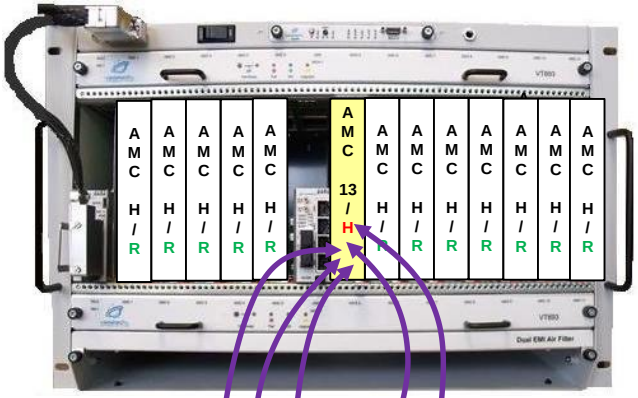
- 12800 ch. if coupling 64 ch. ASIC FE board (SAM type - 1 AGET)

- 51200 ch. if coupling 256 ch. FE ASIC board (GET/ASAD type - 4 AGET's)

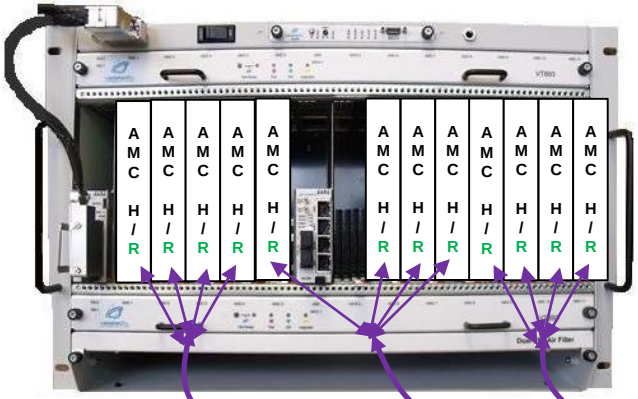
Is the system scalable ?

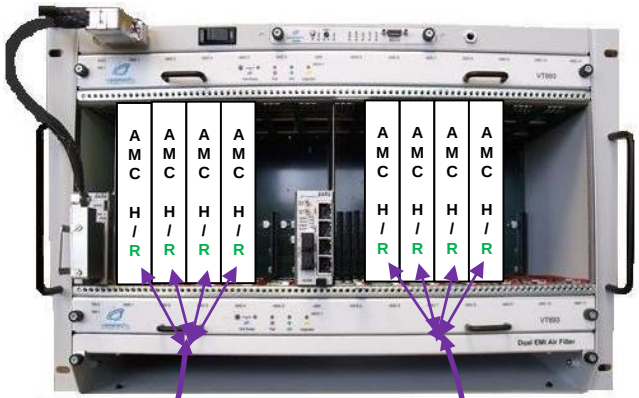
8 – Phase 2
Topology A

"AMC13" - MPSOC (Zynq UltraSCALE+)
12 backplane ports + 20 front panel ports (with 5 QSFP)
➔ 32 ports to feed "ROUTER" modules



≈ up to 480 coupling/trigger links …





Other examples of use in terms of « Physics » channels number:

-7680 ch. based on a 16 ch. DIGITIZER (NUMEXO2 type)

- 30720 ch. if coupling 64 ch. ASIC FE boards (SAM type - 1 AGET)

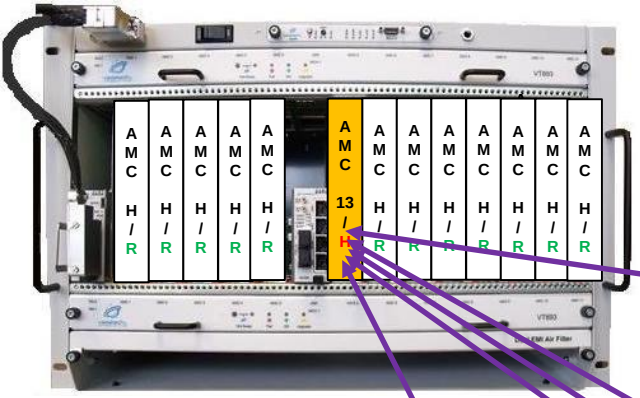
- 122880 ch. if coupling 256 ch. FE ASIC boards (GET/ASAD type - 4 AGET's)

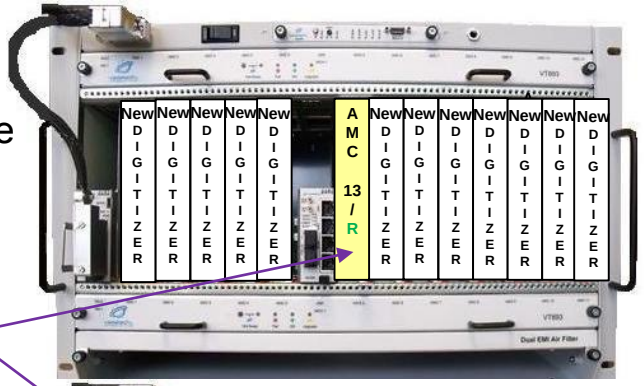
- 491520 ch. if coupling 1024 ch AMC boards (GET/CoBo type – 4x4 AGET's)

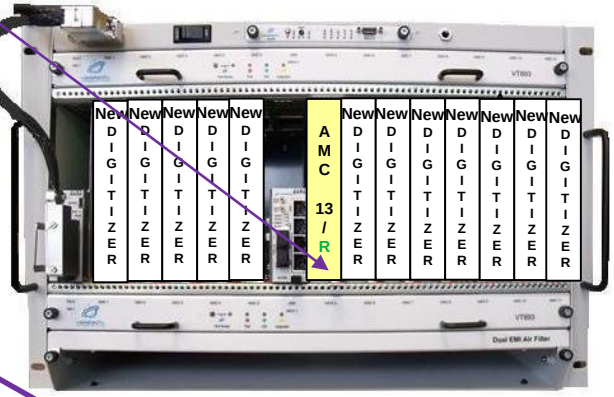
8 – Phase 2

Topology B

Synchronization/Trigger of µTCA.0 (.4) boards that don't have or can't have front panel SFP connection

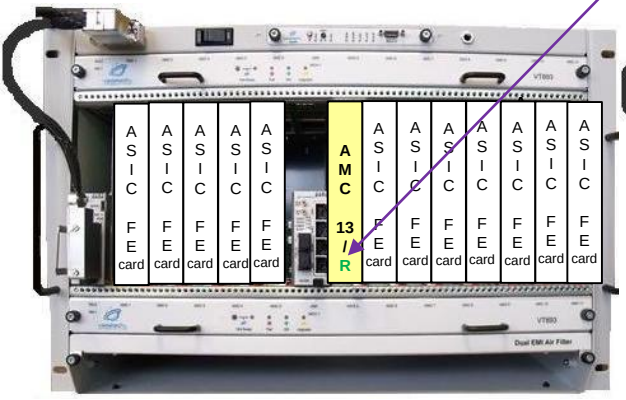


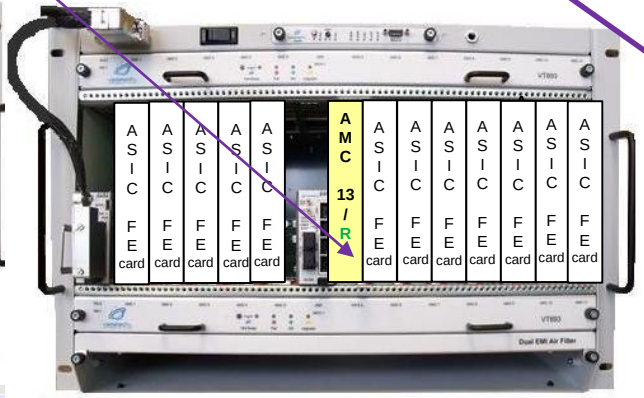




QSFP↔ 4xSFP links (copper or fiber)
Standard 4Gb/s between HUB and Router

AMC 13 is used here as a "backplane" router minimizing cabling to µTCA boards





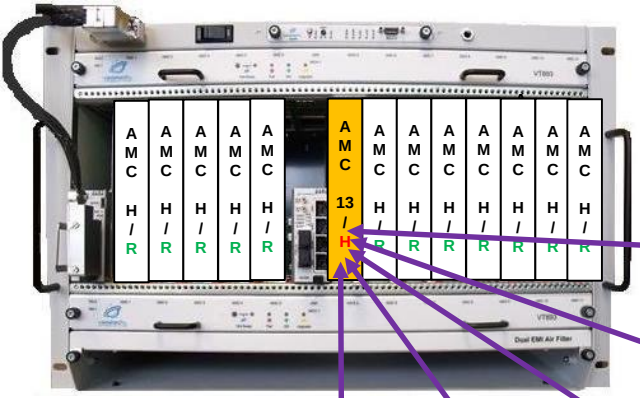
Up to 20 µTCA Shelves (240 boards)

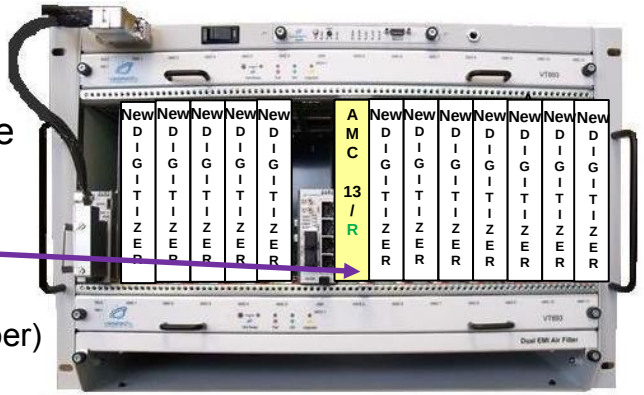
8 – Phase 2
up to topology C

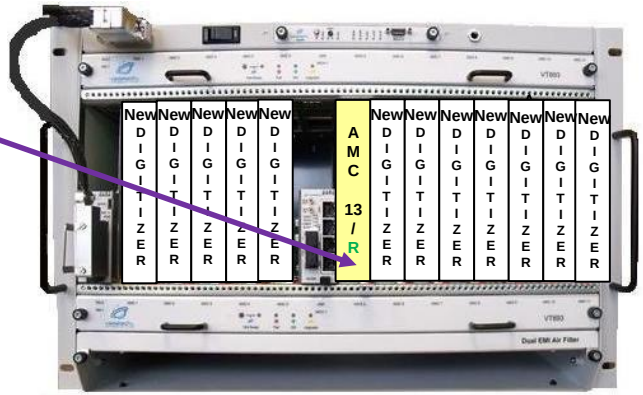
Synchronization/Trigger
of µTCA.0 (.4) boards that don't have
or can't have front panel SFP
connection

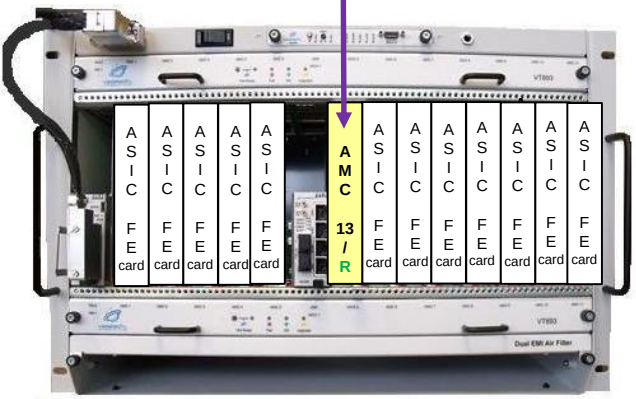
QSFP↔ QSFP links (copper or fiber)
4x4Gb/s by inter-crate cord

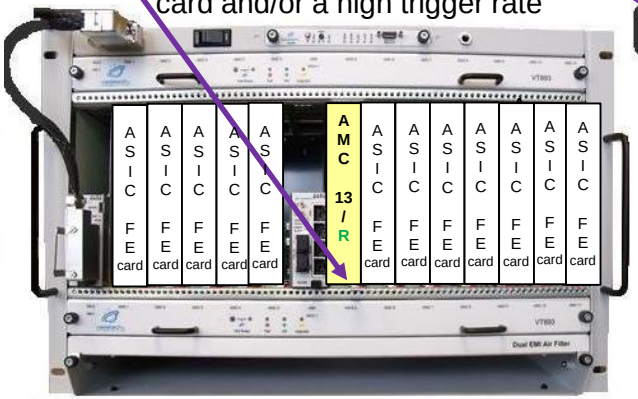
1 link for 3 ASIC FE board
for a high number of channel by
card and/or a high trigger rate

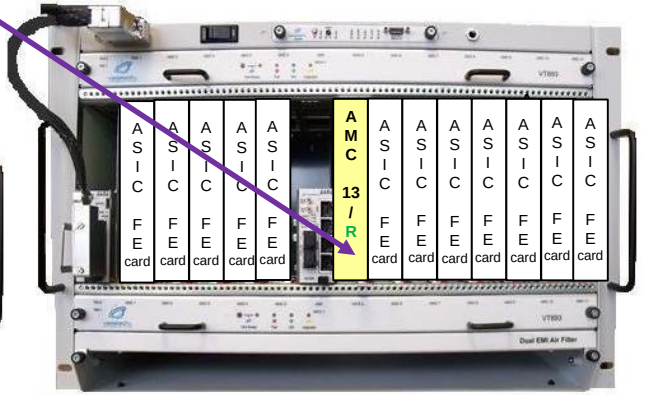




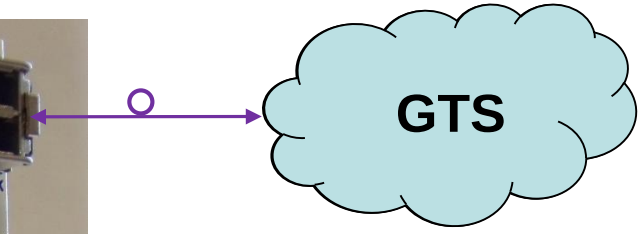








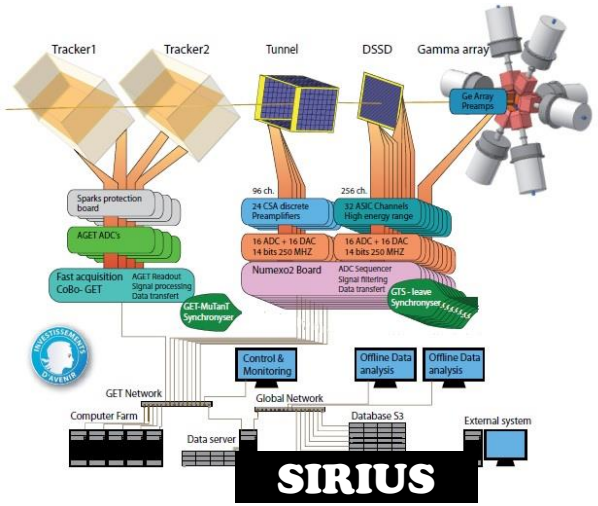
9 – Firmware upgrade of « BEAST » AMC (µTCA™)



Without forgetting our existing data acquisition systems that are CENTRUM coupling based ...

10 – Two examples of possible SMART use in exiting systems

(required hardware & estimated costs)



- (6+16) x 16 ch. NUMEXO2 Digitizer (Tunnel + DSSD)

- 10 x16 ch. NUMEXO2 Digitizer (EXOGAM)

- 1 MUTANT – BEAST (Trackers)

=> 33 Modules to synchronize: 1 HUB + 3 ROUTER (no µTCA shelf required)

Total: 4 x 5000 € = **20000 €**

AGATA
ADVANCED GAMMA TRACKING ARRAY

- based on 45 crystals with one digitizing system by crystal

=> 45 Modules to synchronize: 1 HUB + 3 ROUTER + 1 µTCA shelf (with PM+MCH)

Total: 4 x 5000 € + 10000 € = **30000 €**

- based on 180 crystals with one digitizing system by crystal

=> 180 Modules to synchronize: 1 HUB + 12 ROUTER + 2 µTCA shelves (with PM+MCH)

Total: 13 x 5000 € + 20000 € = **85000 €**

Conclusion

Project scheduling & Key dates:

- December 2018 → Green light from GANIL Committee project for SMART development (Phase 1)

- 2019 → R&D on Zynq based AMC (HUB/ROUTER Triggerless) – Board design (SMART AMC)

- 2020 → Prototype production - SMART concept tests & validation - Phase 1 conclusion

- 2021 → 1st ROUTER production – AMC HUB production or Phase 2 launching with SMART AMC13 R&D

- 2022 → Board design and prototype production (SMART AMC13) – Firmware upgrade (AMC HUB to AMC13 HUB)

- 2023/24 → Full solution tests/validation and HUB production

Thank you for your attention