

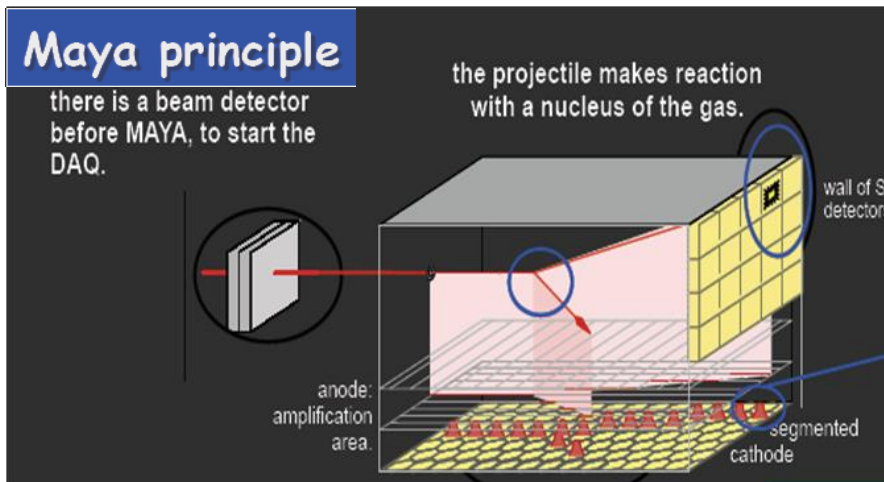


**G**eneral **E**lectronics for **T**ime projection chambers

*Un système basé sur le  $\mu$ TCA<sup>TM</sup>.0  
mais entièrement compatible avec  
le  $\mu$ TCA<sup>TM</sup>.4 ( $\mu$ TCA for Physics)*

# MAYA TPC: 32x32 = 1024 voies

Etat des lieux au GANIL en 2009 ...



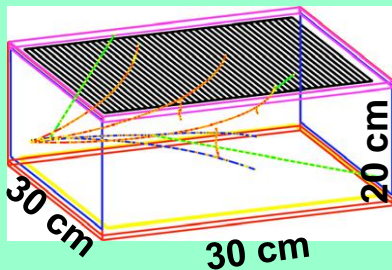
**Système d'acquisition basé sur l'ASIC GASSIPLEX**

- ⇒ Temps mort important (taux de comptage max.  $\approx 100$  Hz)
- ⇒ Faible intégration (16 voies/circuit)
- ⇒ Technologie ancienne (Disponibilité, Quantité?)

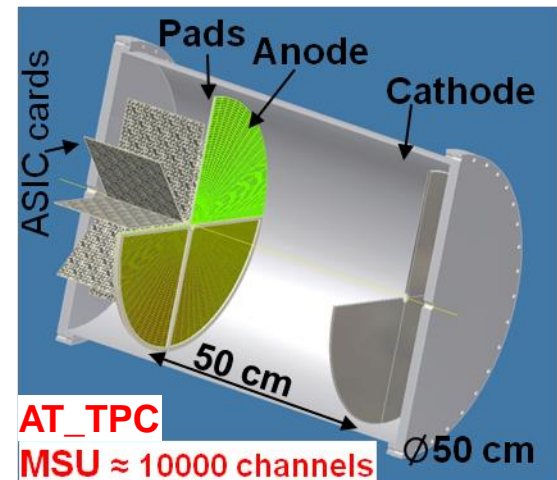
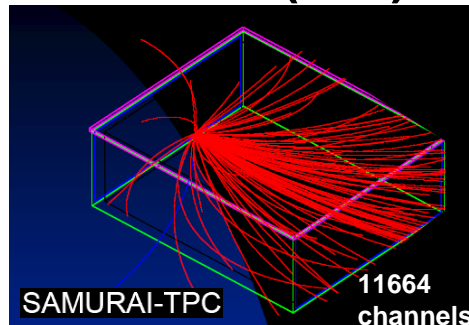
**Ne convient pas aux besoins des nouvelles TPC**

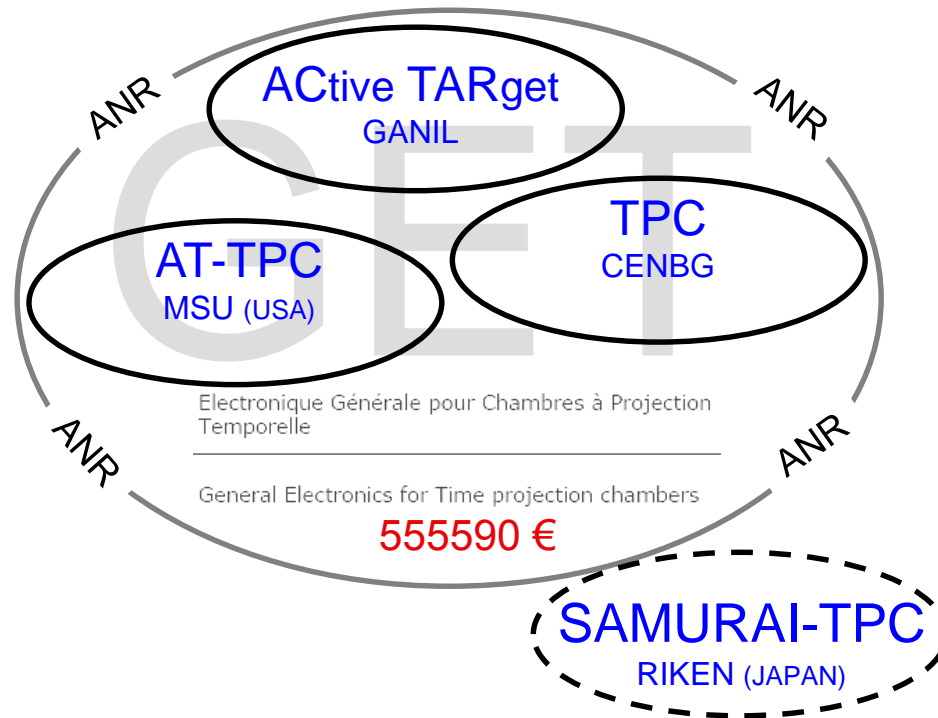
- ➔ Grand nombre de voies (> 5000)
- ➔ + un ordre de grandeur en termes de taux de comptage

**ACTAR\_TPC = 16384 channels @ GANIL**



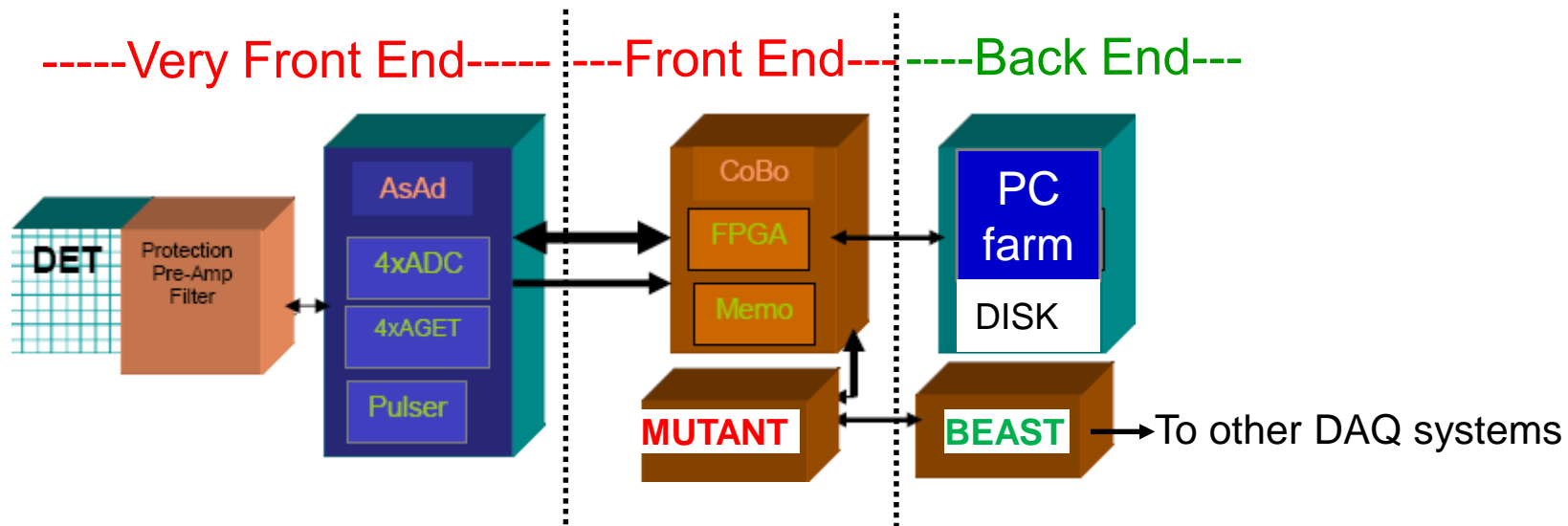
**Demain:  
10000 voies ou plus ...  
@ 1KHz (ICR)**





*collaboration based on an “ANR” grant for the French labs (2009-2014)*

# Reminder of DAQ block diagram



**AGET:** Asic for **GET** – 64 analog channels - 512 cells/channel

IRFU

**ASAD:** ASic and Analog to Digital converter - 4 AGET + 4 ch. ADC

CENBG

**COBO:** COncentration **BO**ard – 4 ASAD - 1024 digital channels

NSCL/MSU

**MUTANT:** **MU**ltiplicity, **TR**igger **AN**d **T**ime ( 3 trigger levels)

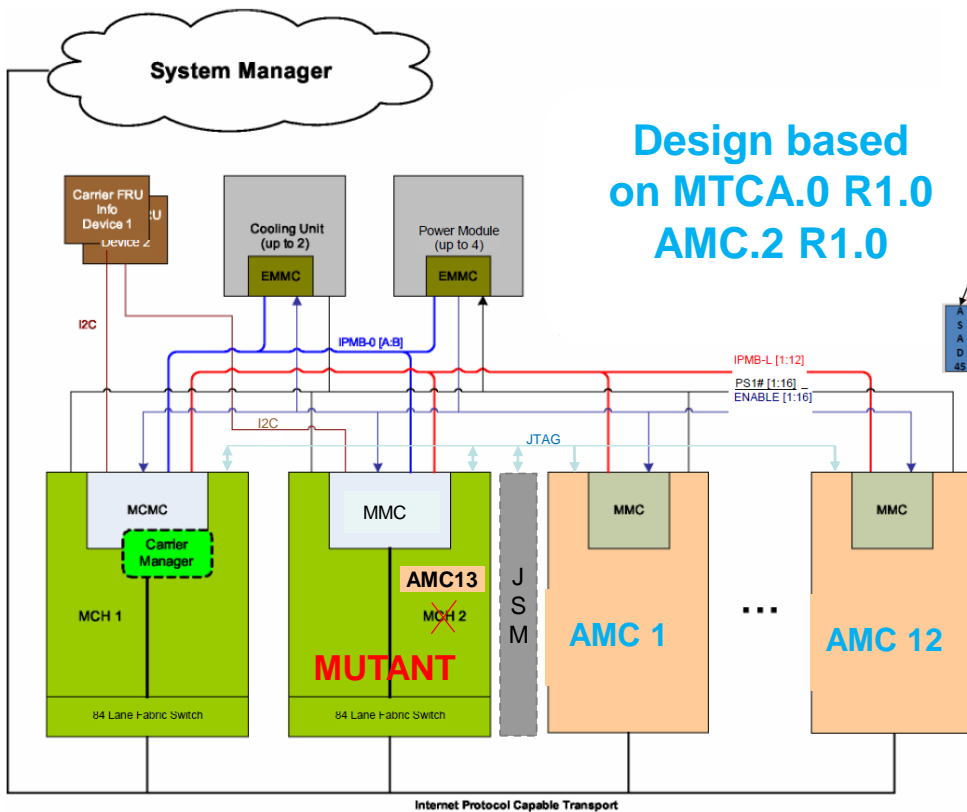


**BEAST:** **B**ack **E**nd **A**daptor for **S**ynchronization by **T**imestamping

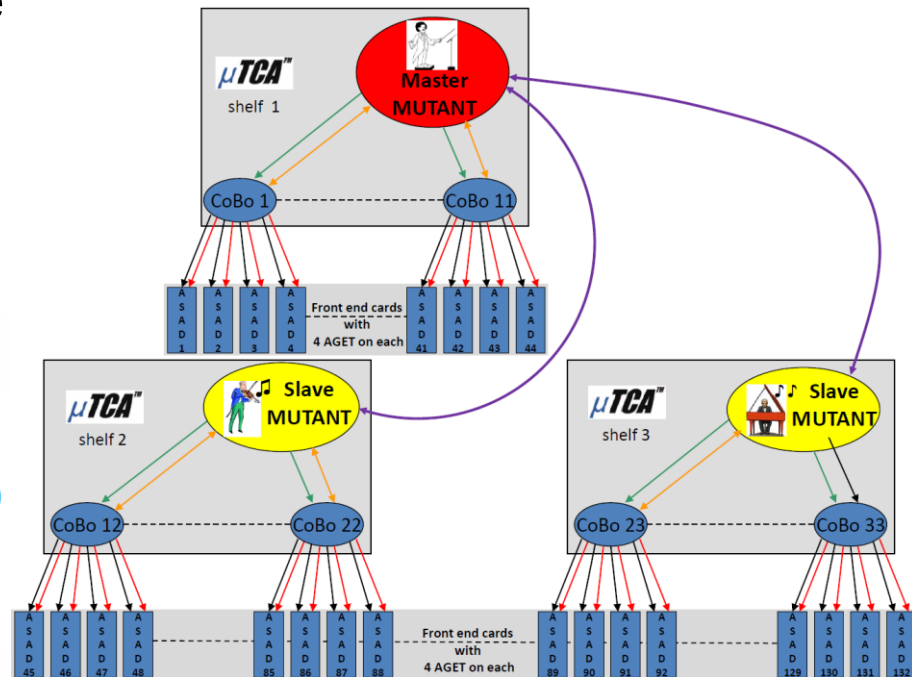




# Short reminder about the global architecture

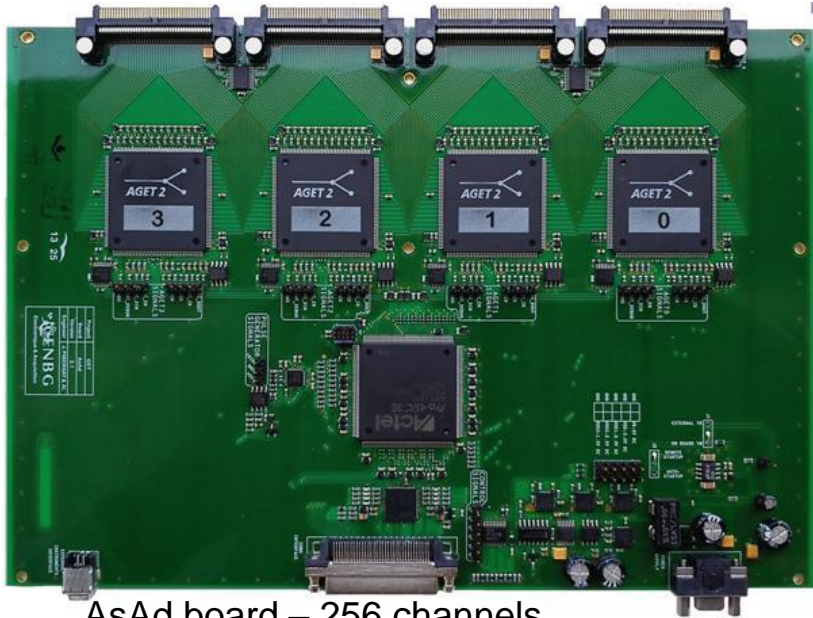


Design based on MTCA.0 R1.0  
AMC.2 R1.0



1024 ch. x 11 slots x 3 shelves = 33792 channels  
↑  
(Vadatech VT893)

# Components of the full GET system



AsAd board – 256 channels  
(4 AGET chips)



CoBo board – 1024 channels  
(managing 4 AsAd boards)



MUTANT module – up to 12288 channels  
(12 CoBo boards / 48 AsAd boards)



## MuTanT

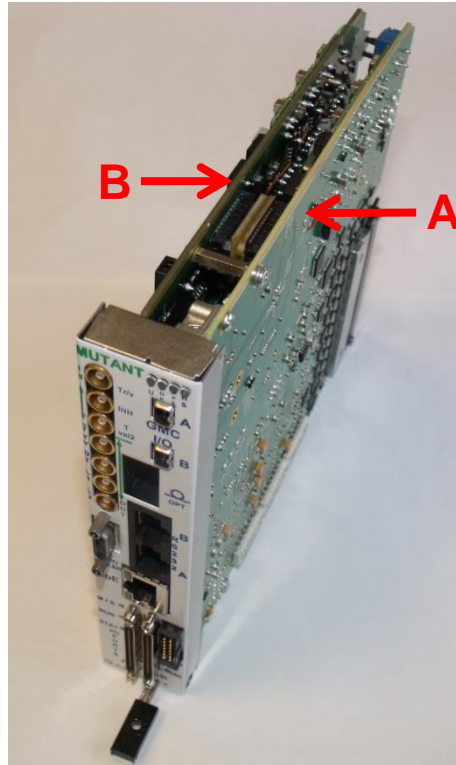
1 module – 2 boards

Multiplicity

Trigger  
(L0,L1,L2)

and Time  
(+ Event Number)

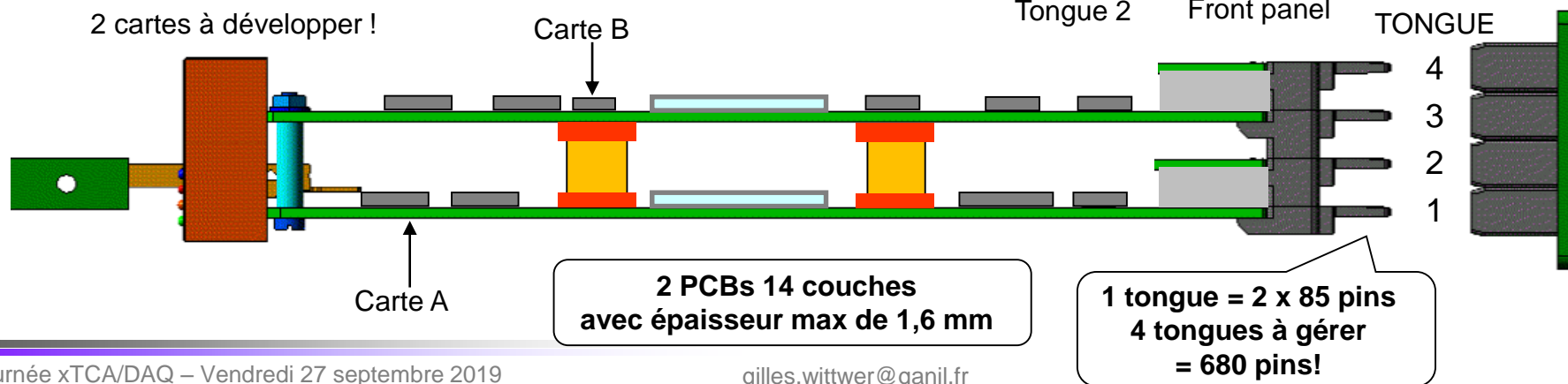
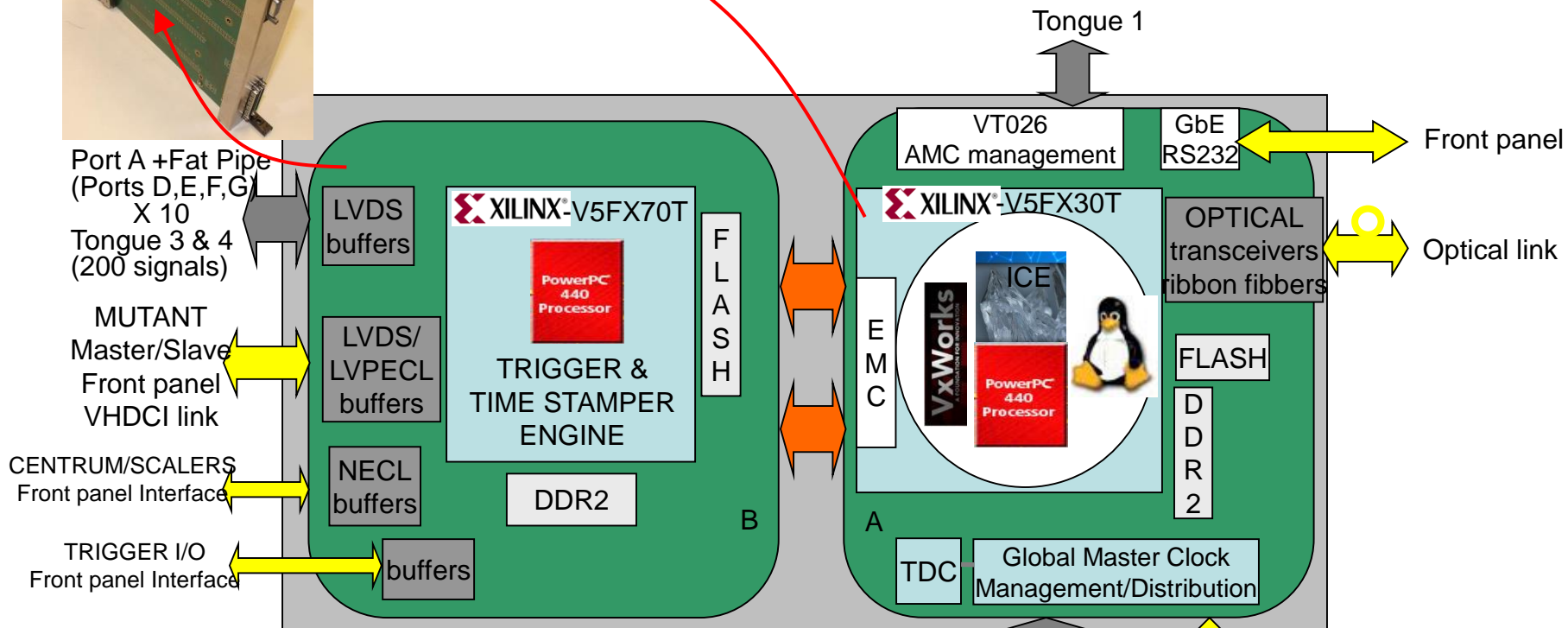
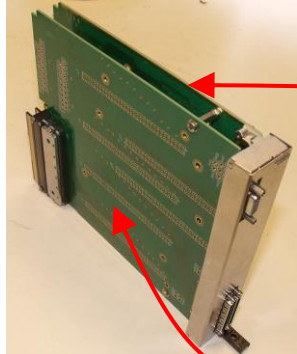
Board B: - Trigger/timestamper engine



Board A: - GMC/WSCA distribution  
- Embedded system (Linux)

- L0: External trigger
- L1: Multiplicity trigger
- L2: Trigger on hit pattern

# Synoptique et assemblage de MUTANT

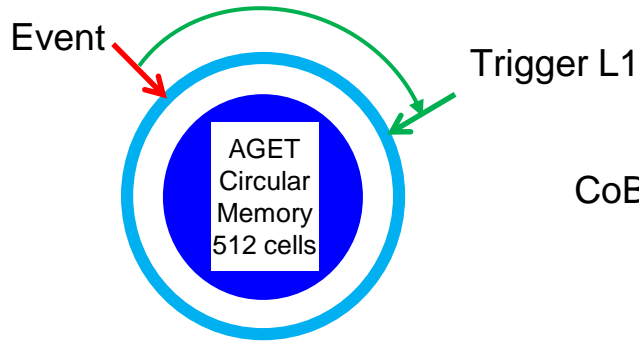




# MUTANT- CoBos data exchanges

## main time values

### Full memory



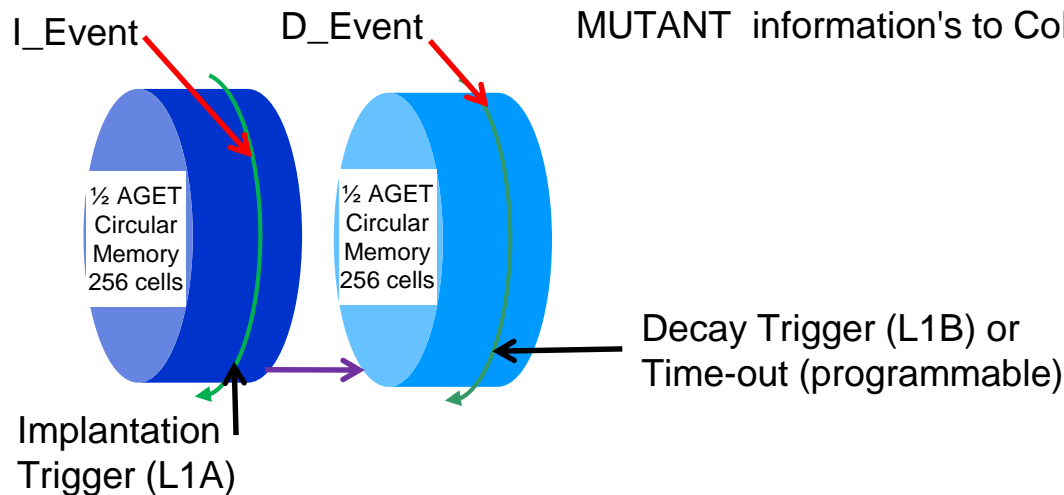
AGET: Sampling Frequency = 1-100 MHz  
 Trigger roundtrip:  $512 \times 10 \text{ ns} = 5.12 \mu\text{s}$   
 to  $512 \times 1 \mu\text{s} = 512 \mu\text{s}$

MUTANT Programmable Delay & Gates are 16 bits wide  
 Attached to GMC (10 ns)

CoBo to MUTANT : L1: new multiplicity value @ 25 MHz max  
 nothing to do @ MUTANT level for lower frequency  
 L2:  $1.3 \mu\text{s}$  to receive the TPC hit pattern (one shelf)  
 $12.8 \mu\text{s}$  for added shelves

MUTANT trigger "OK" to CoBo "STOP": -L0 : 30 ns/655  $\mu\text{s}$  max  
 - L1 : 80 ns /655  $\mu\text{s}$  max  
 - L2 : **depends on the algorithm !**

### 2 x half-memories (2p decay)



MUTANT information's to CoBo: - L2 mask pattern:  $1.3 \mu\text{s}$   
 - Time stamp + Event Number: 120 ns  
 - Time stamp only: 80 ns

# Summary of what to do to be compatible with MUTANT

- 1) In terms of clock/clock\_enable networks (M-LVDS electrical standard)

MUTANT distributes a 100 MHz clock to every CoBo of each crate, phase aligned (skew < 1ns - TDC) ⇒ **μTCA-CLK1**

MUTANT distributes a synchronous start/stop sampling (phase aligned) ⇒ **μTCA-CLK2**

- 2) In terms of hardware data transfers (LVDS electrical standard)

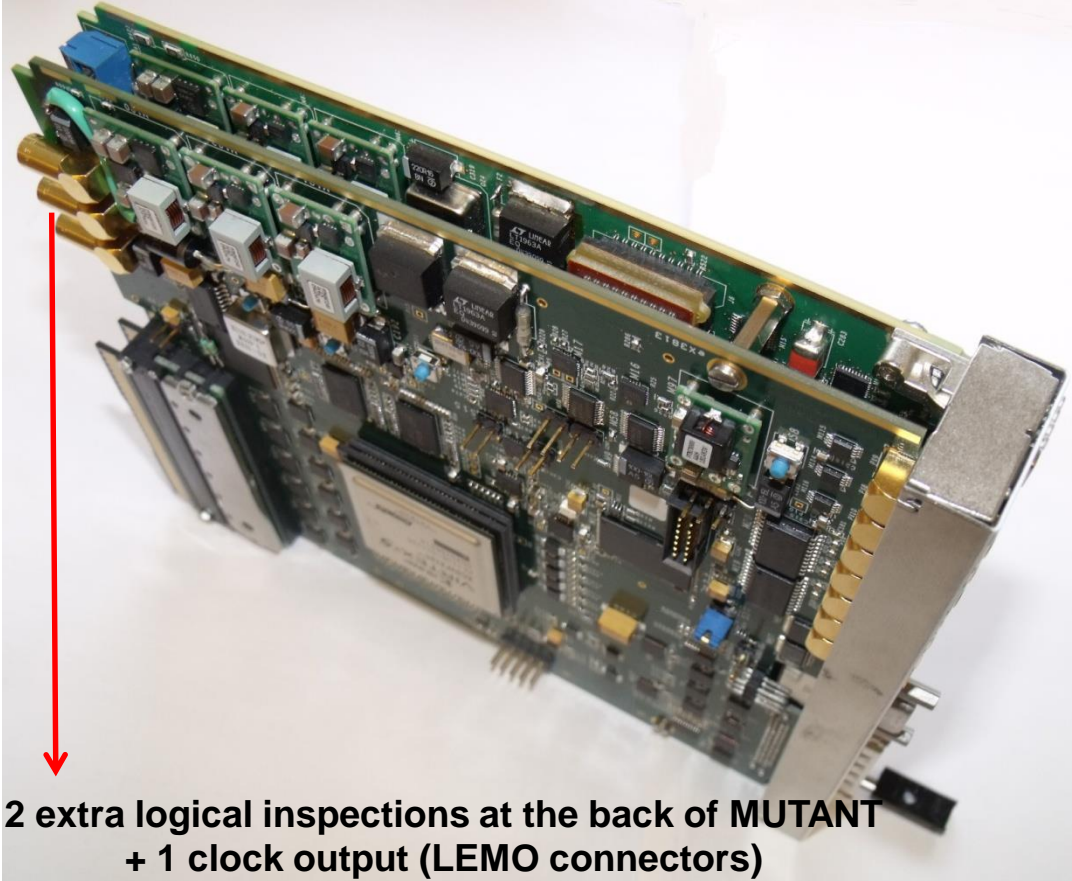
MUTANT exchanges data with the CoBo @ 800 Mbit/s  
⇒ 5 μTCA ports (TX/RX)

- 1 tx bit clock + 4 tx data (DDR)
- 1 rx bit clock + 4 rx data (DDR)

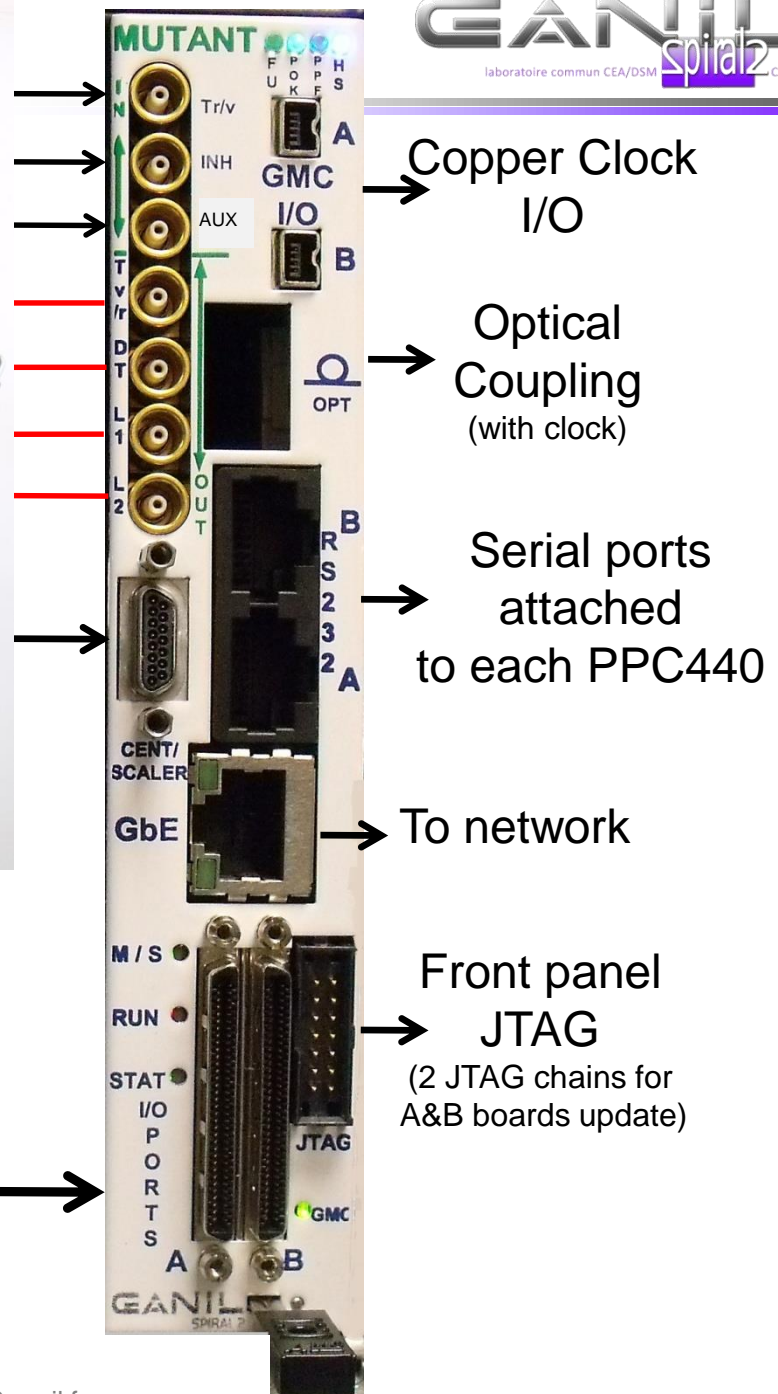
- 3) In terms of communication protocol

- Multiplicity received every 40 ns from CoBo's
- Event Number and Timestamp transmitted to all CoBo's in 120 ns





**2 extra logical inspections at the back of MUTANT  
+ 1 clock output (LEMO connectors)**

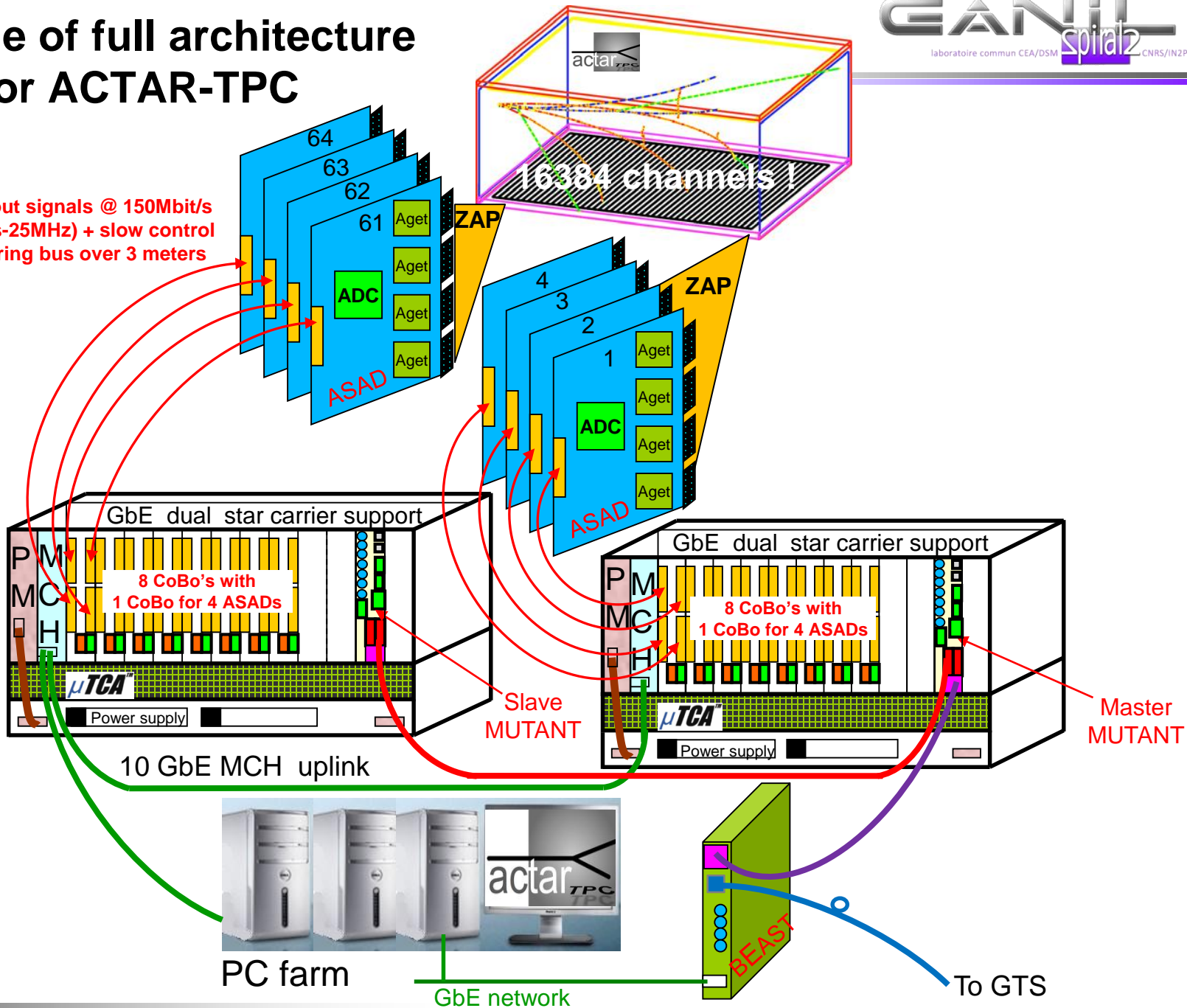


**Inter shelves connection** →  
(between Master MUTANT et slave MUTANT)

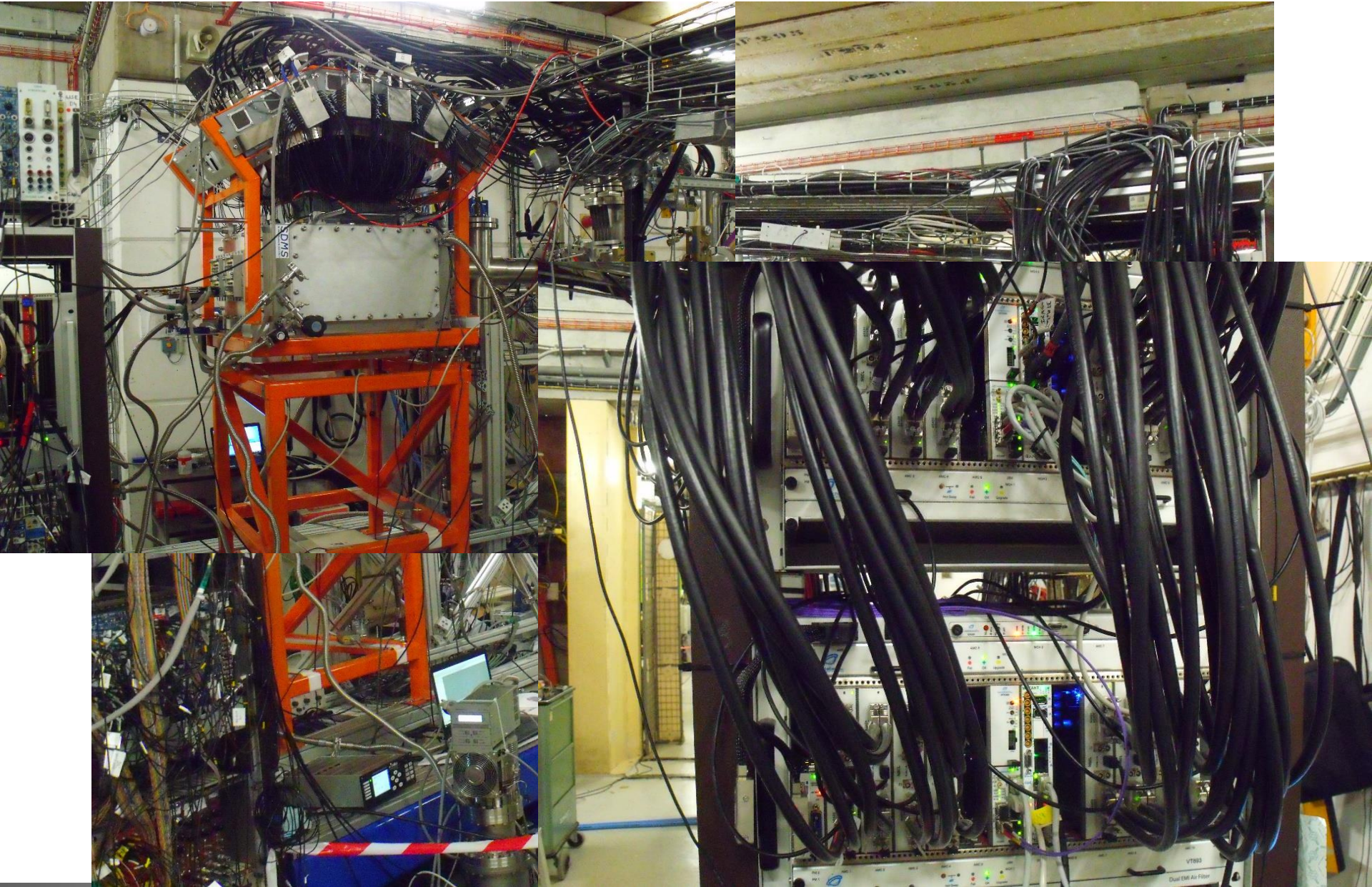
# Example of full architecture for ACTAR-TPC

Very Front End  
Front End  
Back End

LVDS readout signals @ 150Mbit/s  
(ADC 12bits-25MHz) + slow control  
and monitoring bus over 3 meters



# Campagne 2019 -- ACTAR-TPC en salle D6





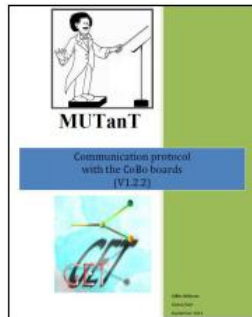
# Conclusion

- Un grand projet (>7 ans) pour notre groupe, à tous les niveaux (technique, social, ...)
  - Appréhension complète d'un nouveau standard et des systèmes embarqués
  - Renouvellement important de nos bibliothèques CAO/Cadence
- MUTANT - Première production en 2015 avec 15 modules construits et tous vendus
  - Un second et dernier lot de 20 modules produit en 2016 pour GANIL et les laboratoires extérieurs (≈ 20 projets dans 15 laboratoires)
  - Valorisation avec bénéfice de 130 k€ pour GANIL
- Le choix du  $\mu$ TCA.0 parfois mal compris en 2009, aujourd'hui bien ancré dans les labs IN2P3 et les projets pour plusieurs raisons:
  - Arrivée du  $\mu$ TCA.4 ( $\mu$ TCA for Physics - 2011)
  - Recommandation IN2P3/IRFU (Journées de perspectives - Février 2012)
  - Obsolescence définitive des bus // (VME/VXI ...)
  - ...



|  |                              |
|--|------------------------------|
|  | Caen, Saclay, Bordeaux       |
|  | Michigan, Texas, Indiana     |
|  | Catania, Legnaro             |
|  | Riken, JPARC                 |
|  | Daejeon                      |
|  | Leuven                       |
|  | Shanghai, Hong Kong, Lanzhou |

- Un système de documentation complet pour les utilisateurs avec des formations adaptées et un support.



**Le groupe DELTA continue avec BEAST aujourd'hui et surtout propose SMART pour demain ...**

**Merci de votre attention.**