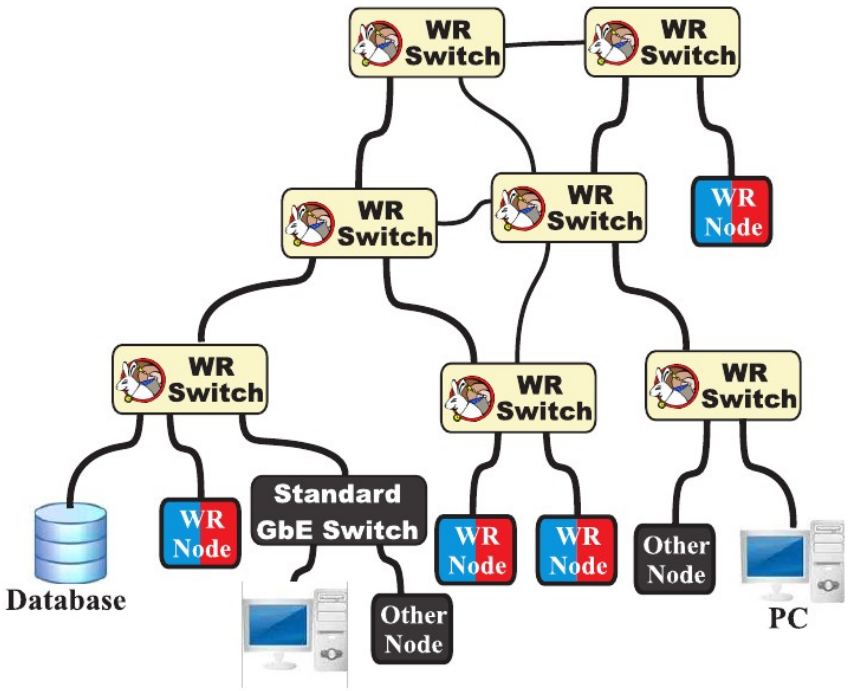
- White Rabbit :
  - Theory
  - DAQGEN implementation
  - Debug tool
  - Test system

White Rabbit principle : main features



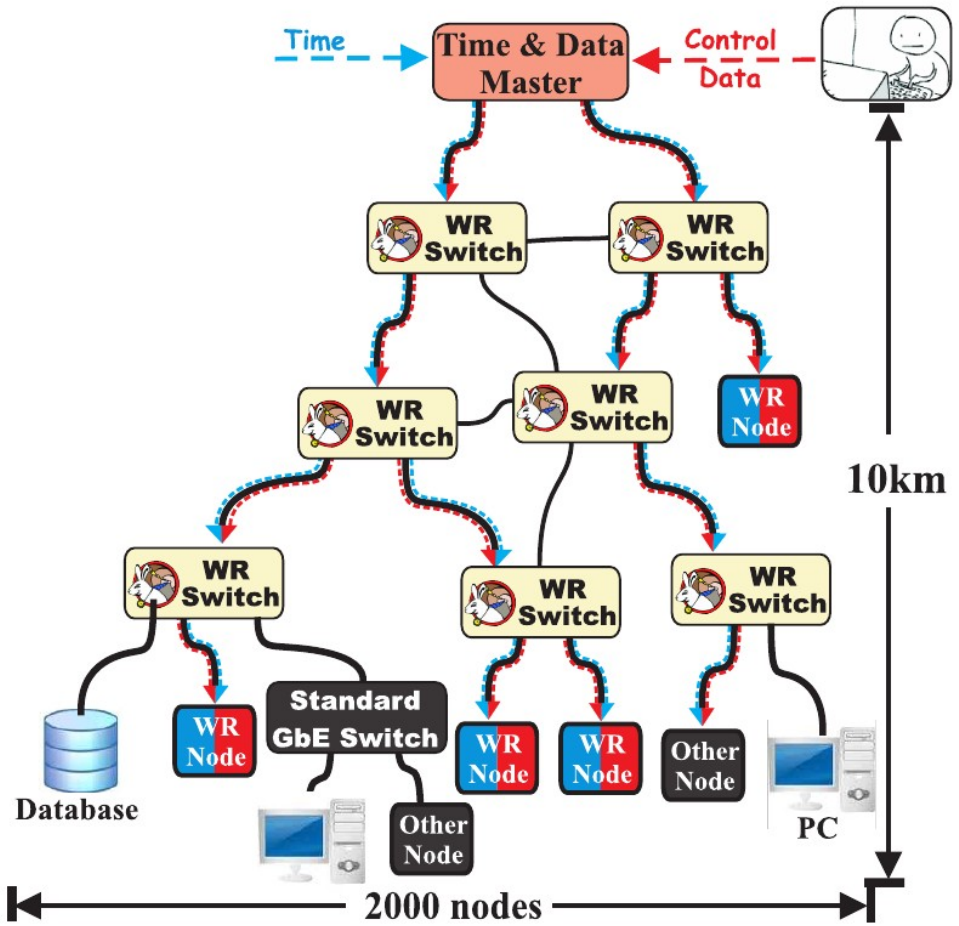
- Main Features
  - Tranparent, High-accuracy synchronisation
  - Low-latency, deterministic data delivery
  - Designed for high reliability
  - Few thousands nodes
  - Copper or fiber medium
  - Up to 125Km fiber links
  - Bandwidth : 1 Gbps
  - WR switch : 18 ports
  - Non WR Devices
  - Ethernet features (VLAN) & Protocols (SNMP)
- Open hardware & Firmware

White Rabbit principle: Enhanced Ethernet

- An extension of Ethernet which provides :
  - Synhronous mode (Syn-E) – common clock for physical layer in entire network, allowing for precise time and frequency transfer
  - Determinisc routing latency – a garente that packet transmission delay between two stations will never exceed a certain bondary

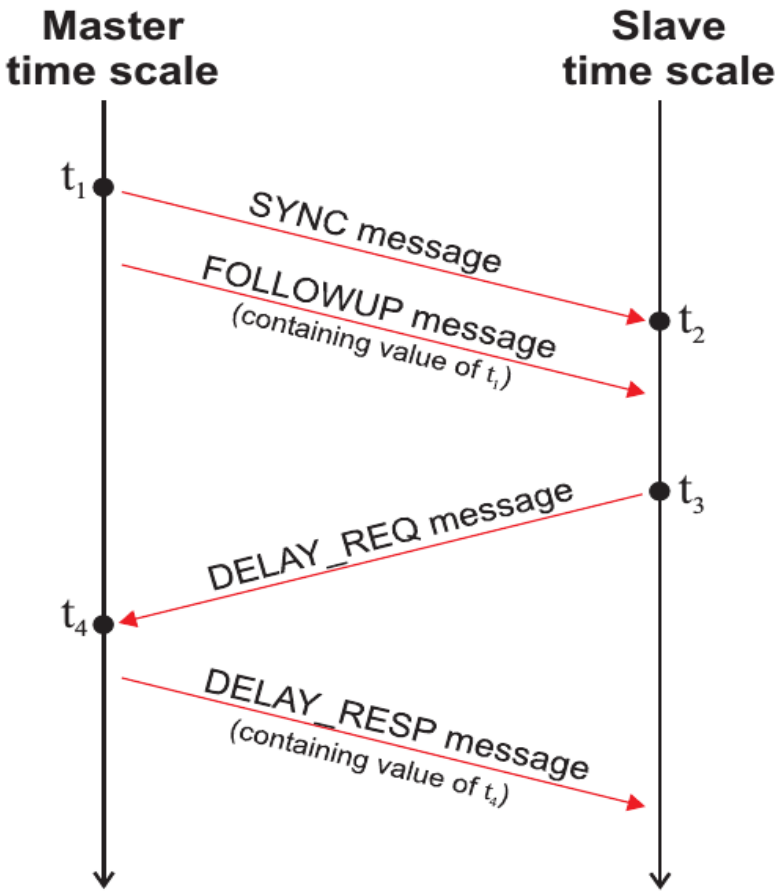
- Technology overview
  - Precision Time Protocole (IEEE1588)
  - Synchronous Ethernet
  - DMTD Phase tracking (Digital ….

White Rabbit - enhanced Ethernet



- Two separate services (enhancements to Ethernet) provided by WR
  - High accuracy/ precision synchronisation
  - Deterministic, reliable and low latency Control data delivery
- Sub-ns accuracy and sub-ps precision combination of :
  - Precision Time Protocol (IEEE1588).
  - Synchronous Ethernet.
  - DMTD phase tracking.
- Low latency
  - 7th Class of service (priority)
- Control data send in control message
  - High Priority HP
- Reliability
  - Forward Error correction

Precision Time Protocol (IEEE1588)



- White Rabbit (surcouche PTP a modifier)
- Packet-based synchronization protocol
- Synchronizes local clock with the master clock
- Link delay evaluated by measuring and exchanging packets tx/rx timestamps

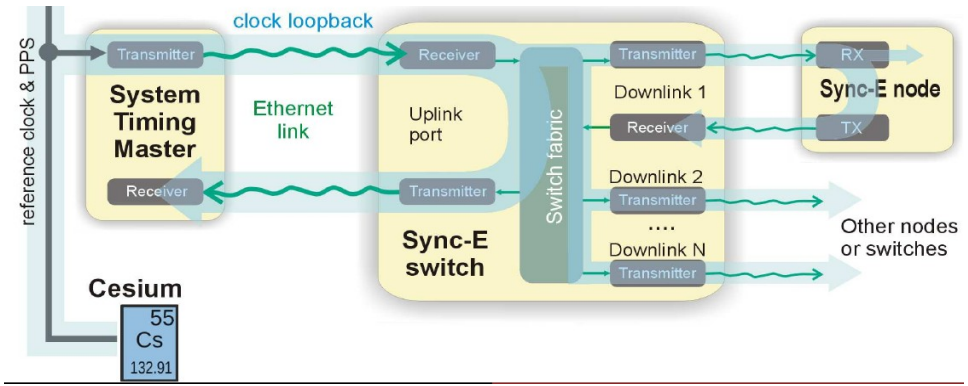
Having values of t1 ...t4 , slave can:

- calculate one-way link delay:

  $\delta ms = ((t4 - t1) - (t3 - t2))/2$

- syntonize its clock rate with the master by tracking the value of
  t2 − t1
- compute clock offset:
  offset = t2 − t1 + δms

Synchronous Ethernet

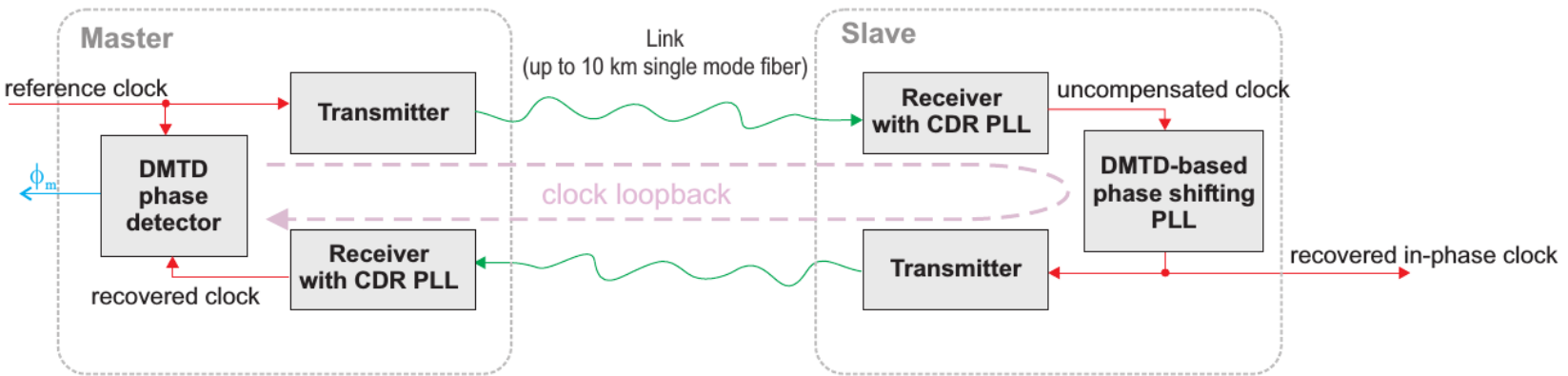


- All network nodes use the same physical layer clock,
- Generated by the System Timing Master.
- PTP is used only for compensating clock offset.
- Having the same clock frequency everywhere enables
- Phase detector technology as the means of measuring time.

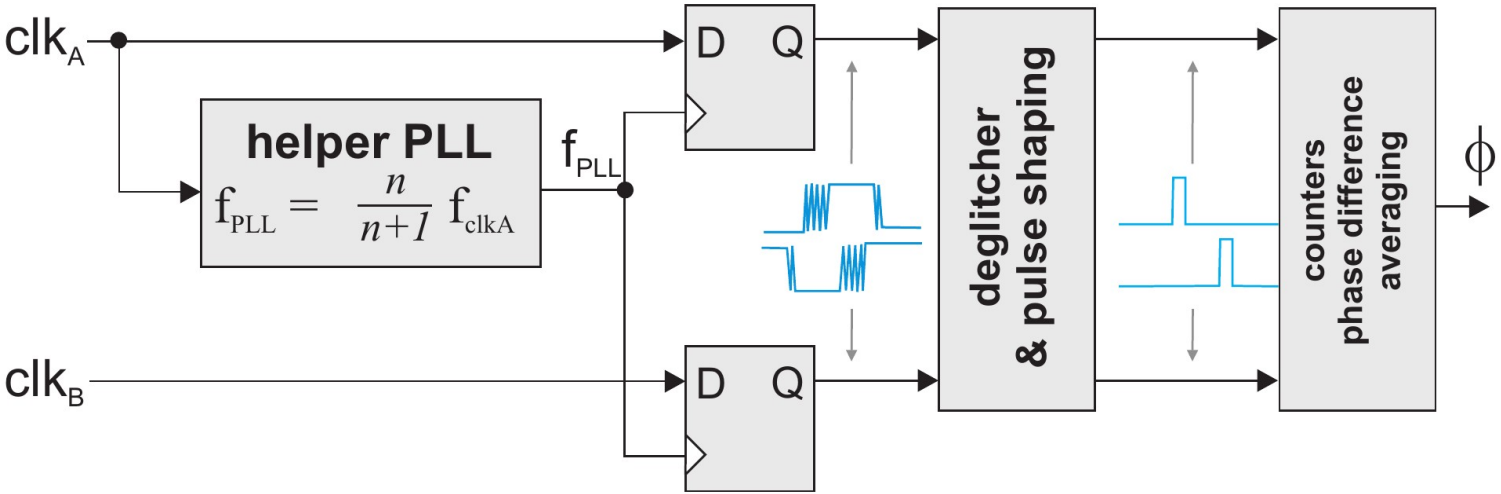
DDMTD : Phase tracking

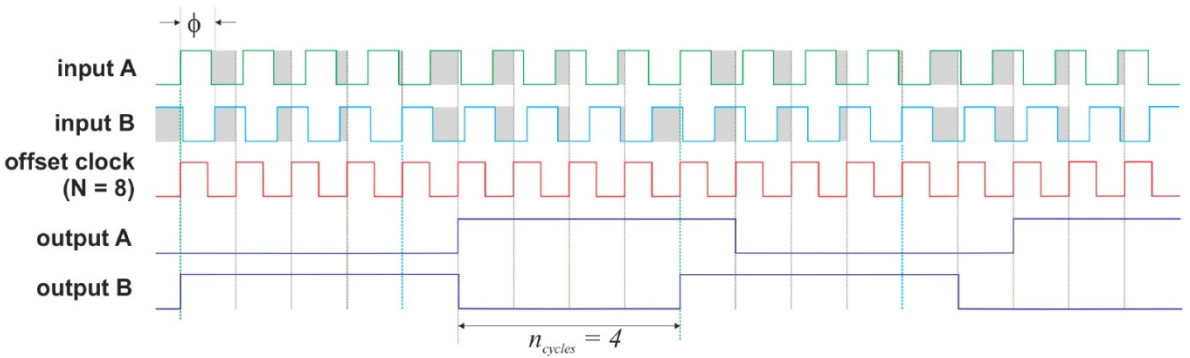
- PTP limitations :
  - timestamping granularity
  - All node have free-runing oscillators
- Solution : take advantage of SyncE and measure phase shift

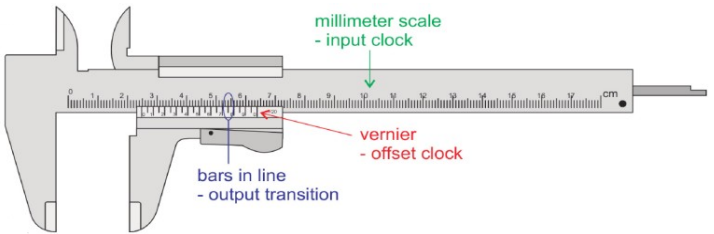
- Measure the phase shift between transmit and receive clock on
- the master side, taking the advantage of Synchronous Ethernet.
- Monitor phase of bounced-back clock continuously.
- Phase-locked loop in the slave follows the phase changes
- Measured by the master.



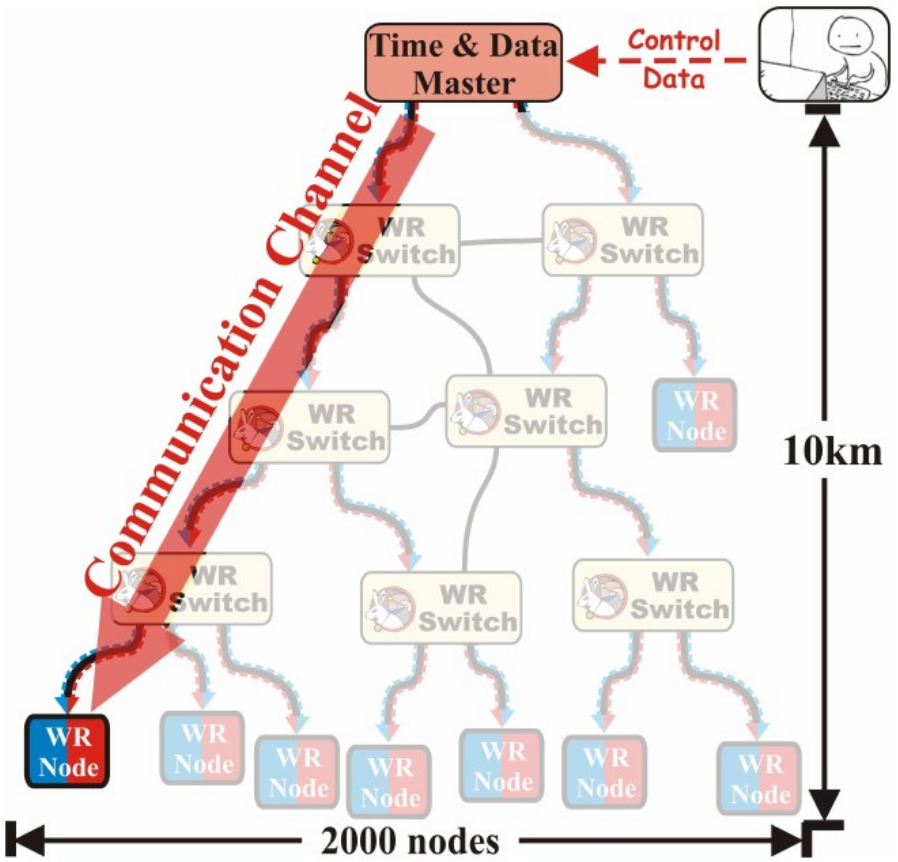
Digital Dual Mixer Time Domaine phase detector





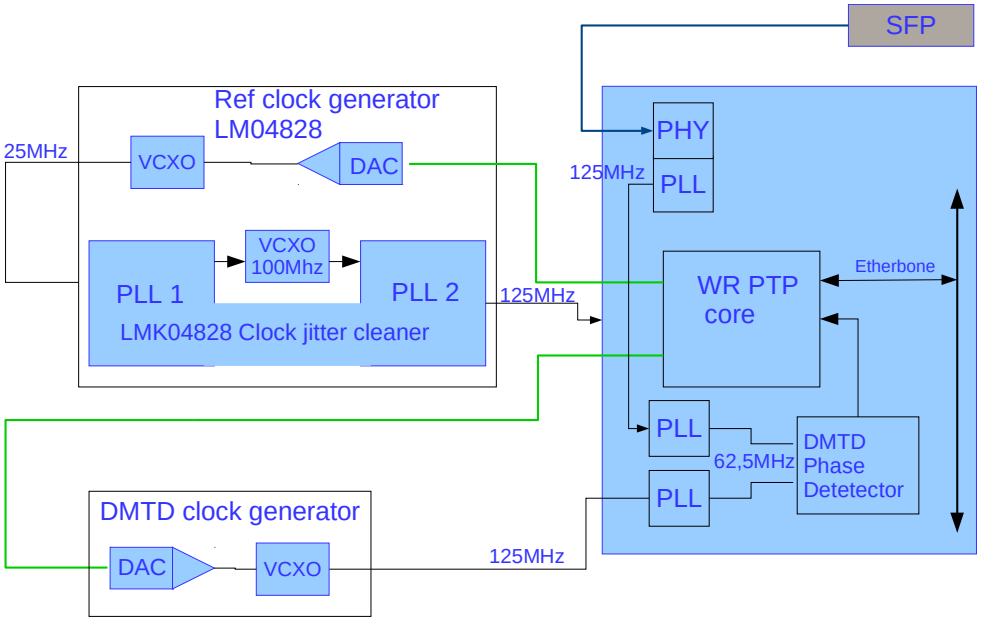


Control Data & Data redundancy



- Two type of data
  - Control data (high priority)
  - Standard data
- Characteristics of Control Data
  - Send in control messages
  - Send by master
  - Broadcast
  - Deterministic and low latency
  - Reliable delivery
- Data redundancy
  - Forward error correction – additional transparent layer :
    - One control message encoded into N Ethernet frames
    - Recovery of Control message from any M (M<N)

WhiteRabbit : DAQGEN implementation

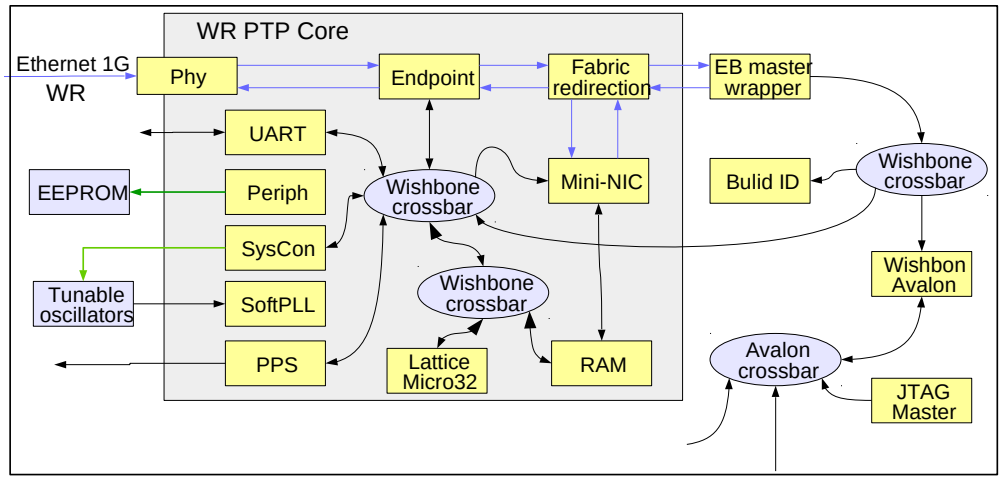


The WhiteRabbit IDROGEN hardware is base on CERN open hardware with Enhancements

- Based on LMK4828 synthesiser
  - Ultra low noise clock jitter Cleaner with Dual Loop PLL
  - 90fs RMS jitter.
- DDMTD internal of FPGA (placement with constraint)
- Two generated local clock :
  - DDMTD source (comparison between WR master clok from SFP)
  - PLL source with phase adjustment
- **IDROGEN Enhancements**
  - PLL selection
  - VCXO Frequency
  - Input frequency for DDMTD
    - remove of internal PLL (future dev.)
  - Tx/Rx routing equalisation

http://www.ohwr.org/projects/white-rabbit/wiki/WRReferenceDesign

Firmware White Rabbit



- All numerical module fully included in FPGA
- Fully coded in VHDL (including phy)
- Based on Lattice-Micro32 µ-controler (writing in VHDL code)
- Communication to FPGA core with Wishbone interface.
- Interface Wishbone to Avalon (LAL/Obs. development)
- Open firmware
  - At the origin developed for Xilinx.
  - Development for ALTERA
    - ARRIA2 & 5 GSI (recently 10)
    - ARRIA 10 Nancay/LAL
- System clock 62.5Mhz
  - future development 125Mhz

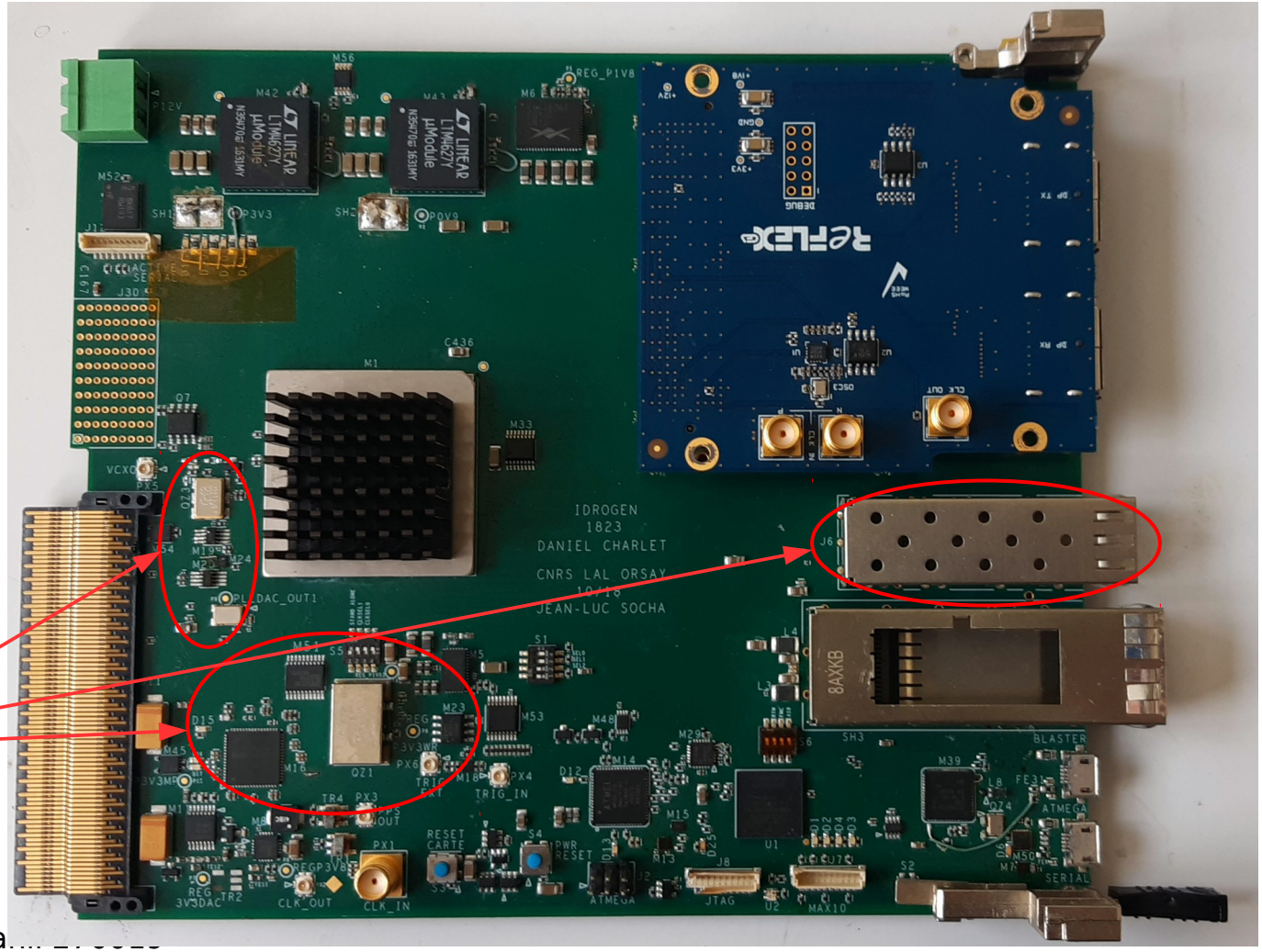
WhiteRabbit debugg core mini-com

```
WR PTP Core Sync Monitor v 1.0
Esc = exit

TAI Time:                    Thu, Jan 1, 1970, 00:03:48

wru1: Link up   (RX: 685, TX: 281), mode: WR Slave   Locked  Calibrated
IPv4: BOOTP running

PTP status: slave

Synchronization status:

Servo state:                 TRACK_PHASE
Phase tracking:              ON
Synchronization source:
Aux clock status:

Timing parameters:

Round-trip time (mu):     691831 ps
Master-slave delay:       349132 ps
Master PHY delays:        TX: 46407 ps, RX: 168643 ps
Slave PHY delays:         TX: 46407 ps, RX: 175043 ps
Total link asymmetry:        -6433 ps
Cable rtt delay:          255331 ps
Clock offset:                 0 ps
Phase setpoint:             528 ps
Skew:                         5 ps
Manual phase adjustment:      0 ps
Update counter:             174
--
```

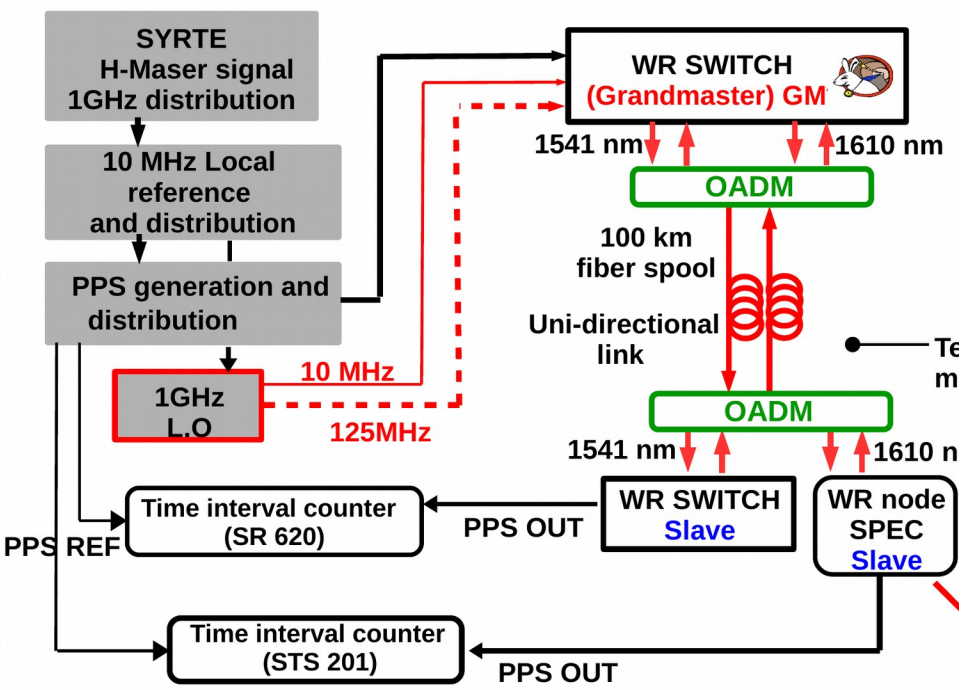
For debugging we use the core mini-com include in the WR core

- Small operating system provided by WR open core
- Serial communication performed by USB in front pannel (IDROGEN enhancement)
  - Status of the link : Delay, phase, transceivers…..
  - Control of the link : Reset, ...

Layout of WR on IDROGEN board



WhiteRabbit, SYRTE test sytem



For the test we use the test system developed by the SYRTE for timing distribution measurement.

- fs measurement capability
- Very high timing stability 10e-16
- WR switch improvement.
  - Remove of local PLL
- Conditioned room.
- Dedicated measuring apparatus
- Selection of fiber length
- Selection of transceivers

For more information

- **White Rabbit and online docs**:
  - Materials: presentations, papers, demos, training material, test reports
  - List of White Rabbit users and companies
  - Components: switch and node
- The White Rabbit Project on Wikipedia
- Selected White Rabbit documents, referenced in the revised IEEE1588 standard
- https://white-rabbit.web.cern.ch/

- Daqgen
  - Hadware shematic & brd
  - Firmware
  - Software
  - https://gitlab.in2p3.fr/DAQGEN