
- DAQGEN, overview of the architecture
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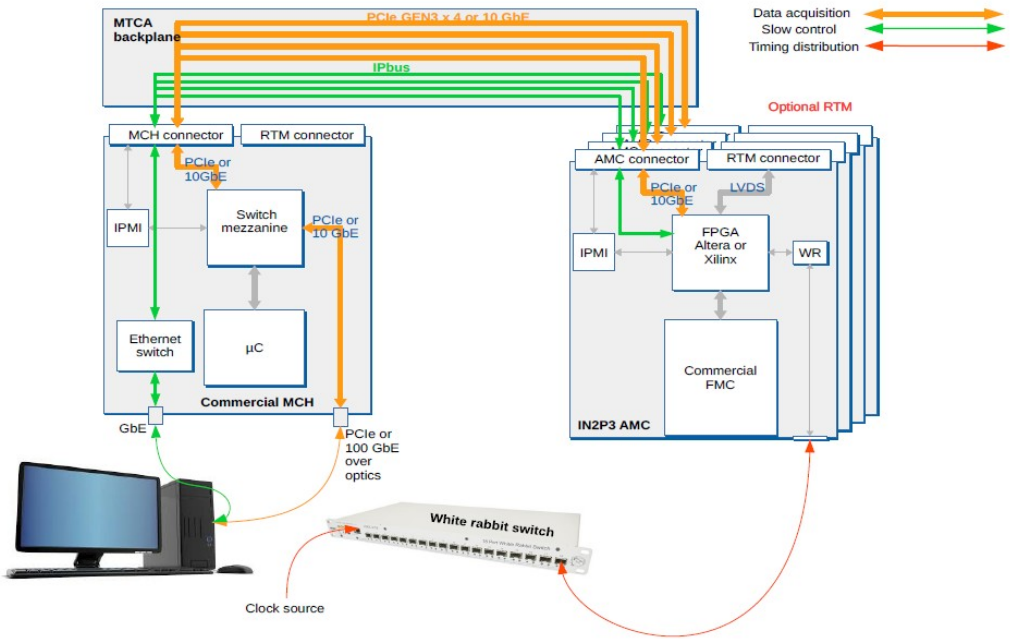
    - Overall Synoptic
    - Clock trees
    - Components configuration
    - Hardware status
  - Firmware
    - Firmware status
- Documentation
- Mezzanine ADC

# ARCHITECTURE



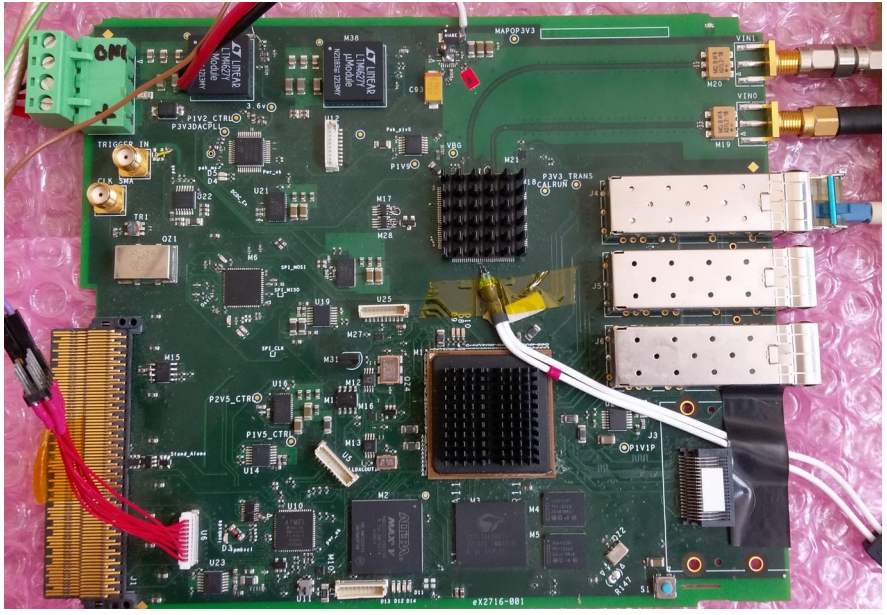

- Standard : xTCA for Physics
- Based on on the shelf material
- Crate controler : MCH from N.A.T
- Data read-out on Backplane :
  - PCIe 4x Gen3 ou Eth10G.
- Crate data transfer :
  - Eth100G (industrial N.A.T)
  - PCIe-over cable (industrial N.A.T)
- Point to point Data read-out
  - 2x10GbE
  - 40GbE (future development)
- Board configuration : IPbus

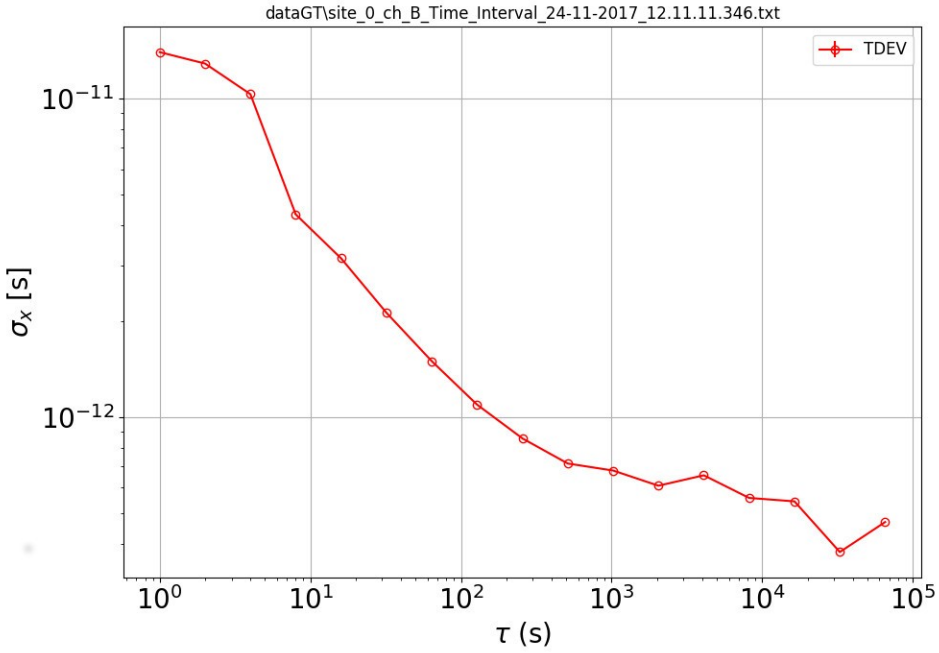
# Historique de la carte IDROGEN

La carte est issue de development de différents laboratoire de l' IN2P3 :

- USB-blaster II : carte PCIe40 ( CPPM Marseilles)
- IPMI : LPSC Grenoble
- Ipbus: LPSC Grenoble
- WhiteRabbit module: carte Nebula (LAL Observatoire de Paris).
- Bibliothèque Cadence IN2P3: IPHC Strasbourg

# History

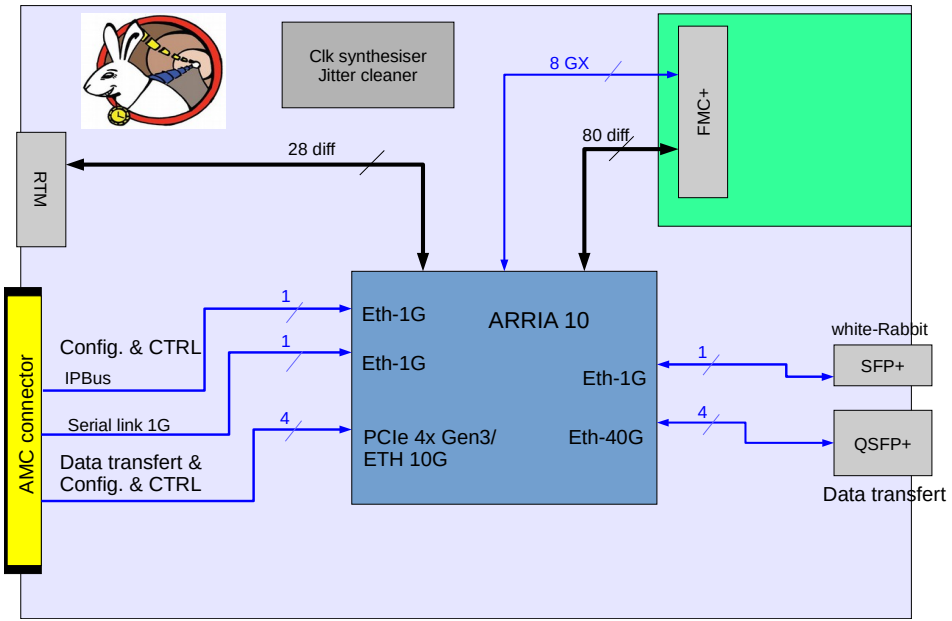





- Derived from Nebula board
  - White rabbit module
  - Power supply tree

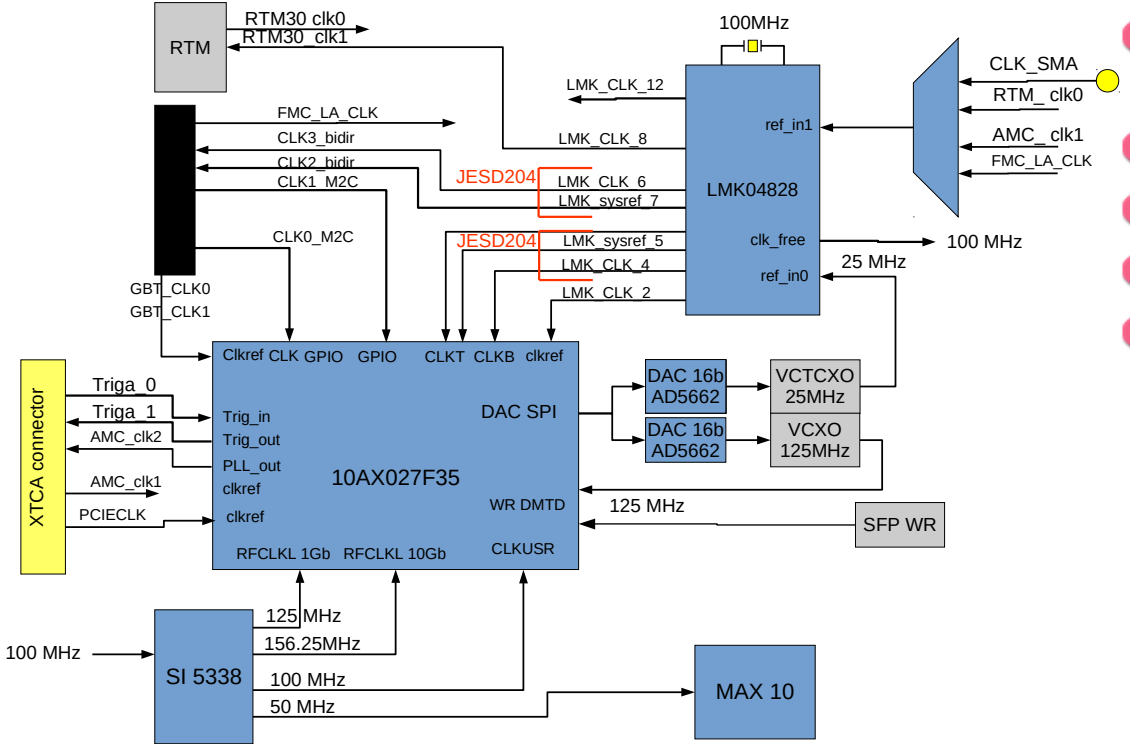
- In collaboration with the laboratory SYRTE (Obs Paris INSU).
- 400 fs after 1000 s and 1 km fibre

# IDROGEN board main feature



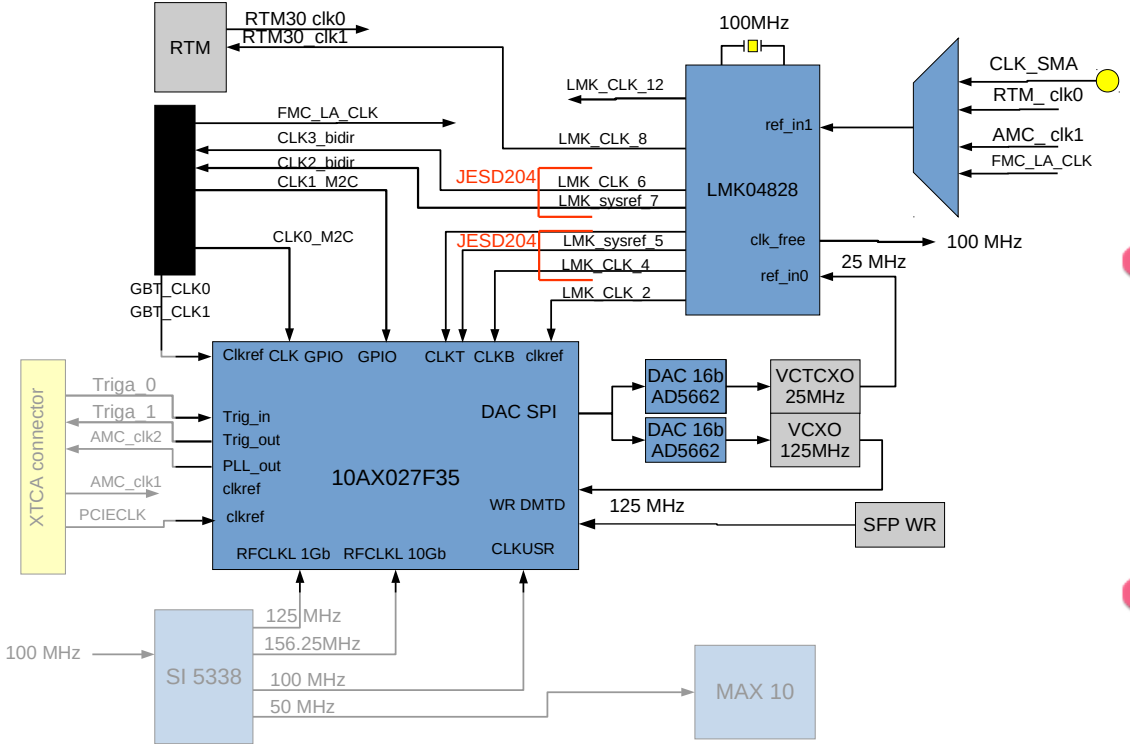

- MTCA 4.0 standard, Double-width, full size AMC.
- FPGA : 10GX027H4F34
- Stand alone mode (power 12v)
- VITA57.1 (FMC) slot.
  - 160 single-ended I/Os (80 LVDS) and/or up to 10 serial transceivers in a 40 x 10 configuration
- White Rabbit compliant.
- Front panel connectivity :
  - WR SFP+
  - QSFP+ 40G, USB
- Backplane connectivity :
  - 1Gbe IPbus,PCI 4x Gen3,
  - IPMB, CLK & trigger lane.
  - RTM connector : J30.
- Low cost

# Clock tree: main features 1



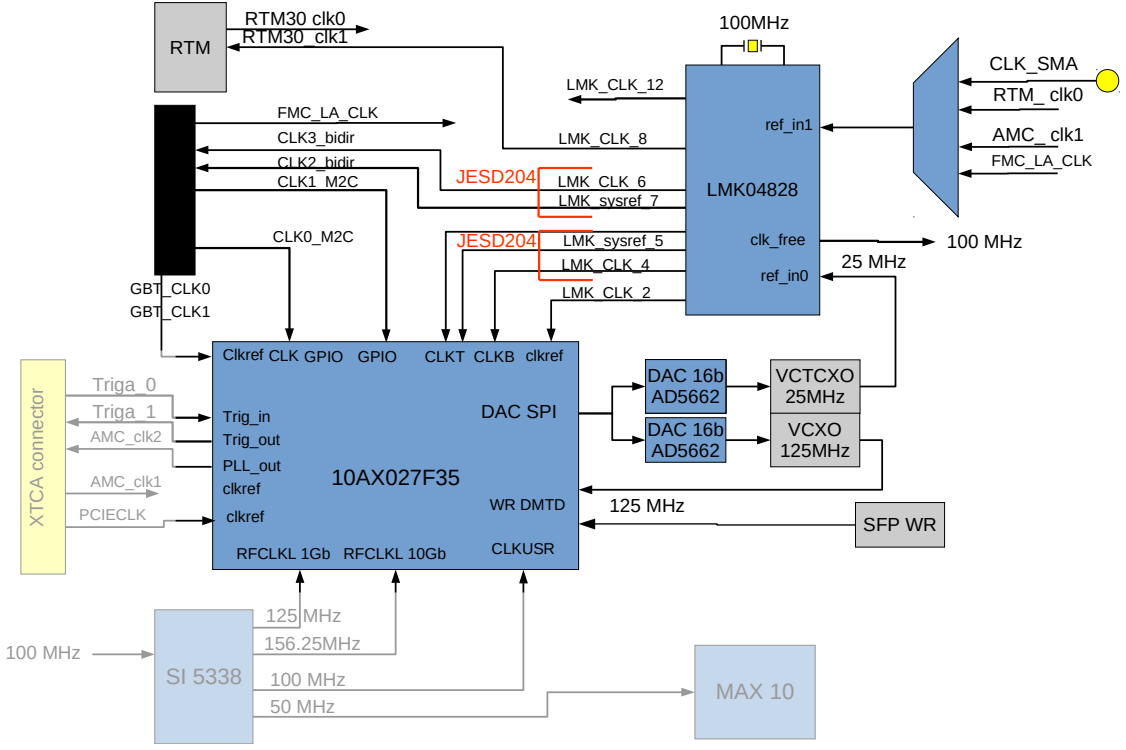

- 2 Clocks cleaner synthesisers.
  - LM04828 for mains clock.
  - SI5338 for Ethernet links and services clock
- All clocks on board derive from synthesisers with single sources.
- All clocks routed in differential.
- Two dedicated clocks JESD204 compliant
- Configure by µC,
- Dedicated tools for configuration.

# Clock tree: main features 2




- LMK4828 clock in :
  - White-Rabbit module.
  - SMA connector.
  - RMT30 connector : CLK0.
  - FMC connector : LA_CLK.
  - AMC connector : TCLKB.
  -
- LMK4828 clock out :
  - FMC connector JESD204 compliant : Clk2_bidir, Clk3_bidir .
  - RTM : CLK1
  - FPGA : CLKREF, clk.
  - AMC_CLK2
- FPGA received also direct clocks from different sources :
  - FMC connector
  - AMC connector
  - RTM connector

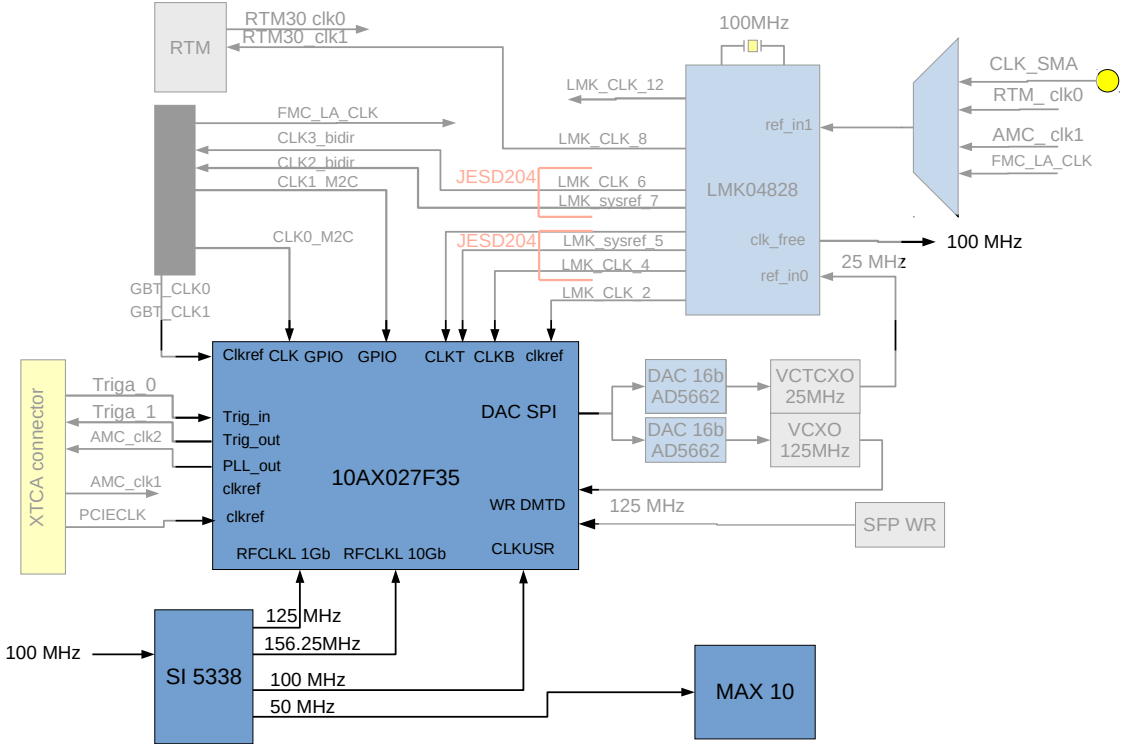
# White Rabbit clocks




A improvement of the open hardware design have been done by LAL/Observatory.

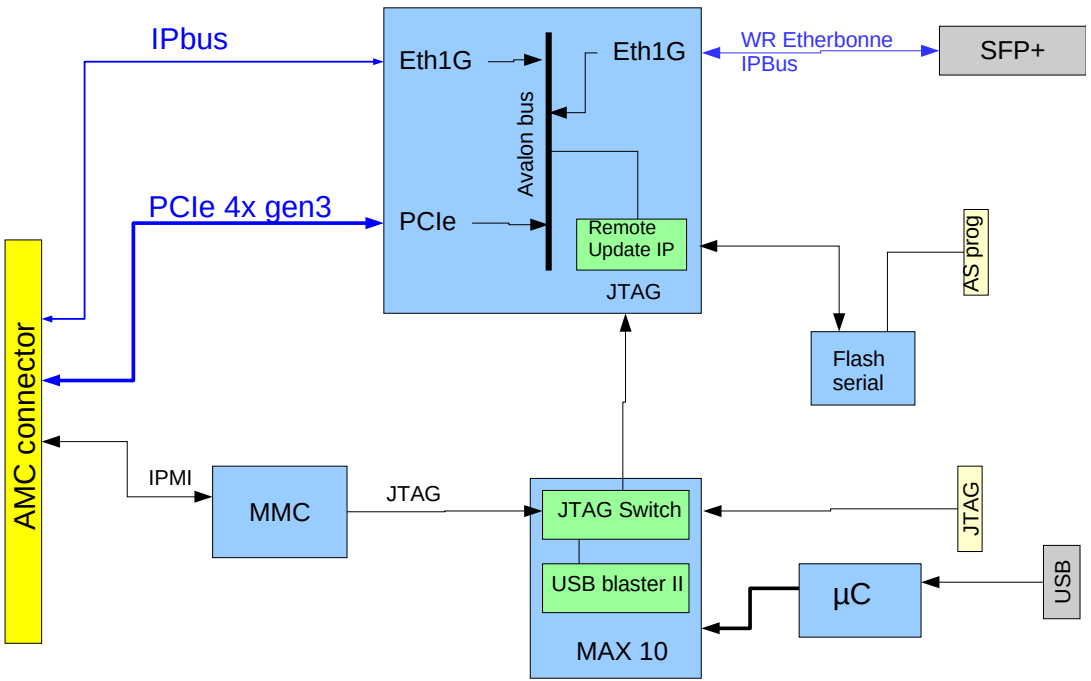
- Base on LMK4828:
  - Ultra low noise clock jitter Cleaner with Dual Loop PLL
  - 90 fs RMS jitter
- Low noise VCXO and ref clock frequency modification
- Dedicated power supply.

# Ethernets clocks



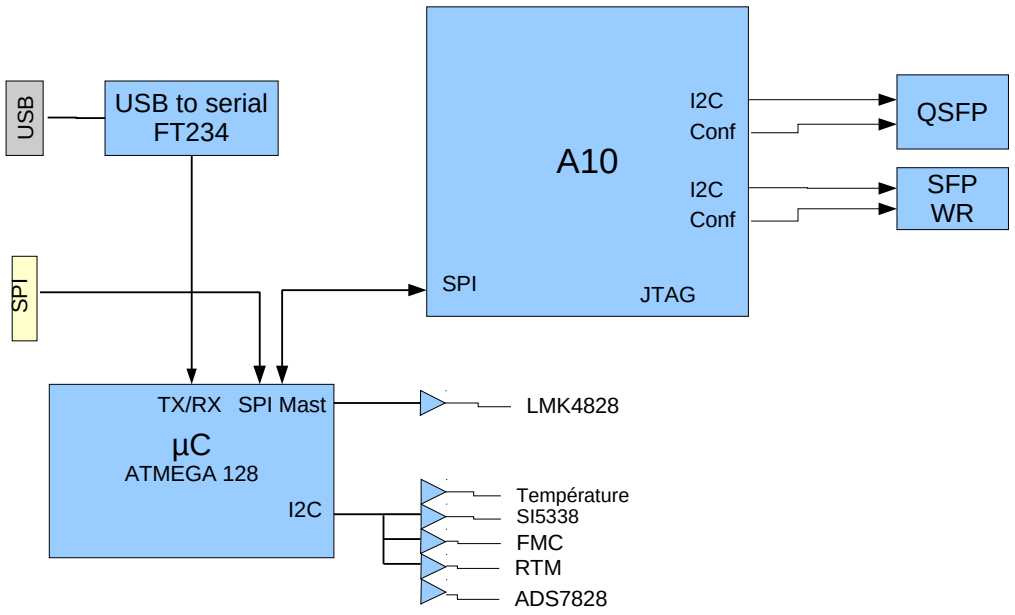

- The serial links clocks are generated by a dedicated synthesiser (SI5338)
  - Configure by µC
  - Input clock reference: LM4828 (clock_free)
  - Output clock:
    - Refclk AMC ETH0
    - Refclk ETH10G
    - CLKUSER
    - Max10.

# FPGA configuration




- Three FPGA configurations capabilities :
  - On-board serial Flash (active serial :
    - EPCQL 256kb
  - JTAG
    - On-board USB-blaster II
    - Connector
  - Remote update :
    - Ipbus.
    - WhiteRabbit Eth link
    - PCIexpress (optional)

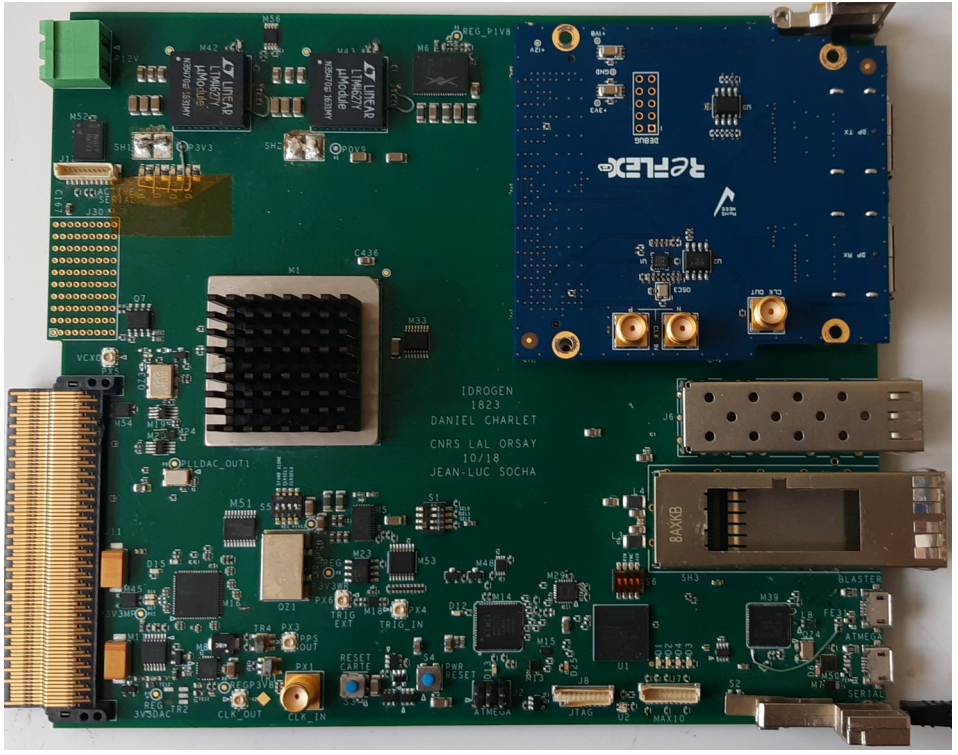
# Components configuration.



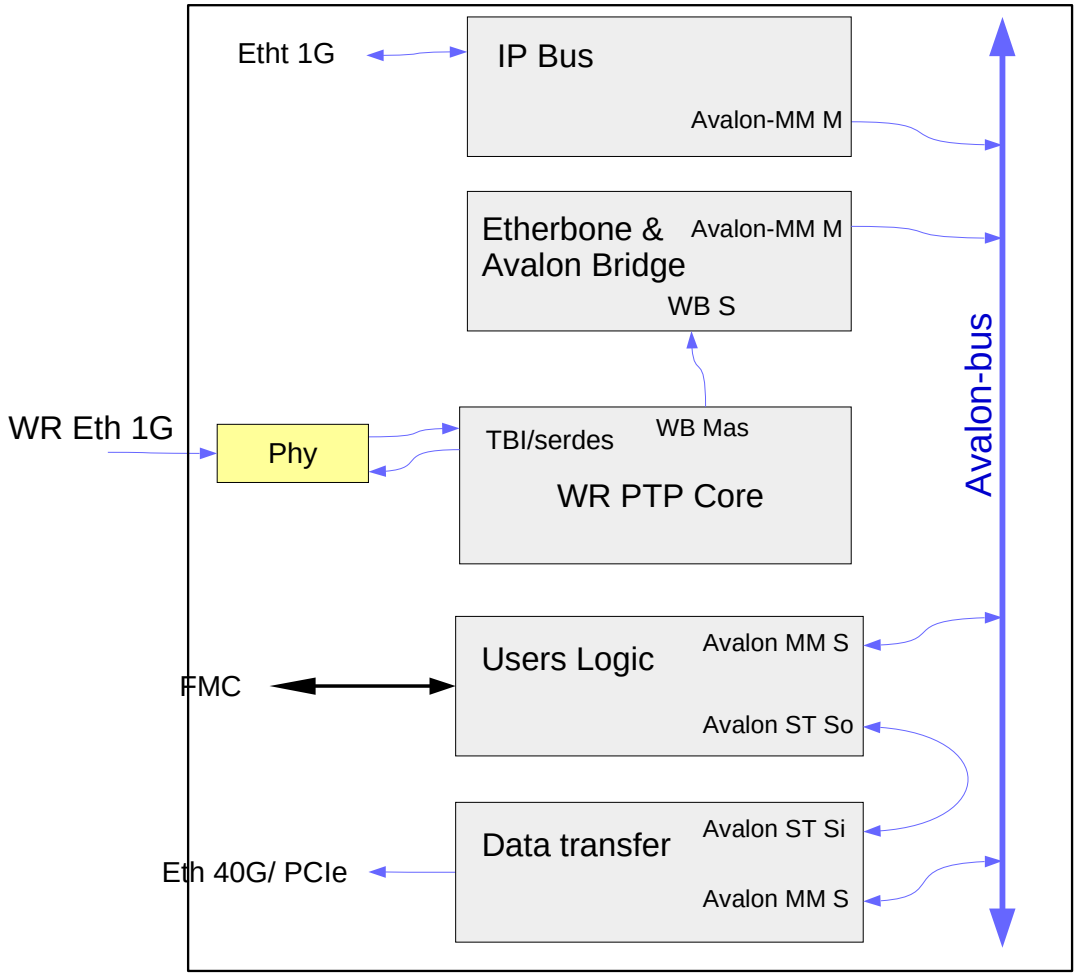

- The mains components are configured by the µC with I2C or SPI.
- The on-board configuration (µC flash) is performed at the power up.
- The configuration could be modify by :
  - USB with dedicated software (see Idrogen software presentation).
  - IPBus or WR via SPI bus (in development)
- The transceivers are configured by the ARRIA10
- µC is configured:
  - SPI dedicated connector.
  - SPI FPGA (not tested).

# hardware status

- PCB currently in production
  - 2 pres-series board
- Test up to end of 2019
- 10 boards production :  beginning of February 2020.
  - 5 for PAON IV project (DIMACAV).
  - 1 CPPM, CENBG (IN2P3)
  - IPHC (IPHC)
  - 2 Observatory of Paris (Observatory)
- Delivery of boards : May 2020



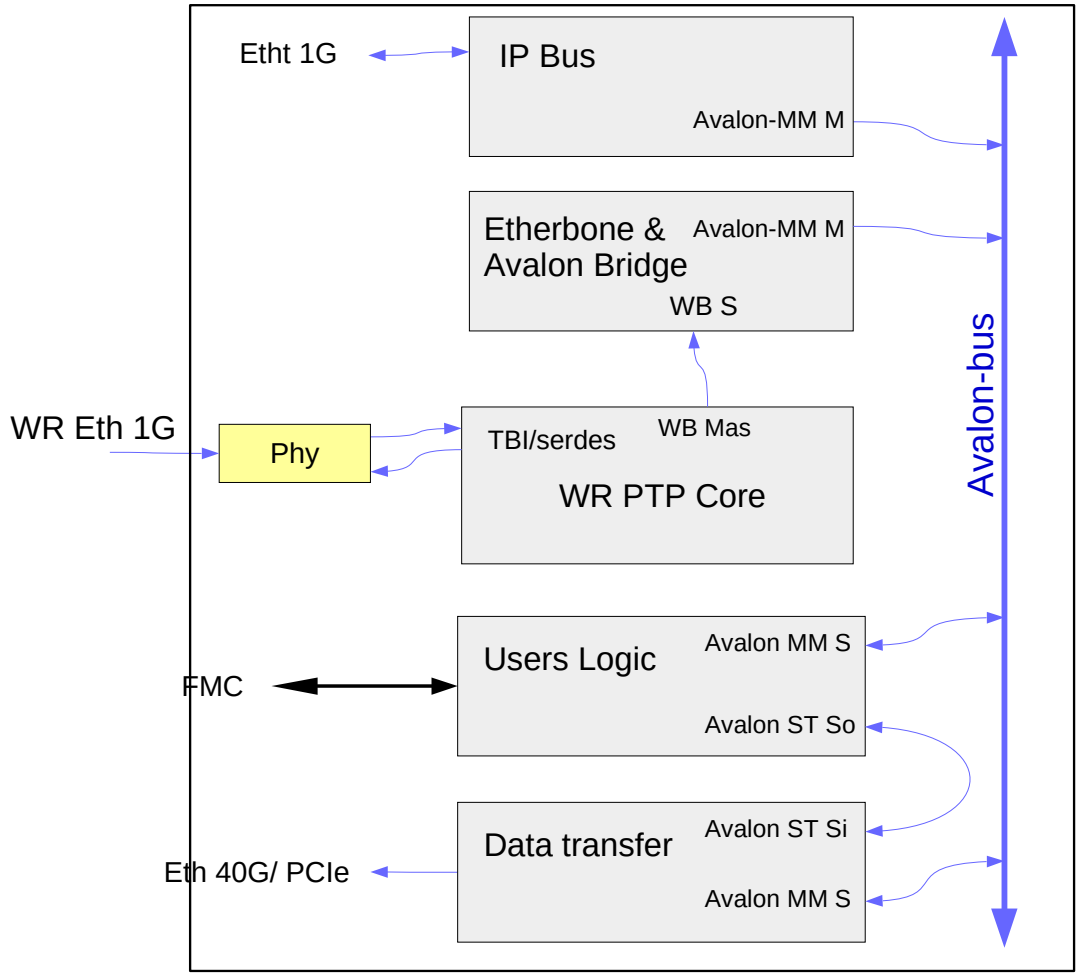
# Firmware architecture




The firmware is develop using QSYS system integration tools.

- Two QSYS Avalon master : IPBus & WR
  - WhiteRabbit PTP core, Avalon master bus.
    - Manage all functionalities for the WR
    - Etherbone protocol.
    - Interface to FPGA core by Wishbone to Avalon interface.
  - IPbus, Avalon master bus
    - Slow-control
    - Data read-out
- Users Logic, interface to FMC connector.
  - Avalon Slave interface.
  - Avalon Streaming source to data-transfer module
- Data transfer, data read-out
  - 2 x 10G Ethernet
  - PCIe Gen3 x4
  - 40G Ethernet (if IP available at IN2P3)

# Firmware status

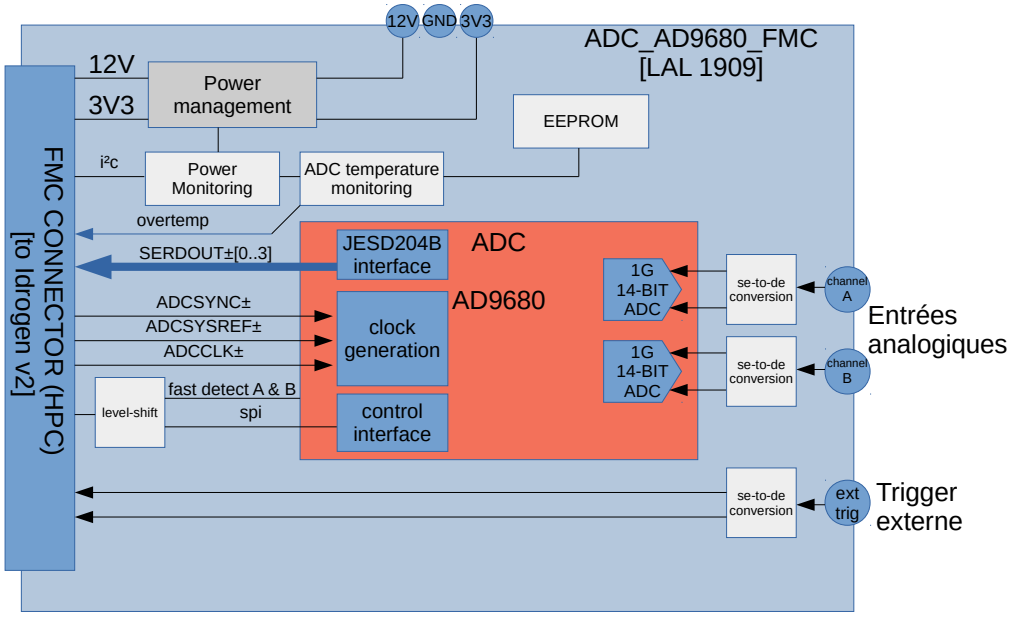



- WR PTP core : CERN open-core
  - Tested
- Etherbone & Avalon bridge
  - Tested
- IP-BUS
  - LPSC on going porting

- Data transfer,existing bloc to integrated :
  - PHY, MAC : Intel IP
  - UDP framing (CASPER project)
  - ARP (CASPER project)

  - Users Logic :
  - Ref design : supply by Analog-Devices.

# Mezzanine ADC

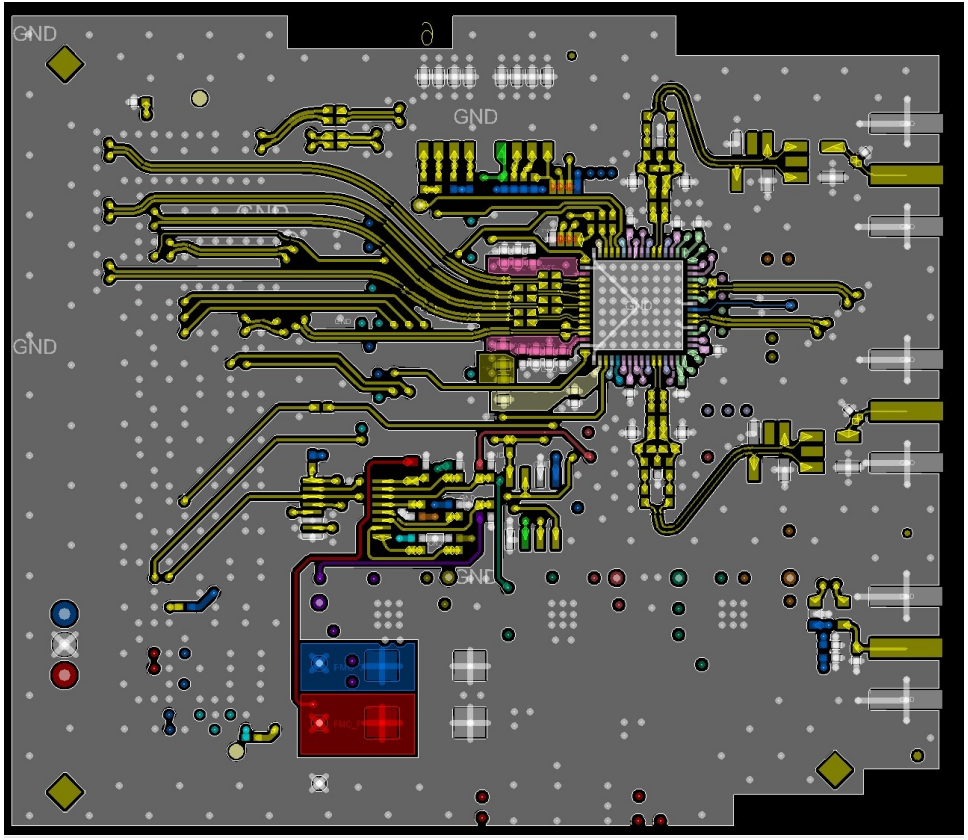



The motivation of the development of a new mezzanine instead off an on-the-shelf ADC mezzanine :

- include : its own PLL.
- ADC clock source : External clock

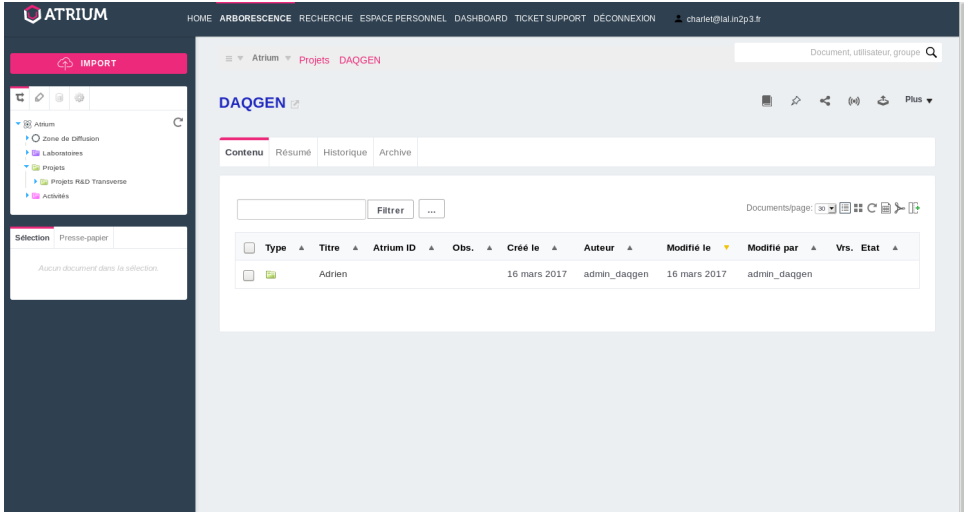
- Mezzanine main features :
  - VITA57.1 (FMC)
  - ADC 9680
  - 2 channels
  - 14 bits
  - 1.25 GSPS
  - JESD204
  - 2GHz analog bandwidth
  - External trigger in

# Status Mezzanine ADC




- PCB : 4 Layers
- Schedule :
  - Production of 2 prototypes : October.
  - Test : mid November.
  - Production of 6 boards : Beginning of 2020.

# Documentation



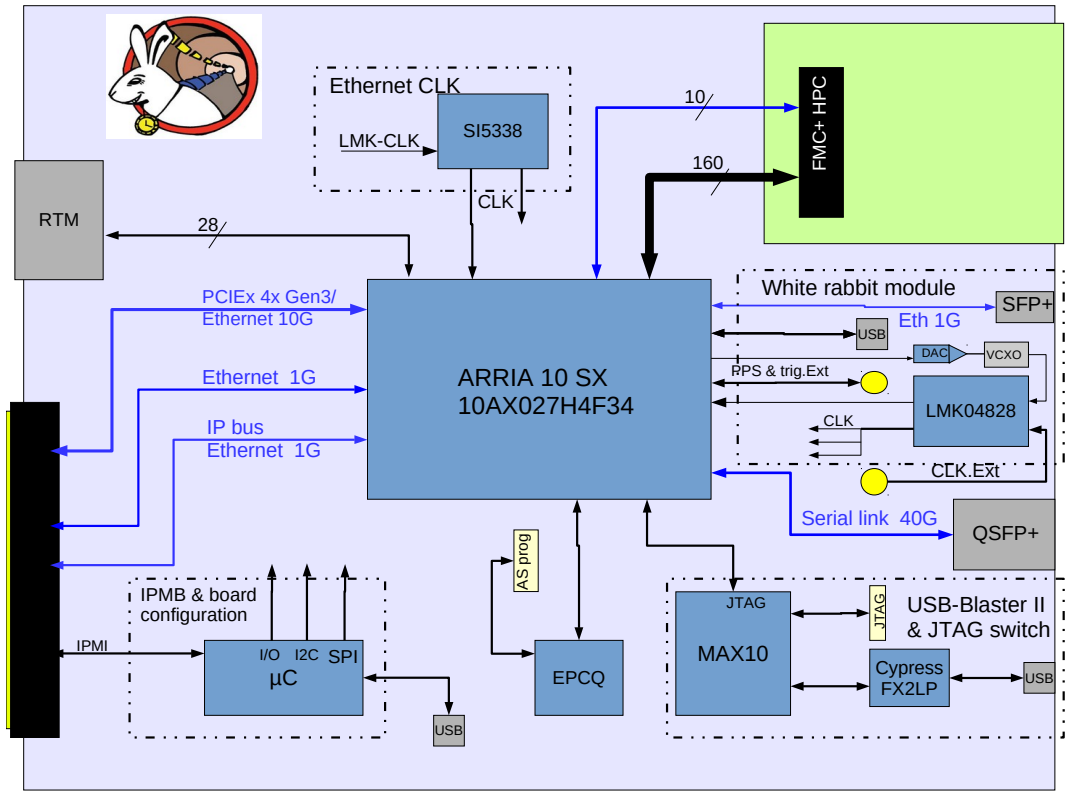

- Schématique
- Brd
- Firmware
- Software
- Documentation

# Conclusion

- IDROGEN-2  en cours de fabrication
- Firmware whiteRabbit porté sur ARRIA10 testé
- Tous les modules du firmware disponible mais sont à assembler
- Carte IDROGEN disponible début  2020.
- Mezzanine ADC disponible début 2020

- Carte OXIGEN (Version xilinx) : développement devrait débuter prochainement

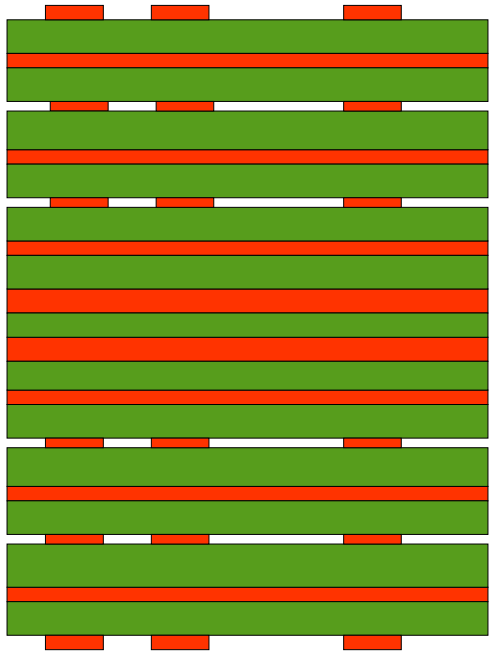
# Carte IDROGEN




- On board configuration (µC)
- Very low noise synthesizer PLL
  - synthesizer cleaner (LM04828) for WR clk and derived clk.
- Dedicated PLL for serial links
- Integrated USB-Blaster II.
- FPGA configuration :
  - Active serial,
  - IP bus.
- External connectivity :
  - PPS,
  - Trigger,
  - Ext CLK.
- FMC connectivity

# Empilement

| | | | |
|---|---|---|---|
| 1 | 55 | Signaux | 85 Ohm |
| 2 | 40 | GND | |
| 3 | 17 | Signaux | 85 Ohm |
| 4 | 40 | GND | |
| 5 | 17 | Signaux | 85 Ohm |
| 6 | 40 | PWR | 3,3v |
| 7 | 70 | PWR | 0,9v/12v /1,8v |
| 8 | 70 | GND | |
| 9 | 40 | PWR | |
| 10 | 17 | Signaux | 85 Ohm |
| 11 | 40 | GND | |
| 12 | 17 | Signaux | 85 Ohm |
| 13 | 40 | GND | |
| 14 | 55 | Signaux | 85 Ohm |



| | |
|---|---|
| 75 | 1 |
| 100 | 2 |
| 100 | 3 |
| 100 | 4 |
| 100 | 5 |
| 50 | 6 |
| 50 | 7 |
| 50 | 8 |
| 100 | 9 |
| 100 | 10 |
| 100 | 11 |
| 100 | 12 |
| 75 | 13 |

- 14 layers
  - 6 signal layers
  - 3 Gnd
  - 5 power layers
- 4 layers with laser drill.
- Impedance controlled (85 Ohm ) on signal layer.