Test Beam Summary and Single Slab Performance studies.

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SiW-ECAL CALICE

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- Two weeks of Beam Test at TB24. From 24th June to 7th July.
- Presence from

- Plus support & hardware from

Outline

- Software + data
- Setup
- Event Reconstruction and time correlation
  - Noise bursts (we need to optimize the val evt veto)
  - Some Results

- Performance comparisons: COB vs FEV, SLB vs DIF, 2019 vs 2017
  - Retriggers,
  - Pedestals
  - MIP signals

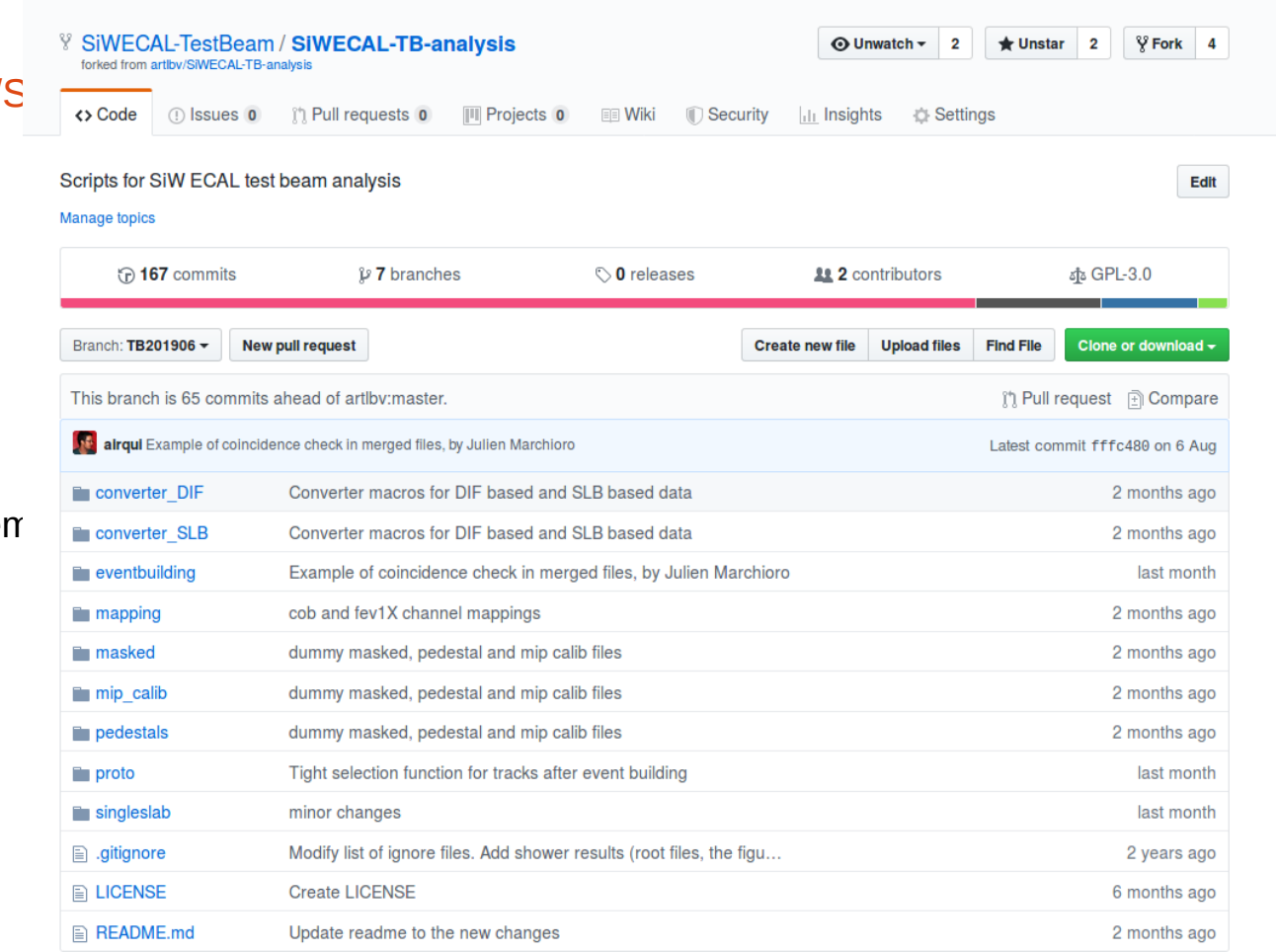
Unless explicitly said, all results correspond to the run 32015 (first long run with all systems in and synchronized, no tungsten)

I also show some TB2017 data taken in similar conditions.

Software

Software

- Public github repository
- https://github.com/SiWECAL-TestBeam/SiWECAL-TB-analysis
- **branch TB201906**
- Don't use the version in the eos! It is outdated in there.
- Full of READMEs
  - Please use them (and help complete them if needed)



Software: folders

- **converter_DIF and converted_SLB**
  - Default root converters. From binary (DIF) or ACII (SLB) to single slab root files in the 2017 style.
  - Since the SLB delivers all the SLB data in one file, it would be good idea to create root files with all slabs together from the beginning.
- **mapping**
  - One file for FEV10, 11, 12 and FEV13 mappings
  - FEV11 COB mapping
  - Simple function to read them.
- **mip_calib, pedestals, masked**
  - Folders with the calibration, pedestal and list of masked channels.
  - Simple ASCII files
  - WE NEED THEM FOR THE EVENT BUILDING but as this require full analysis not yet finalized, in each folder there are macros to create dummy files.

Software: folders

singleslab

- Analysis macros for single slabs.
- Main functions: PedestalAnalysis, Retriggers, SignalAnalysis → Read the README

eventbuilding

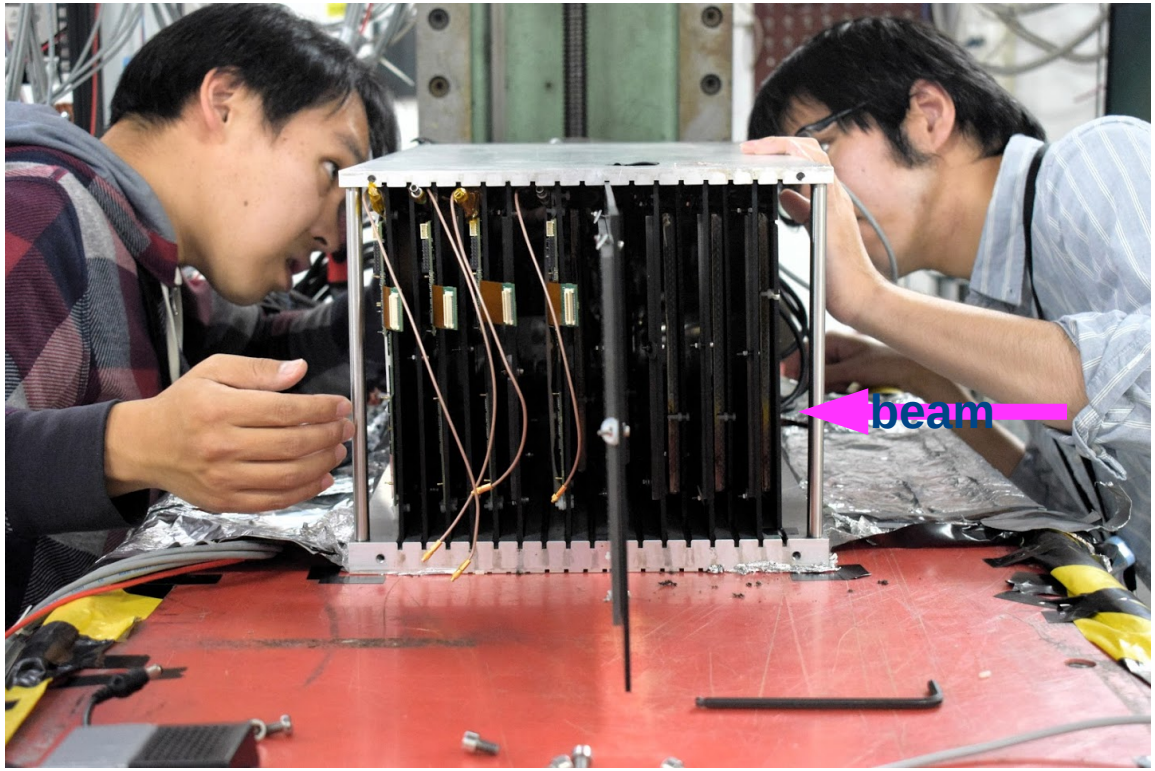
- Mix of python and simple c++ root scripts to perform the event building.
- mergeRootFiles.cc → Merge single slab files and automatically peforms the bcid offset correction between the slabs
- build_events.py → performe the event building by looking at conicidente bcids (+-3). This requires mapping, pedestal and calibration files.
- eventbuilding/macros contains an example of coincidence check in merged files.

proto

- Example macros to run over event built files (analysis of all the slabs at the same time)

Setup

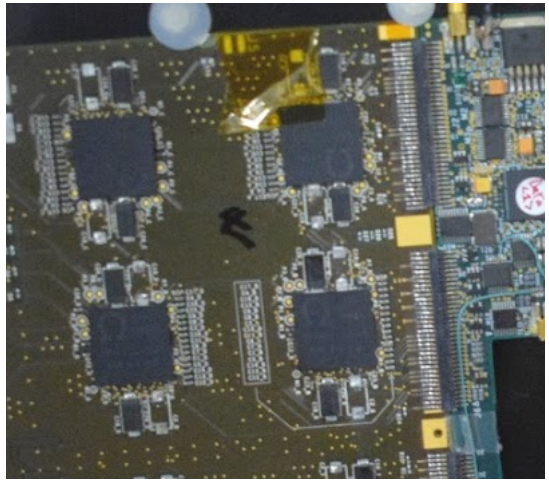
Setup



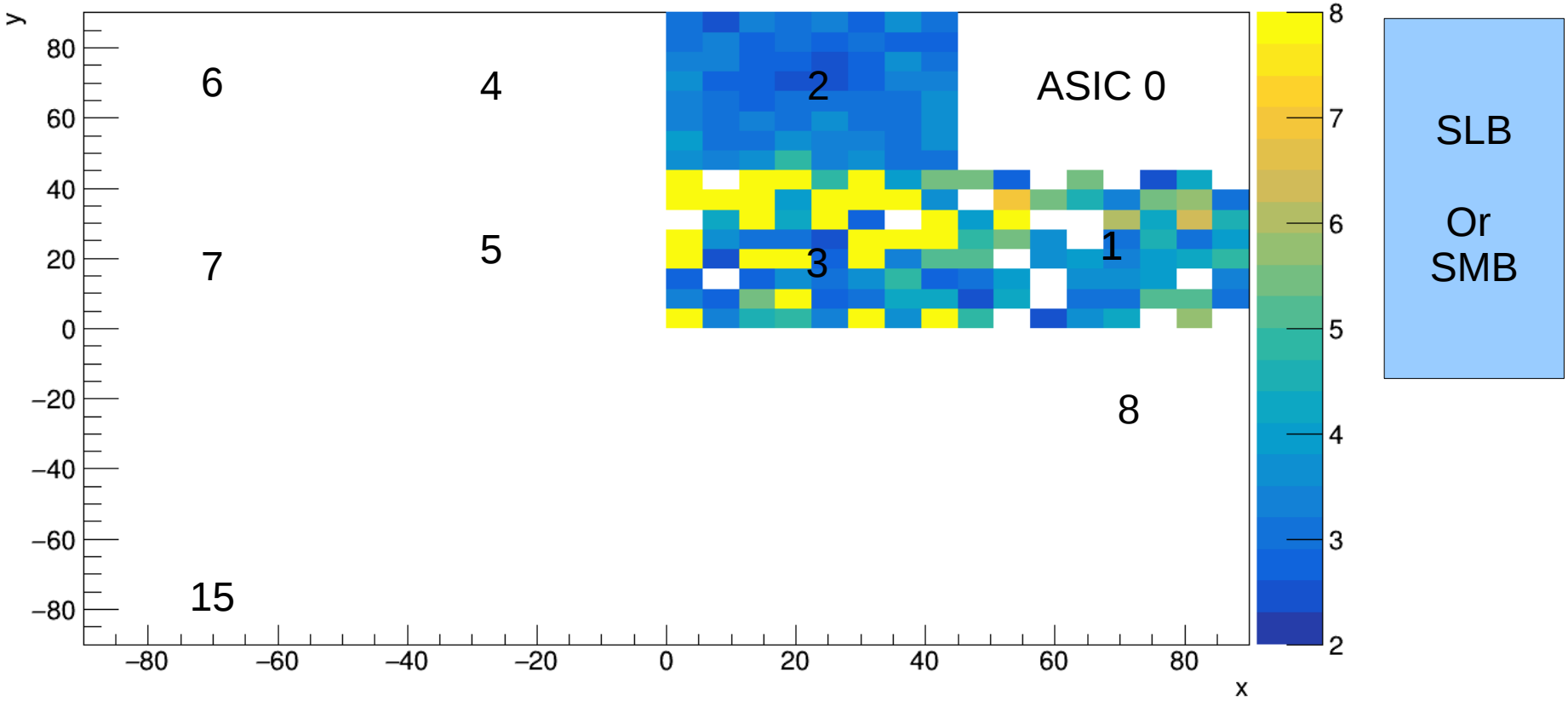
Layer	Plate slot	Name	LVcable	DIF cable	HDMI cable	GDCC port	other
1	17	P1 (650um)	6	6	?	6	dif_1_1_1
2	15	P2 (650um)	7	7	?	7	dif_1_1_2
3	13	P3 (320um)	8	8	?	3	dif_1_1_3
4	11	K1 (650um)	9	9	?	4	dif_1_1_4
5	9	K2 (650um)	10	10	?	5	dif_1_1_5
Layer	**Box slot**	**Name**	**LV cable**	**kapton slot**			
6	8	COB_a, SL1.2	4	6			
7	5	FEV12, SL1.1	3	4			
8	3	FEV12, SL1.3	2	2			
9	1	COB_c SL1.0	1	0			

SLB based slabs

- Two COBs with different amount of extra components (i.e. AVDD, DVDD external decoupling capacitances)
  - COB_a started “naked” and ended up with 4 CMS 140uF capacitances
  - COB_c with zero extra components (but an aluminum plate used as a chip protection used during the gluing).
- 2 FEV12 fully equipped with all components



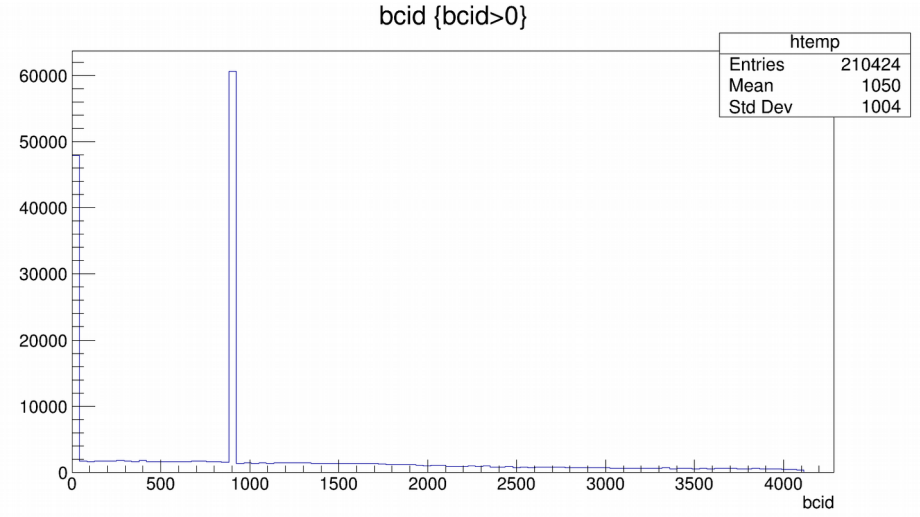
X-y plots, convention:



Time Correlations

Filtering bcid =0 events in SLB systems

- Noise bursts in the SLB systems (BCID <15, BCID ~900). To be removed with a val_evt signal.
- These events are removed in all analysis shown here.



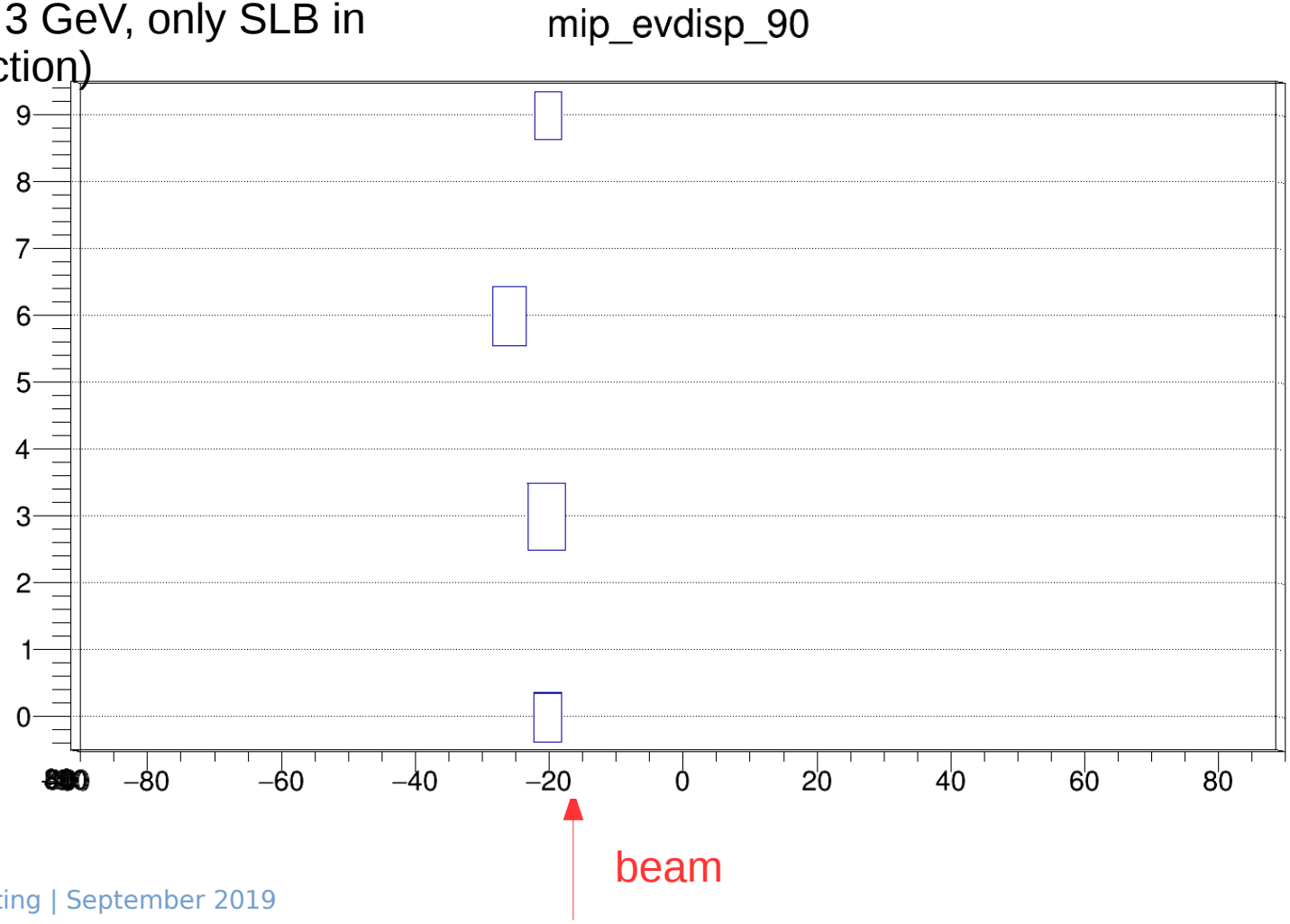
SLB and DIF based slabs synchronization

- https://llrelog.in2p3.fr/calice/2147
  - Setup of Synchronation via common spill send by the pulse gen used by the CCC.
  - FEV13 setup prepared in the usual way. Spill freq to 4Hz, 2.4ms.
  - SLboard system is prepared in self-trigger mode with acquisition windows source from external signal
  - FEV13 systems needed to reconfigure each time to reset the cycle number.

- The event building is based in having common cycle numbers (acquisitions) and a fixed bcid offset between the two systems
  - In an offline analysis, the BCID offset was calculated to be: BCID(SLB) = BCID(FEV13) + 2492

Some built events (vey preliminary)

32014 (MIPs, 3 GeV, only SLB in the reconstruction)



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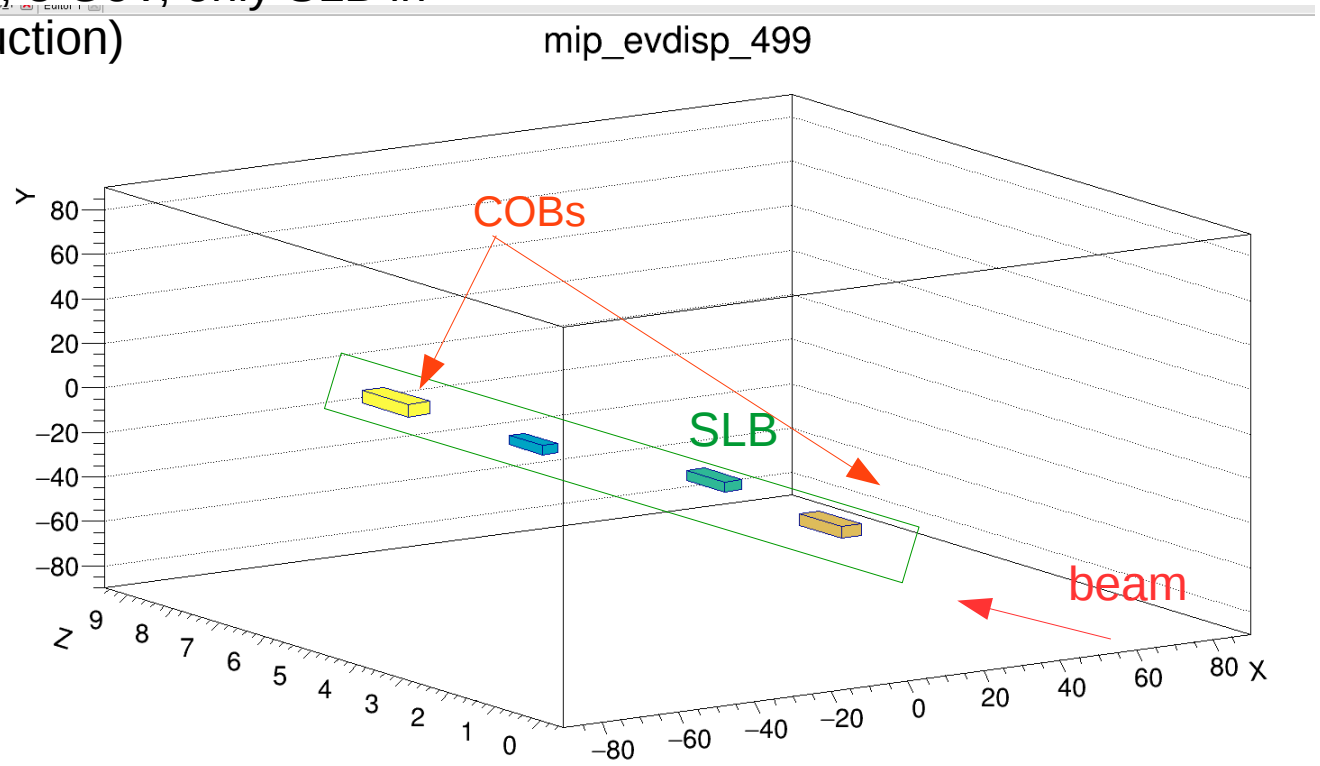
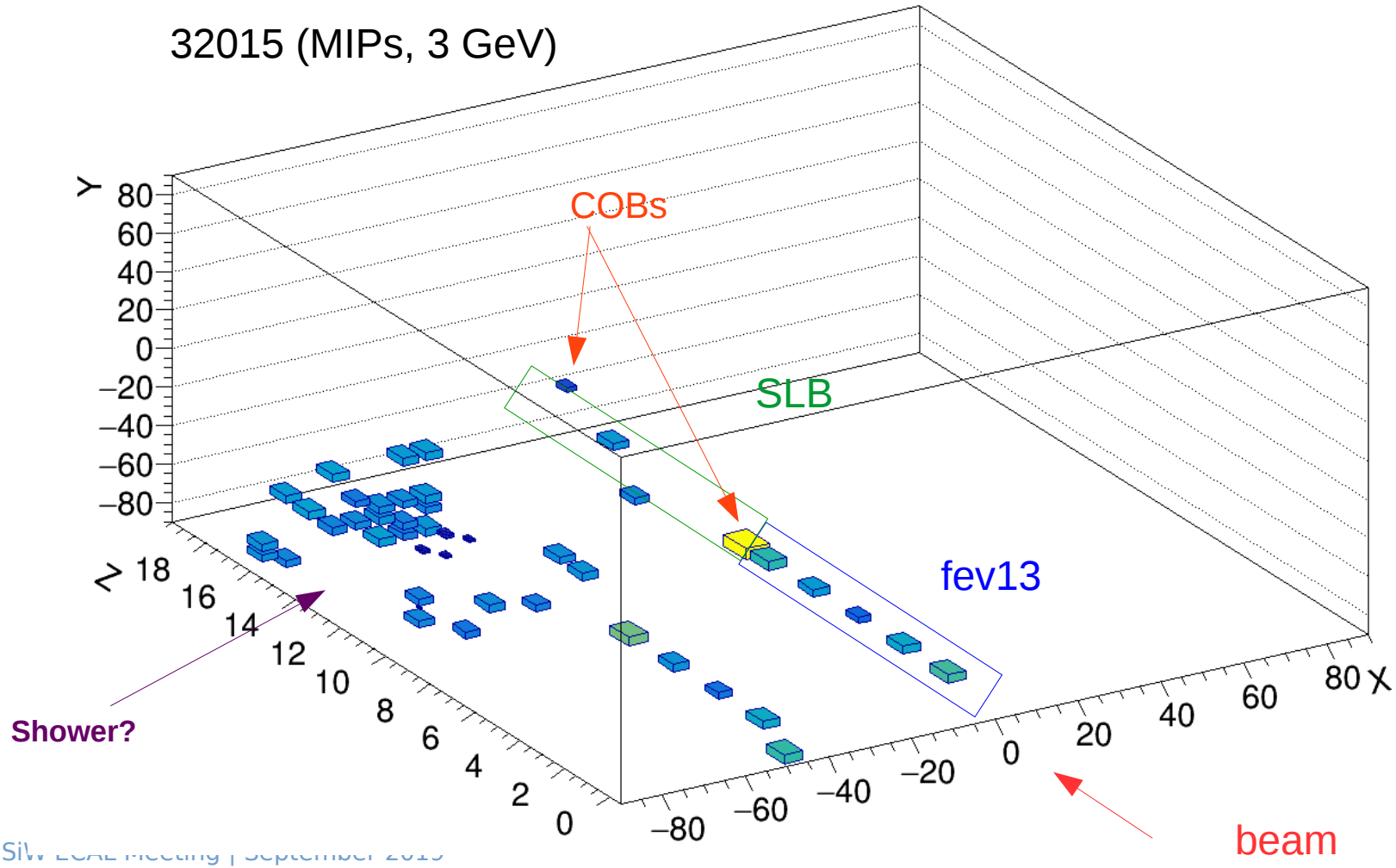
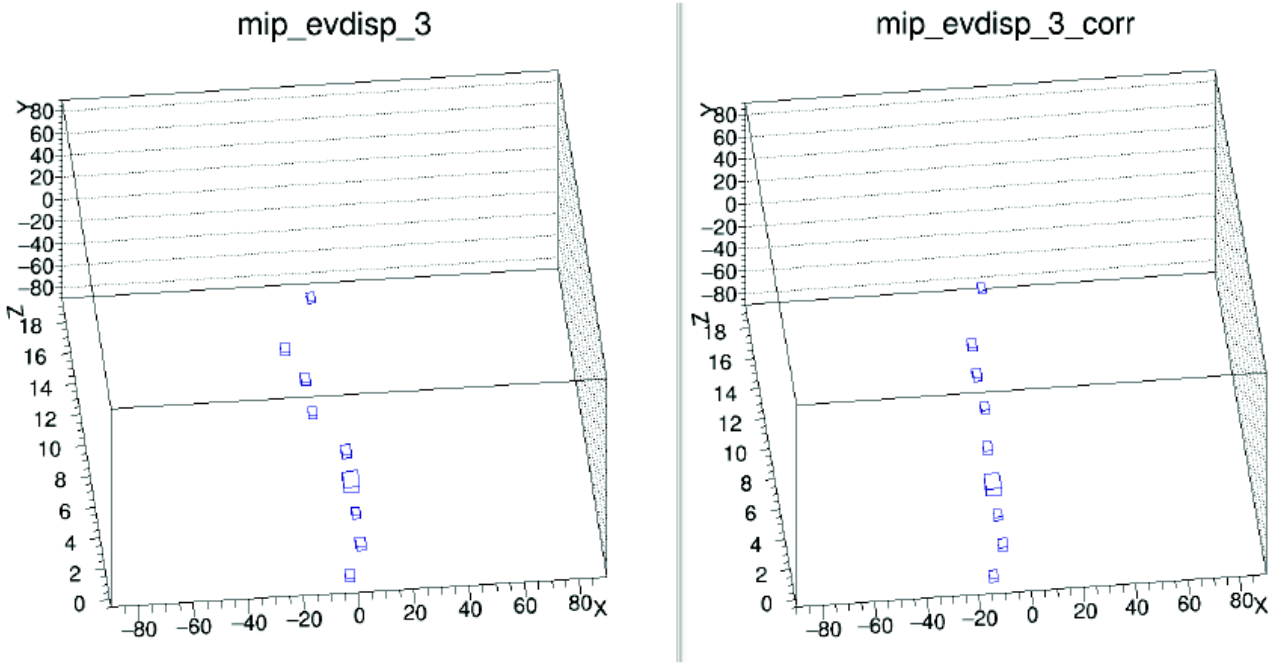


Some built events (vey preliminary)



Some results: using tracks to align the modules



- Julien Marchioro (Work in progress)
- See folder *proto* in the repository

Retriggers

What is a retrigger?

- We have observed, (since the beginning of the tech. Prototype) the presence of the so-called retriggers.
- They are seen as bunches of consequtive triggers in trains of bcids
  - They are associated to power supplies baseline changes and instabilities.
  - Traditionally reduced by adding extra decoupling capacitances.

- They are filtered in the very early analysis stages, using a variable that we called badbcid (if badbcid=0, then the event was not bad).
- We do the filter in an ASIC per ASIC basis. If there is more than one event **separated by 1-10 BCIDs** (tuneable), we tag the fulls train of events using badbcid==3. This includes THE INITIAL trigger, which may be a good one.

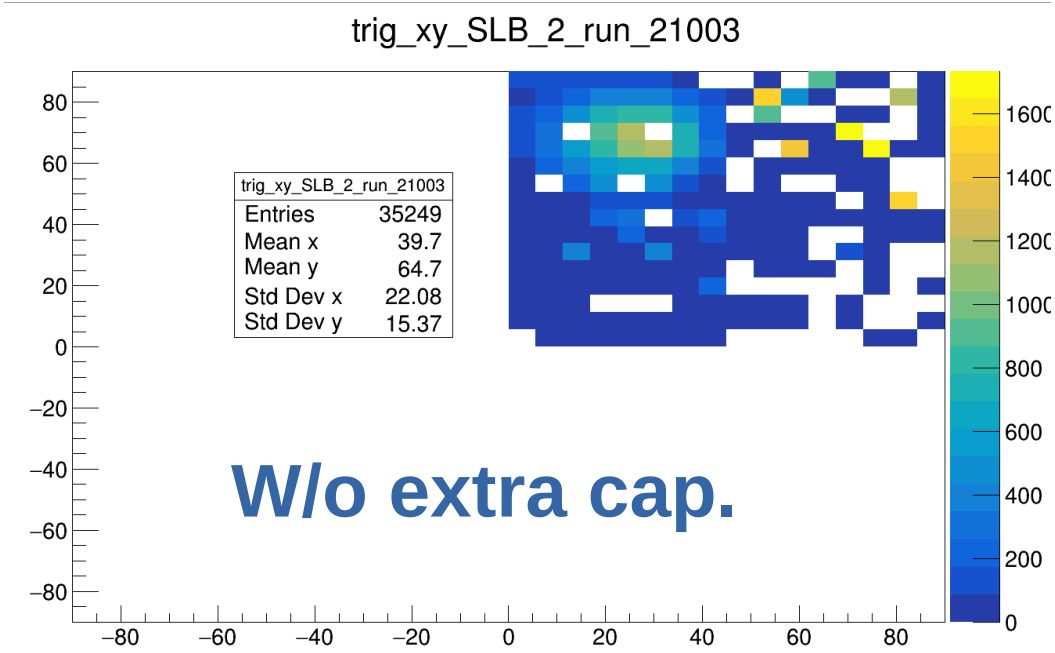
COB-a: with and without extra capacitances

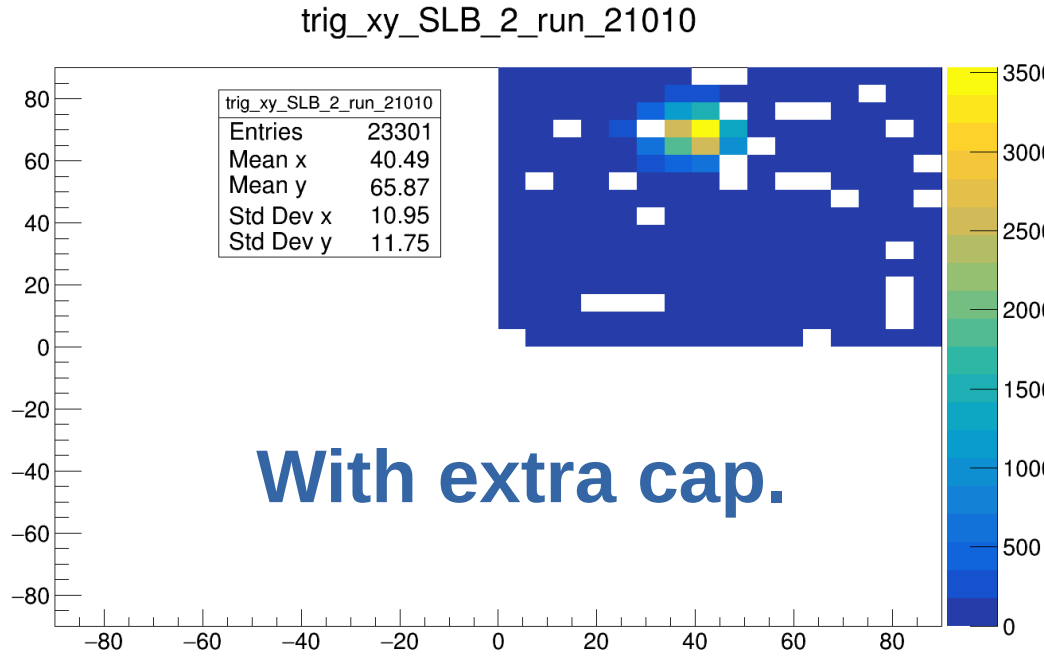
- First runs with 3.6pF, DAC=300 and with same acq window (2ms, 10Hz)
- Add 4x150uF cap. Between AVDD and GND. https://llrelog.in2p3.fr/calice/2130
- The two compared run have similar statistics of total events,
  - But the first run (21003) had no collimators between the beam line and the detector (higher rates and larger beam spot)

- Disclaimer: It is also true that the first runs may suffer from more noise for the sensors (stabilization of the glue, stabilization of the depletion etc etc).

COB-a: with and without extra capacitances

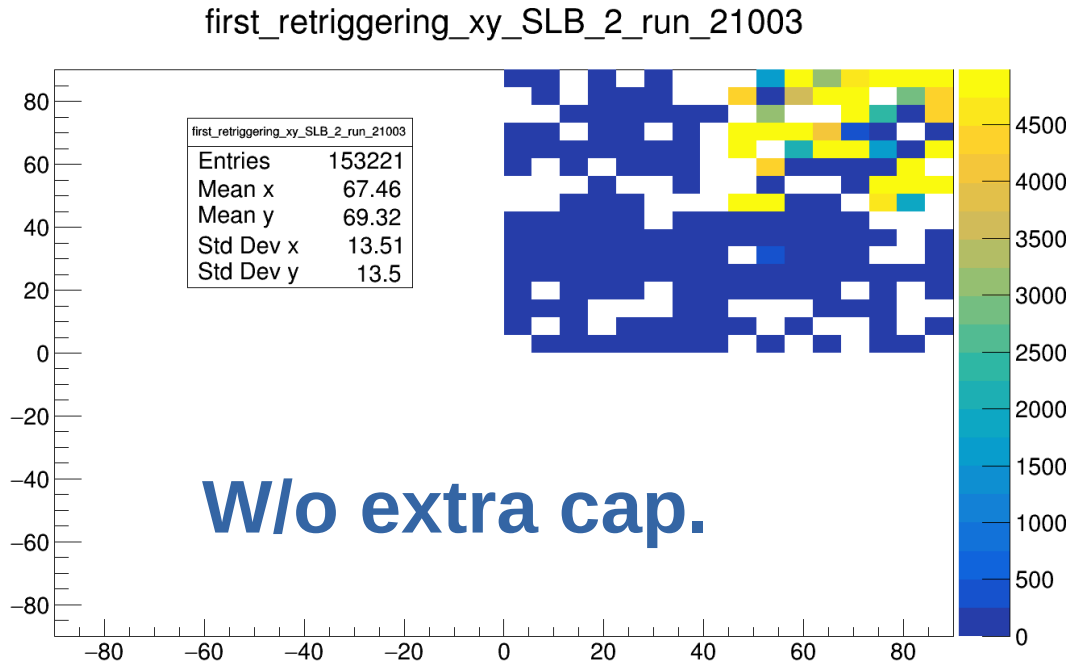
- ***GOOD* TRIGGERS:** More or less comparable statistics in both runs.
- Around 1000 entries per cell in the beam spot in the first run, and ~3500 in the second, but the beam spot was smaller.
- In the first run we have systemtically noisy cells near the SL-board (ASIC 0)

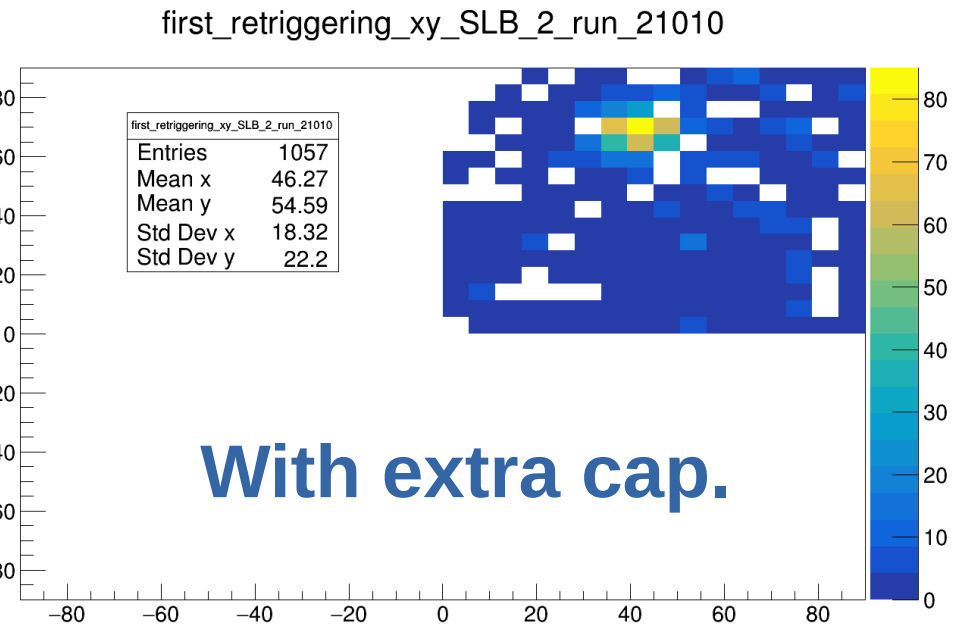




COB-a: with and without extra capacitances

- ***RE*- TRIGGERS:**
- Before adding the capas. Lots of retriggers in the nearby of the SLBoard !!
- After adding the capas, we have a maximum of 80 rettrigers trains over 3500 good hits, in the beam spot ! So they may not even be retriggers, just overfiltered signals.





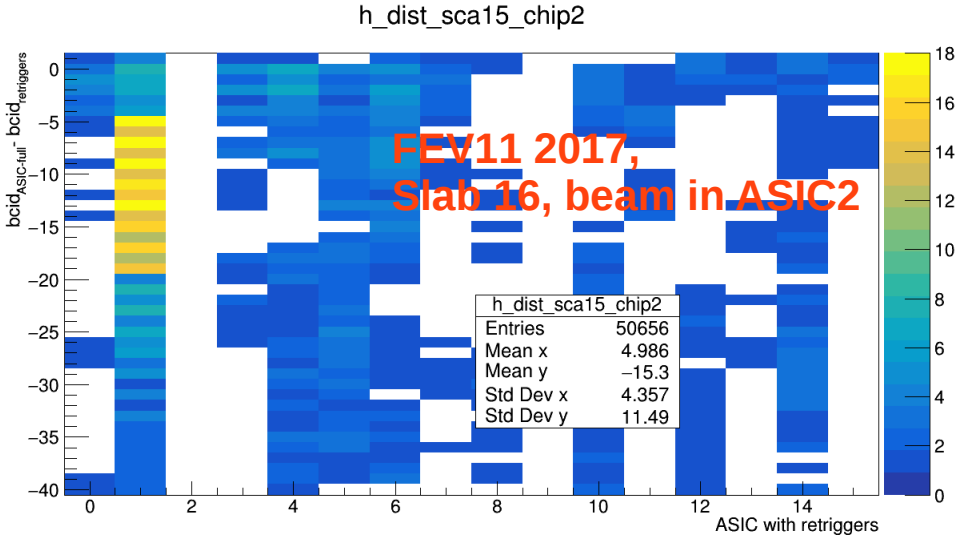
Some pre- conclusions:

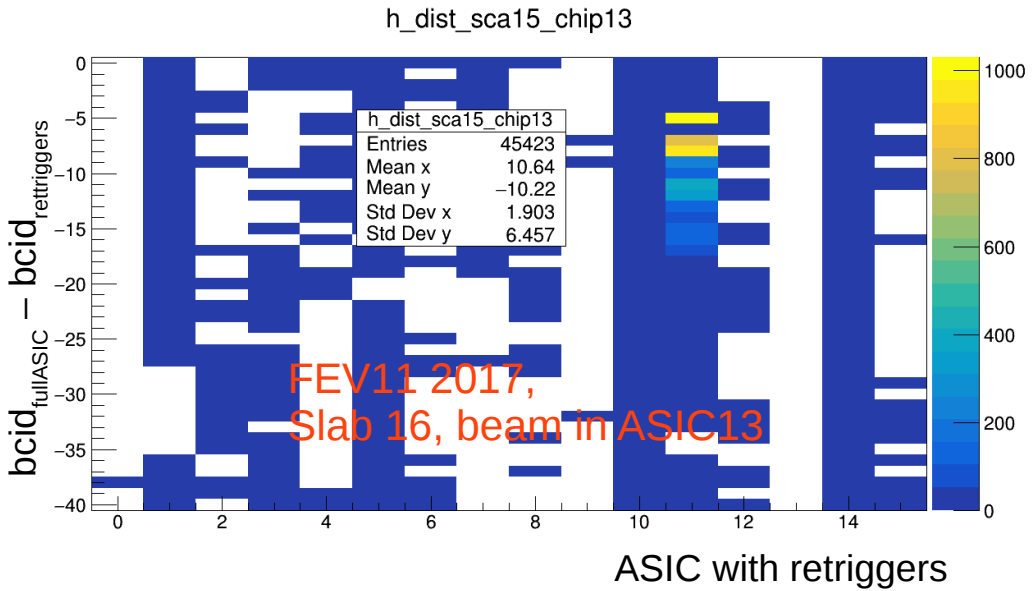
- Even with the differences in the settings and enviroment between the two runs we can safely conclude that the decoupling capacitances had a large effect to reduce the retriggers occuring in different region of the PCB “far” from the beam spot (and near the electronics).

- The observed issues in the chips near the connectors are NOT NEW. Seen also in the past (FEV11).

Study of the retriggers. CHIPSAT in FEV11

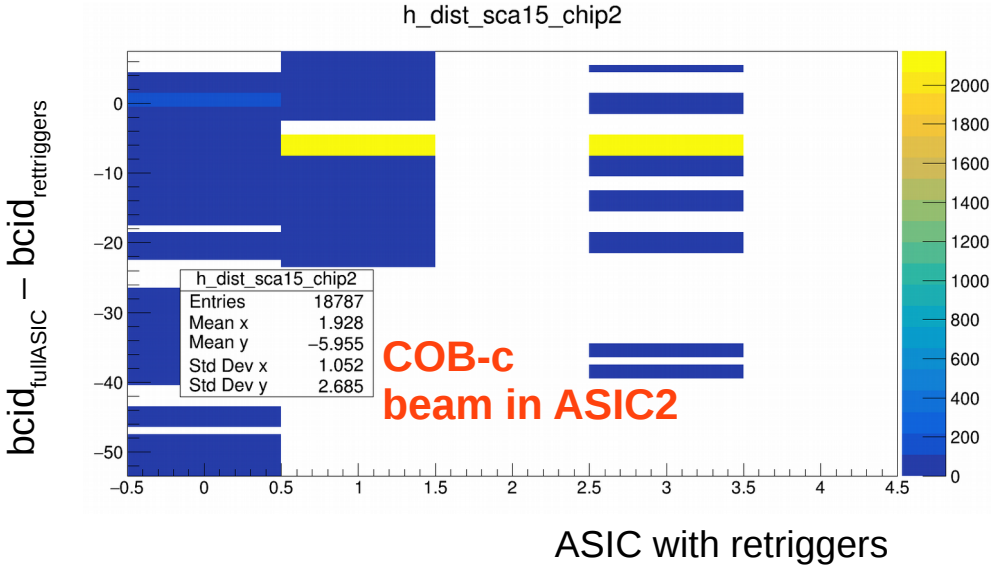
- Chipsat signal as a source of retriggers.
- If the ASIC in which the beam is directed is full… I check the correlation with the bcid of all retriggers in other ASICs

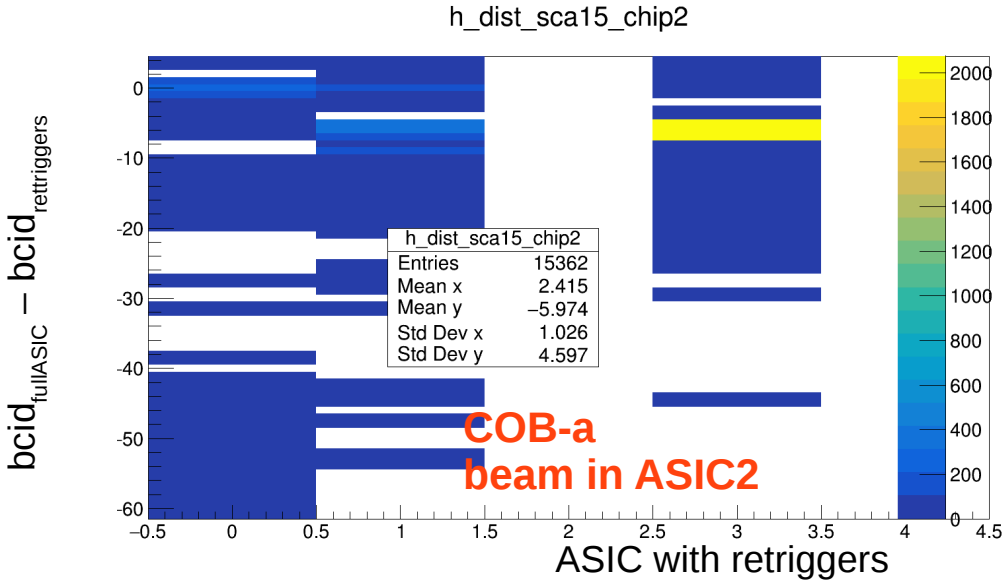




- FEV11 TB2017.
  - Correlation of about 5-10 bcids

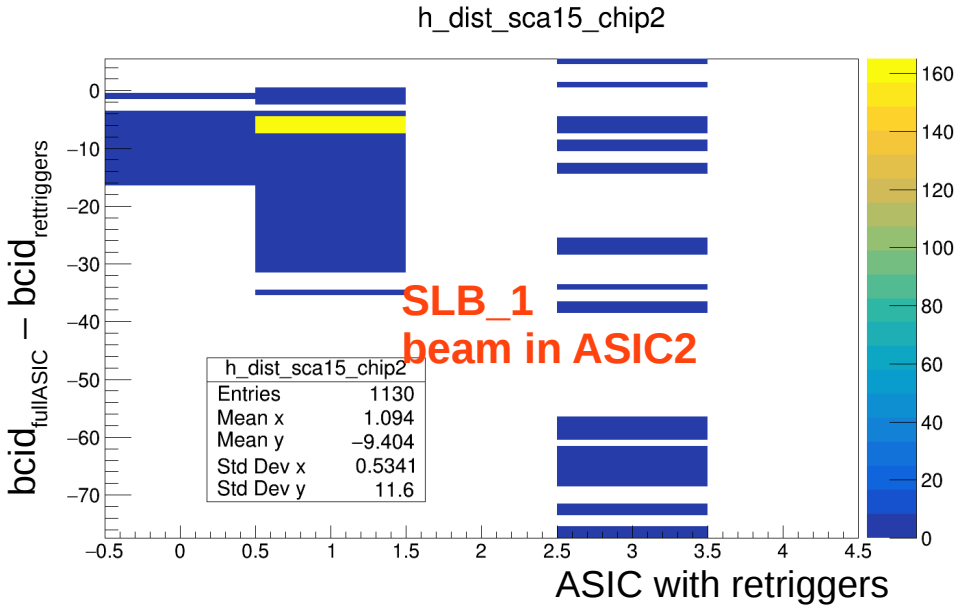
Study of the retriggers. CHIPSAT in COBs





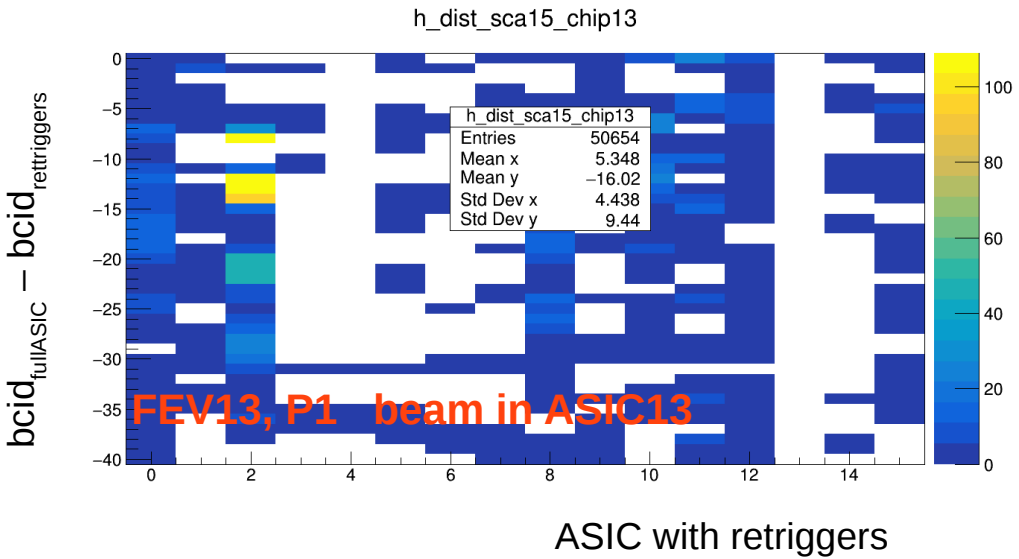
- Less entries in the COB-a case, and only in one ASIC.
- CHIPsat has effects in different ASICs.
- Also a ~5 BCID separation, although the clock period is now half than in 2017.

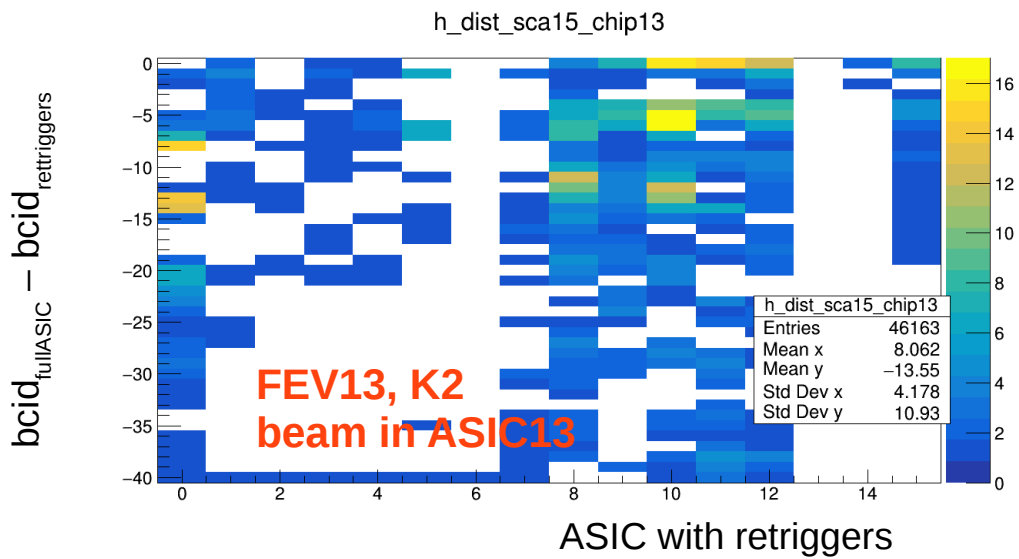
Study of the retriggers. CHIPSAT in FEV12



- Similar pattern than COB-c and FEV11 but much less entries than COBs…
- ISSUE with SLB configuration (wrong gain? Wrong hold value? Wrong threshold?)
  - NO DIRECT COMPARISON POSSIBLE until we understand it
  - Briefly discussed later.

Study of the retriggers. CHIPSAT in FEV13s





- Factor x2-3 more of rettriger entries
  - But number of chips is x4 larger
  - And the retriggers are “less correlated” (most of the entries don’t fall in the plotted range)
- Similar pattern? Maybe yes for P1, for the others it seems less clear: .

Some pre- conclusions:

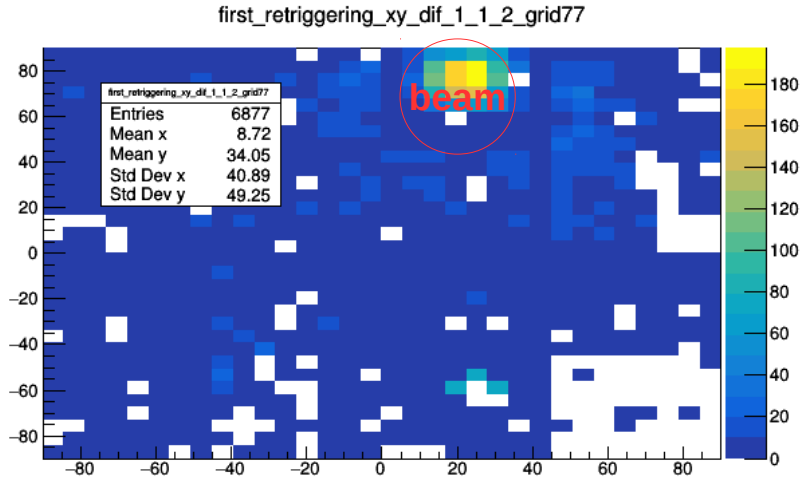
- The relation between chipsat and start of retriggers seems to not depend on the front ends (DIF or SLB).
- The FEV13 seem to be less sensitive… maybe because of the separation in more than one AVDD layers in the PCB
  - But it seems that FEV13 have more total retriggers? See next discussion.
- The COB-a (with extra capacitances) shows better performance than the C
  - Unfortunately, the comparison of the COB-a before and after adding the capacitances is not conclusive due to the difference of beam rates (difference of events per acquisiton).

Retriggers : FEV11

FEV11
Slab16

~0.2 retrig trains / trigger

All/first ~36

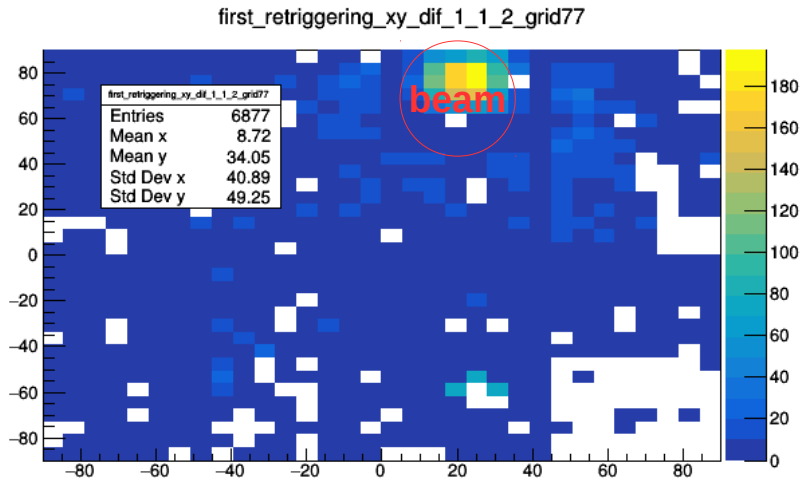


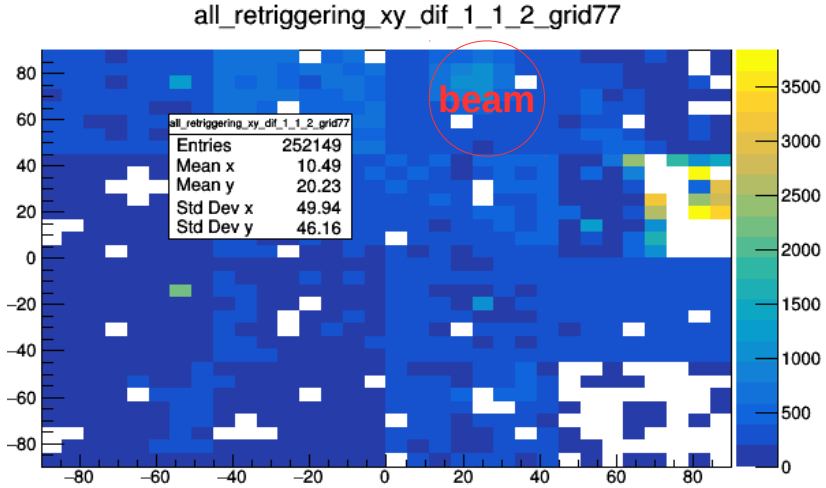
Retriggers : FEV11

FEV11 Slab16

~0.2 retrig trains / trigger

All/first ~36



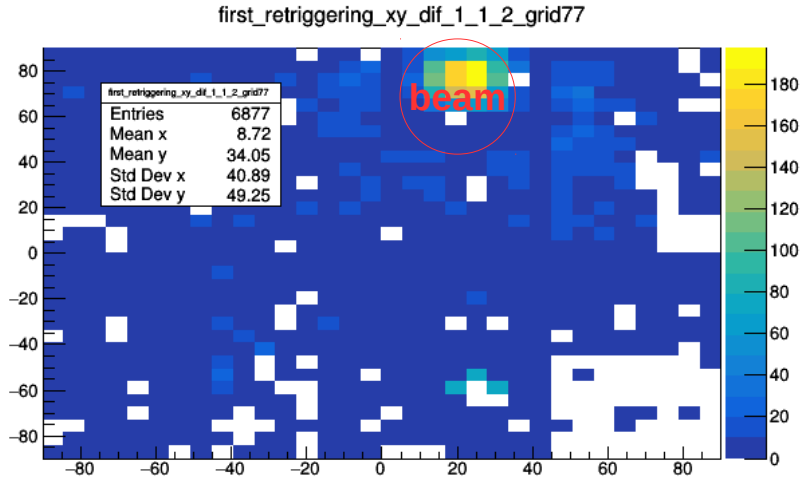


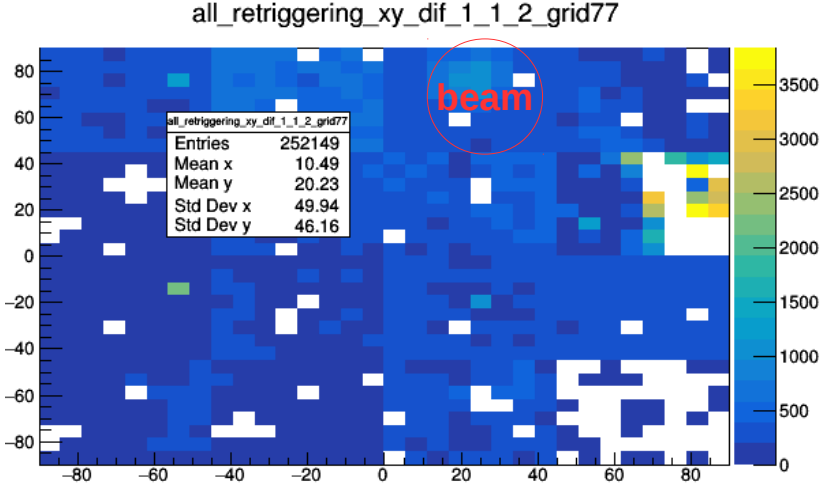
Retriggers : FEV11

FEV11 Slab16

~0.2 retrig trains / trigger

All/first ~36

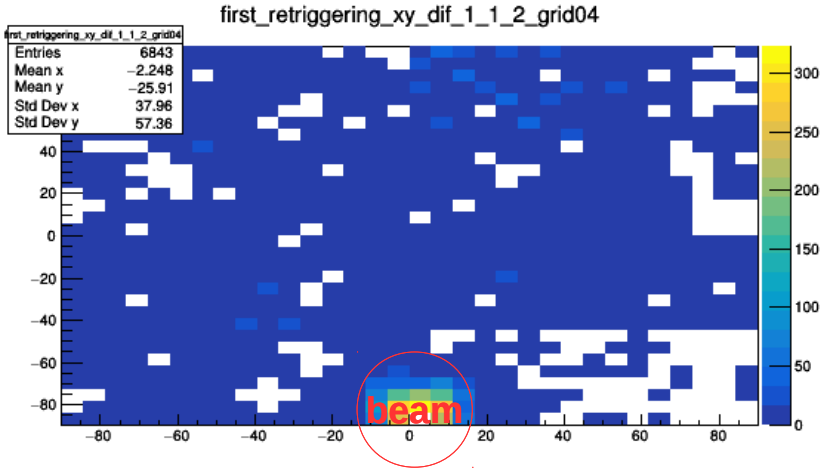


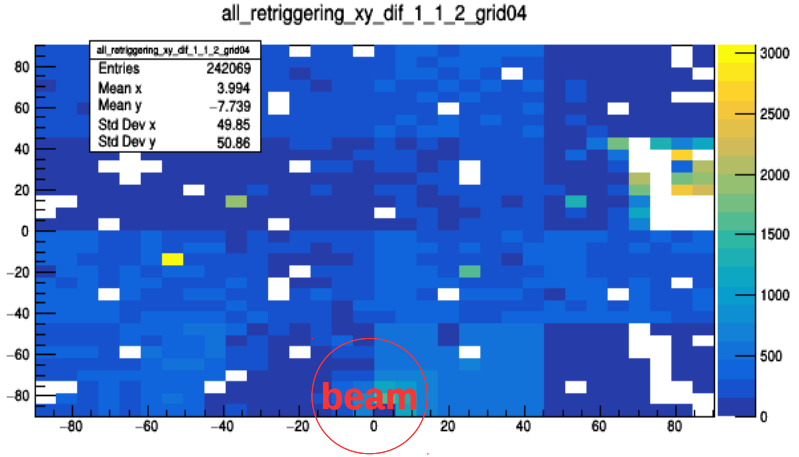


FEV11 Slab16

~0.17 retrig trains / trigger

All/first ~36



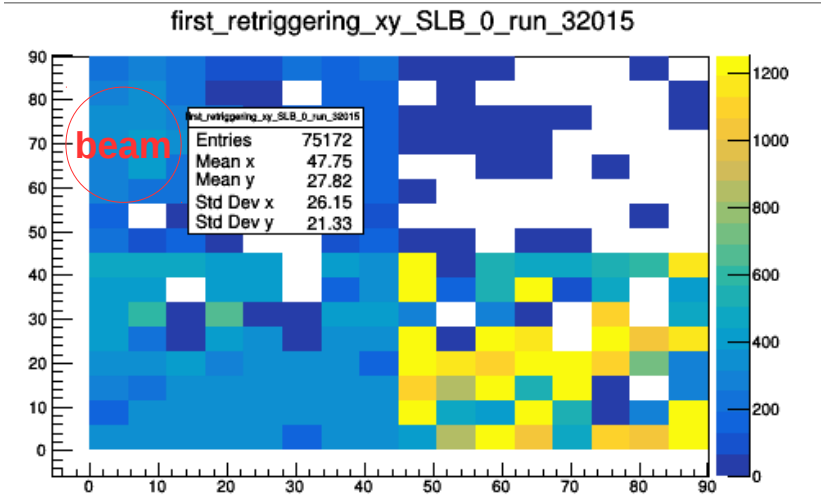


Retriggers:

COBc

~1.05 retrig trains / trigger

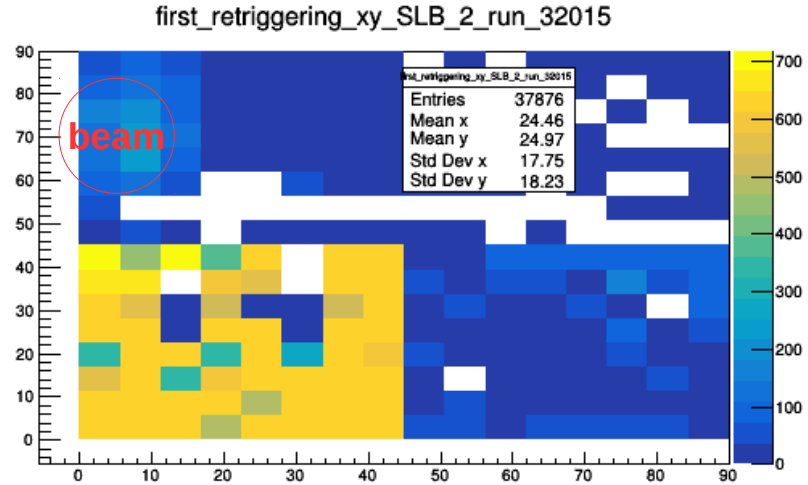
All/first ~4



COBa

~0.4 retrig trains / trigger

All/first ~4

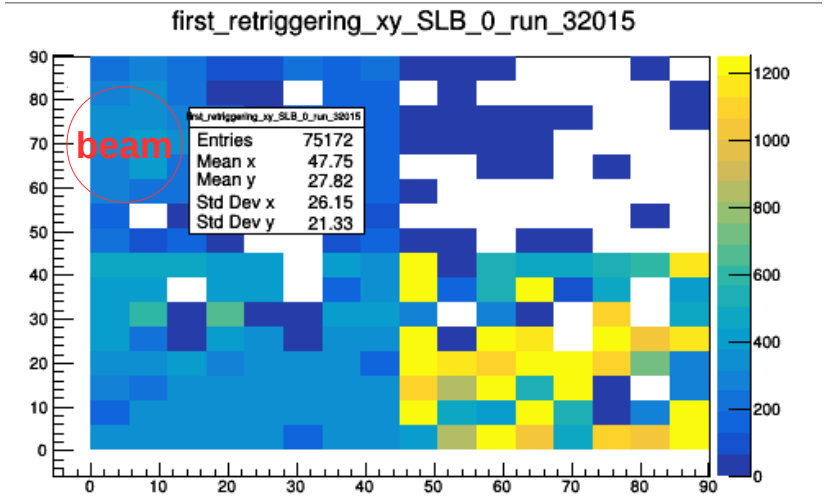


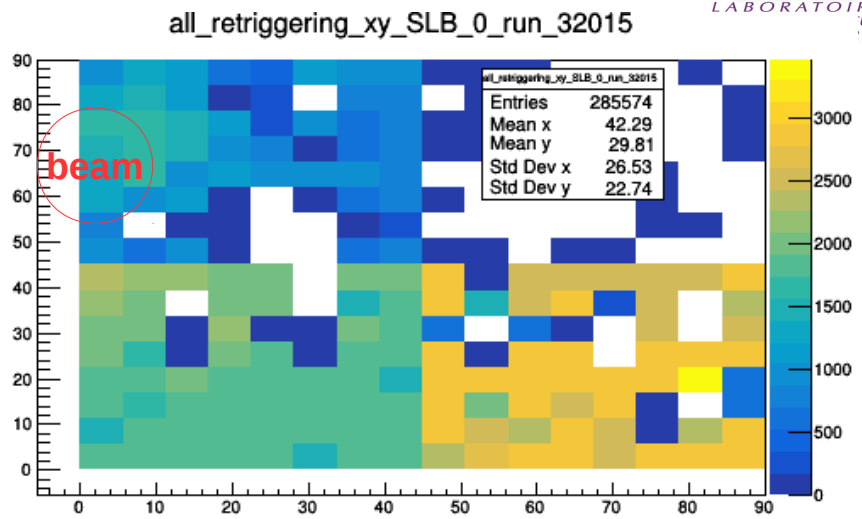
Retriggers:

COBc

~1.05 retrig trains / trigger

All/first ~4

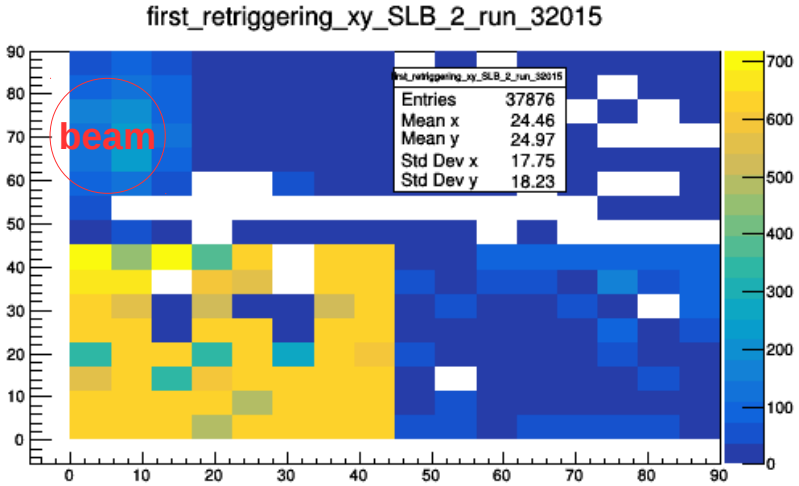


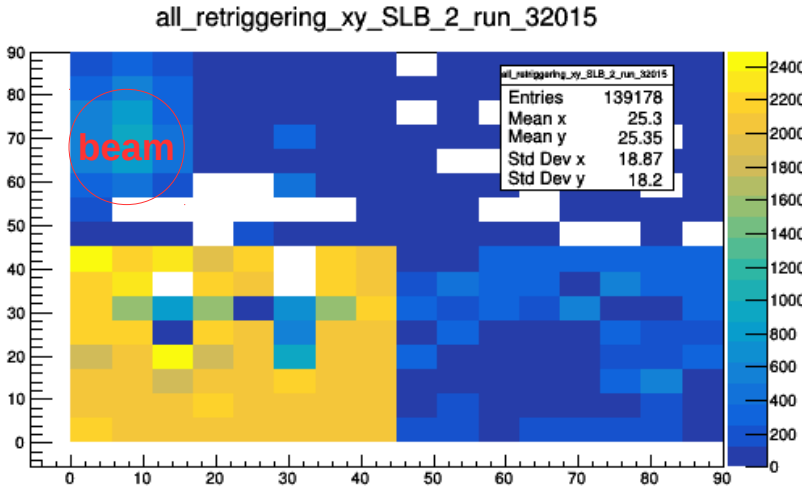


COBa

~0.4 retrig trains / trigger

All/first ~4



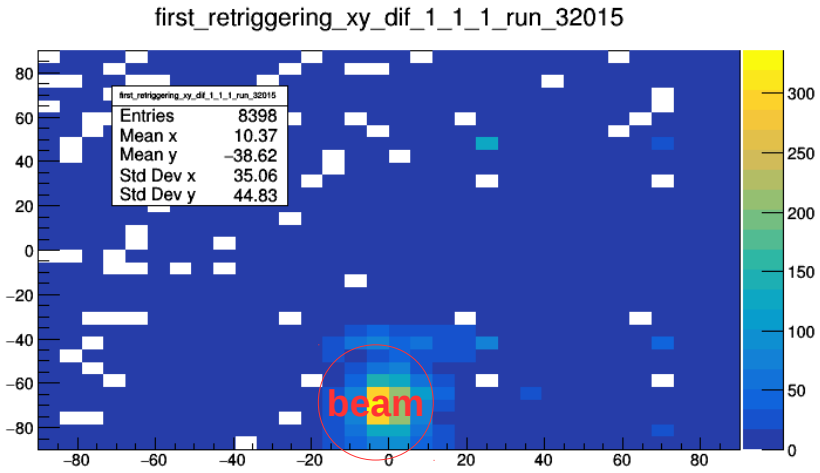


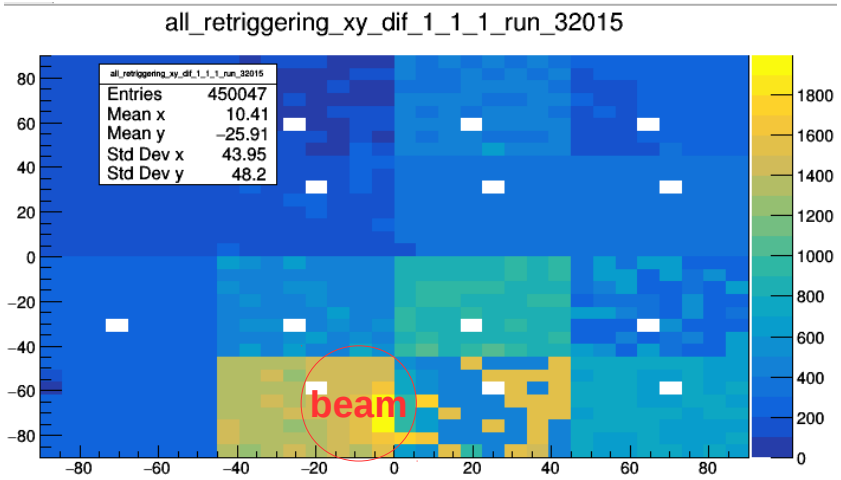
Retriggers: Location (FEV13 P1 vs K1)

P1

~0.2 retrig trains / trigger

All/first ~53

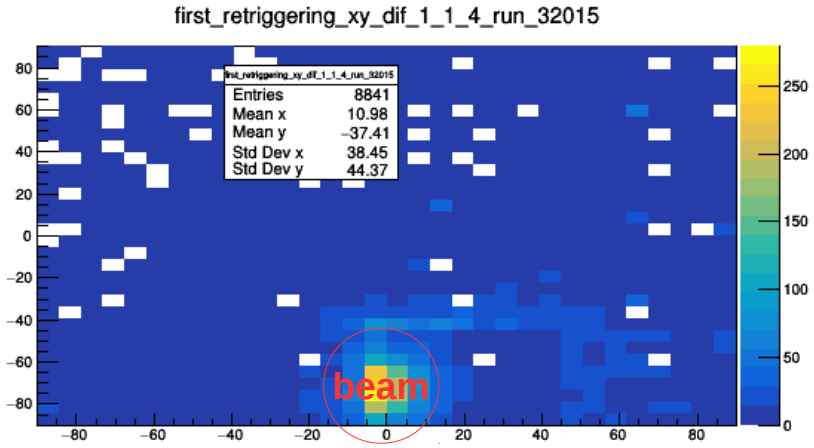


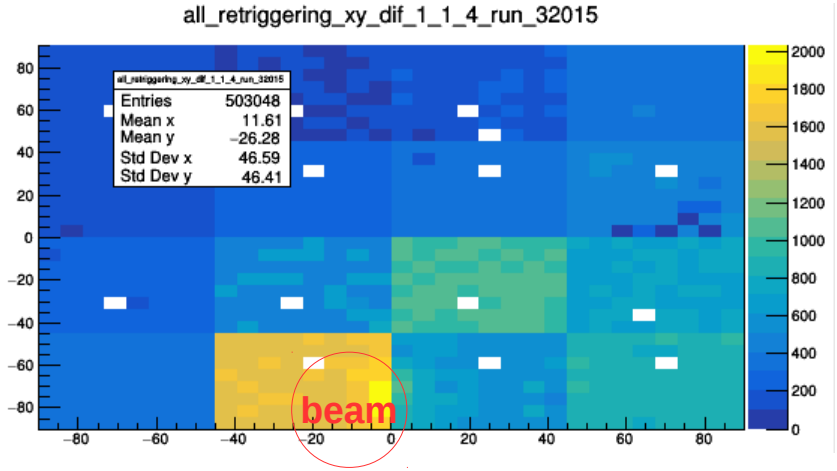


K1

~0.2 retrig trains / trigger

All/first ~57





Retriggers conclusions:

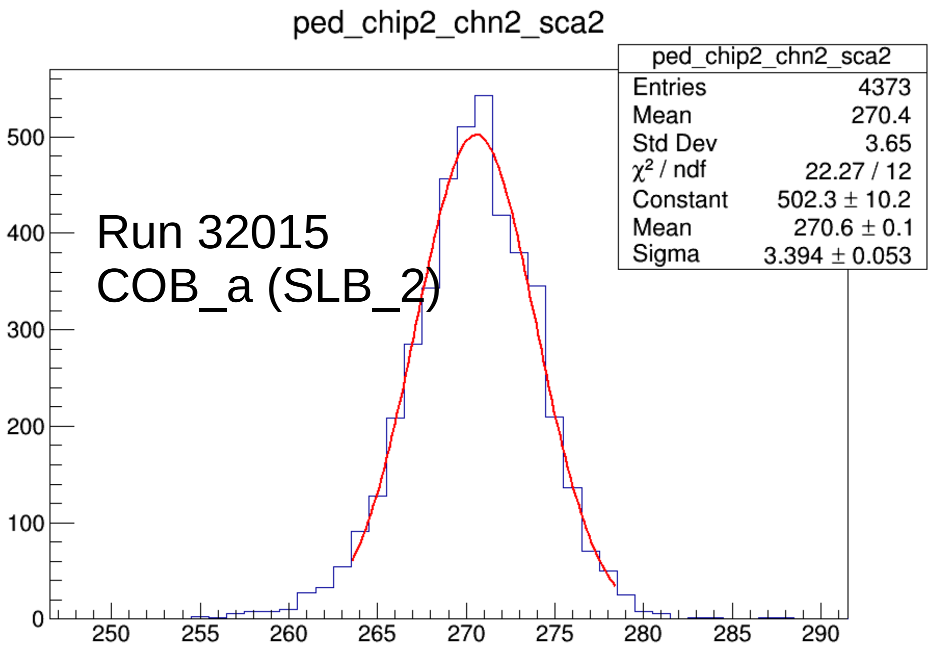
- The COB with cap. Is better than the one without.
- The COB, FEV11, FEV13 all have similar performance but:
  - COB version seems to solve the chn 37 issue
  - COB (with extra decoupling cap) & FEV13 seem to solve the issues near the electronics
  - COB has less retriggers in the beam spot than the others (~1/20 to be compared with ~1/10)

BUT !! Many of the retriggers trains start from the neihgbour chip

- FEVs has less retrigger trains (0.2 per trigger) than the COB (0.4 per trigger) but the trains are larger and involve a larger number of channels and chips.
  - The ratio of first / all in the FEV11 was 36, in the COB was 4 and in the FEV13 was 55

Pedestals

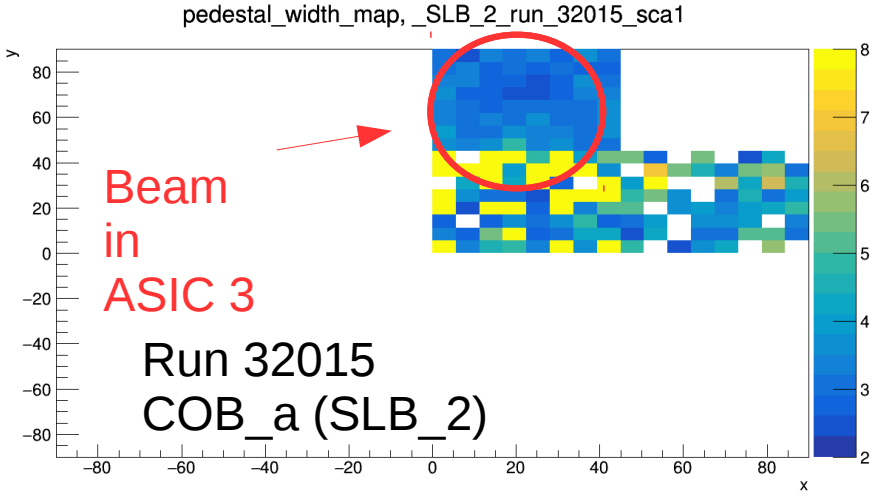
Pedestal calculation

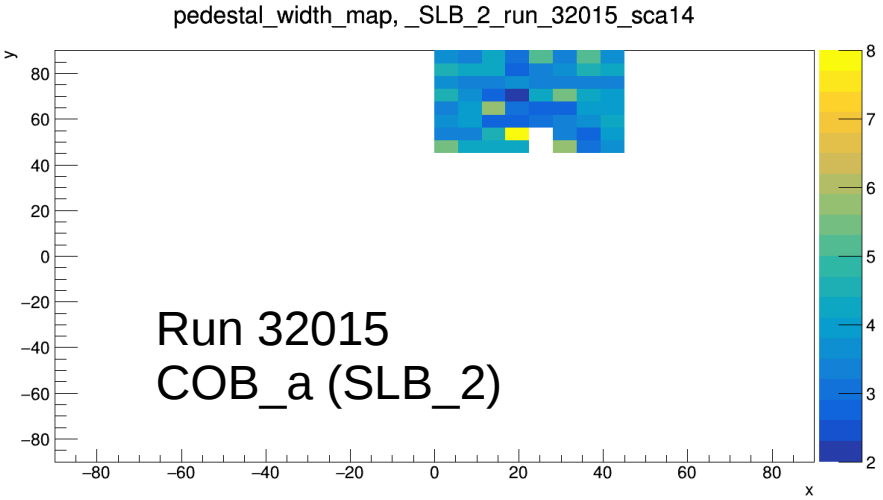


- After event filtering.
  - Retriggers and plane events are tagged in the root files using the badbcid variable (if badbcid !=0 → “bad event”)
- Check the charge (HG) of non triggered cells.
  - Always in self-triggering mode
- Pedestal = Mean (gauss fit)
- Width = Sigma (gauss fit)
- Histograms are saved in root files, and fit values in a txt file

```
#pedestal results (fit to a gaussian) remove channels/sca with two pedestals peaks from the analysis : _SLB_0_run_32015
#chip channel ped0 eped0 widthped0 ped1 eped1 widthped1... ped14 eped14 widhtped14 (all SCA)
0 0 0 0 0 0 0 0 278.435 0.327673 3.44518 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 1 0 0 0 0 0 0 275.49 0.277462 3.13925 275.677 0.255243 3.33528 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 2 0 0 0 0 0 0 279.953 0.195636 2.42415 279.759 0.175012 2.26449 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 3 0 0 0 0 0 0 277.342 0.262307 3.44113 277.17 0.252224 3.36281 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 4 0 0 0 0 0 0 285.095 0.339535 3.66054 284.865 0.243777 3.09483 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
```

Pedestal calculation: pedestal width

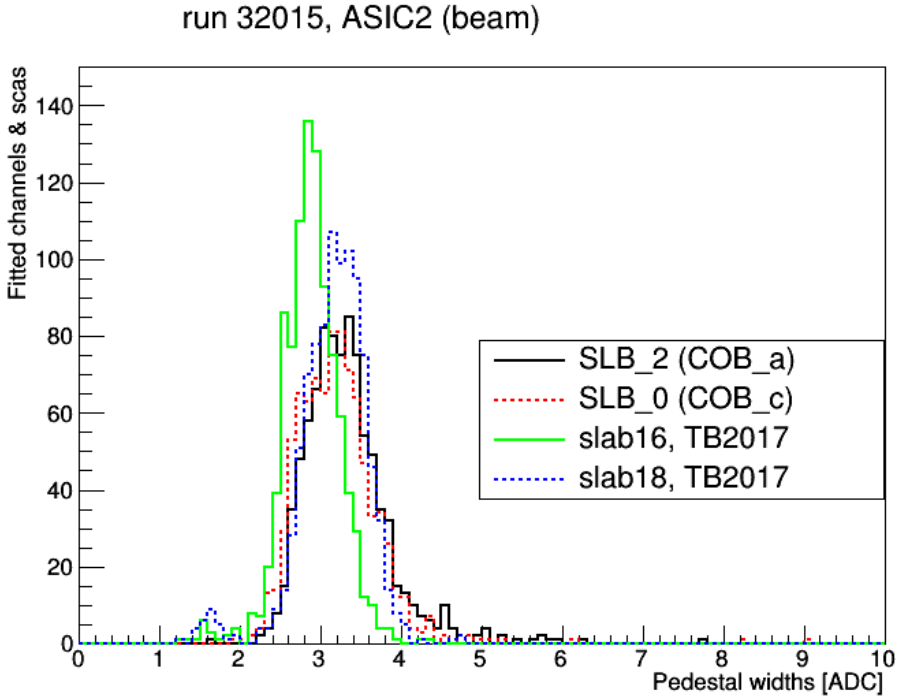


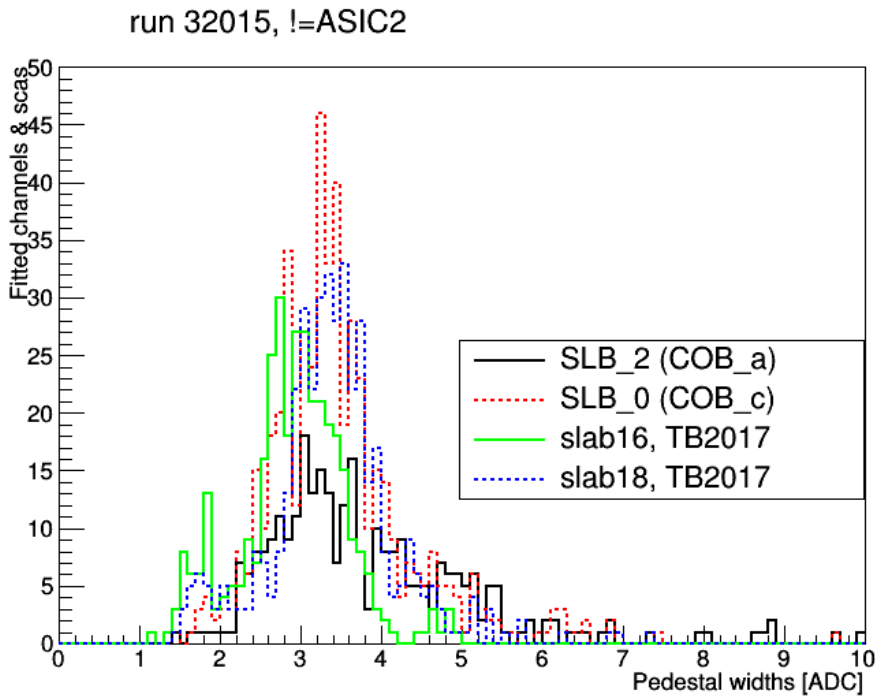


- SCA == 0 is usually empty
  - (filled by noise burst in bcid==0)
- Pedestal distributions are always better calculated in the chip that has real triggers.
  - The others chips have real noise + retriggers… which may shift the baseline of the power supplies (double peak spectrum).
- This happens for all board and front end types
  - A comparison is shown later.
- Next slide: calculated pedestal width for all channel and SCAs in different slabs.
  - SLB are compared with FEV11DESY2017 (MIP run at ASIC 2)
  - FEV13 are compared with FEV11DESY2017 (MIP run at ASIC 13)

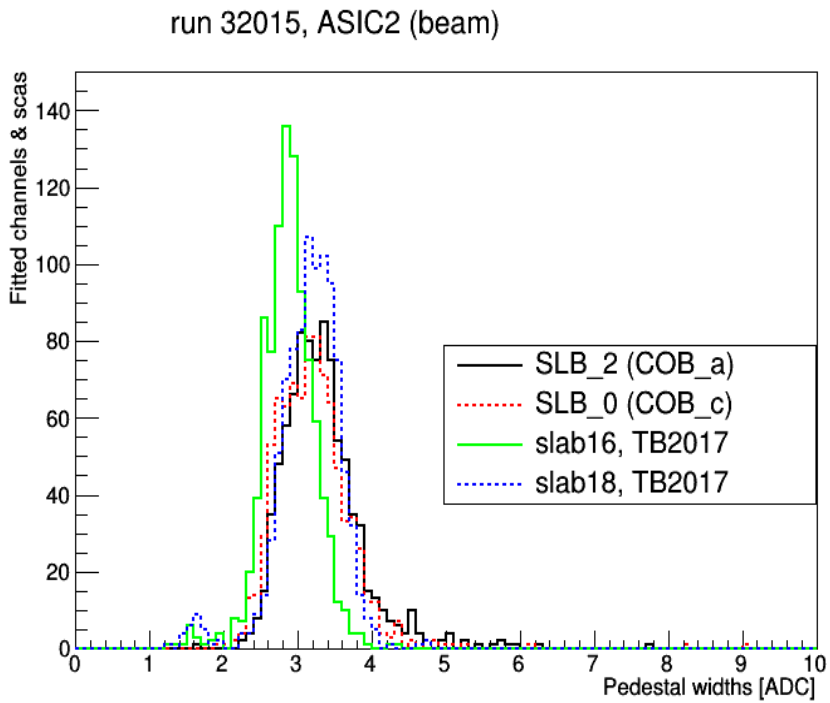
Pedestal calculation: width

- COBs vs FEV11 (2017). Only considering ASICs 0-3
  - Similar width averages (slab16 has lower noise i.e. lower average of the distribtuion of the widths)
- General Wide spectrum behaviour for ASICs far from the hit.
- In general: COBs and FEV11 (equivalent run in 2017) seem very similar in pedestal width terms.



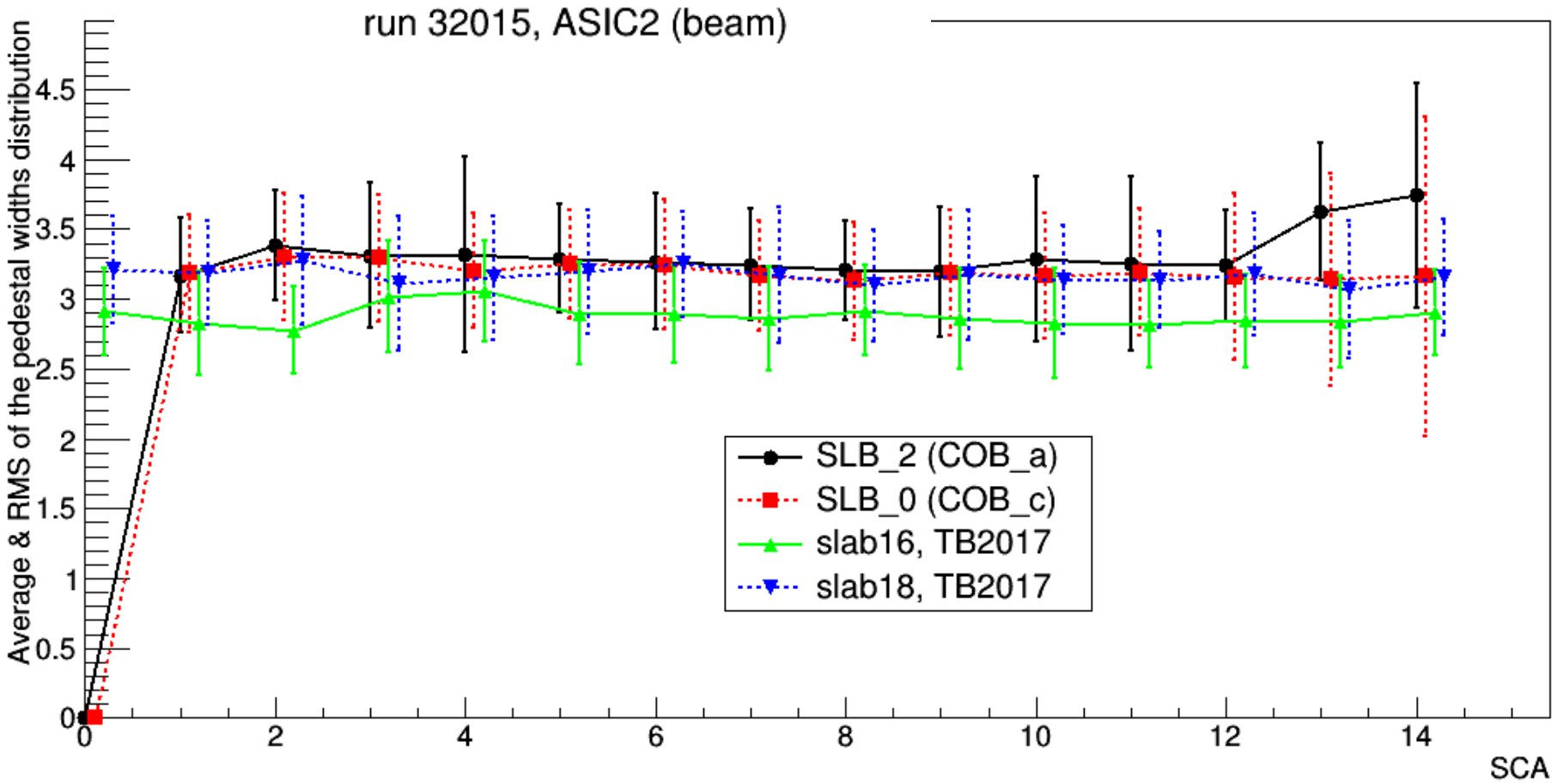


Pedestal calculation: width



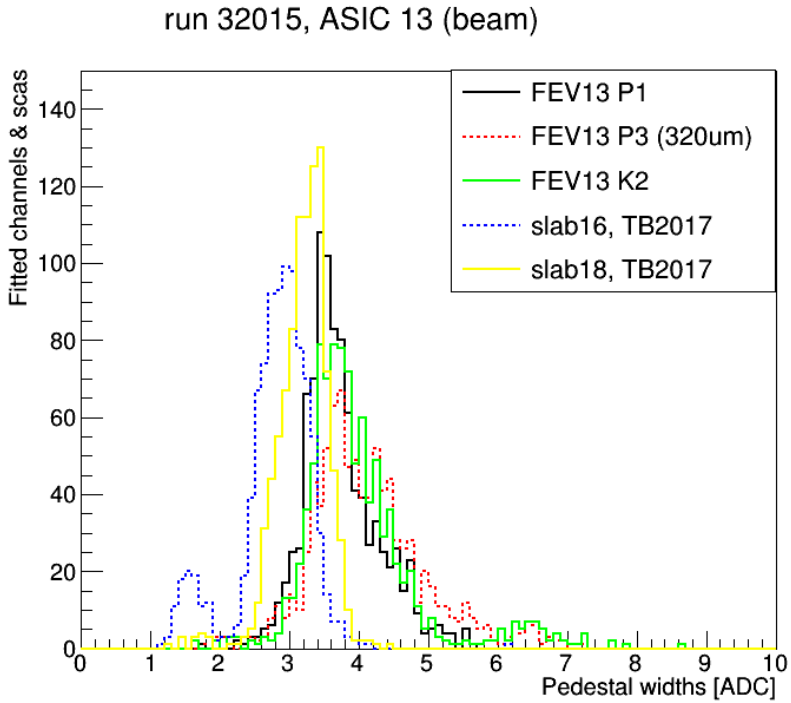
- This is for all SCAs together.
- What if we calculate the average and RMS of each one of these distributions in an SCA basis?

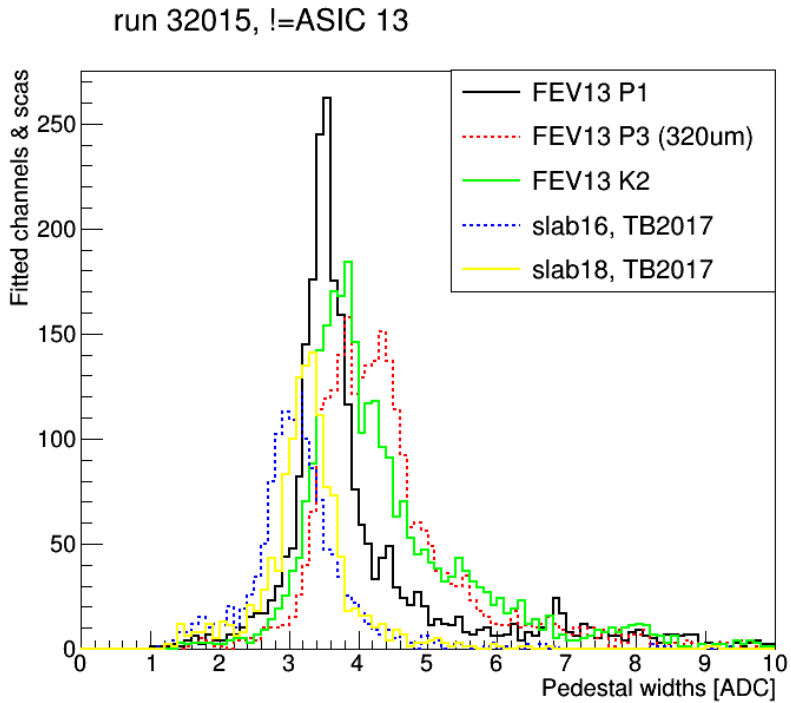
Pedestal calculation: width



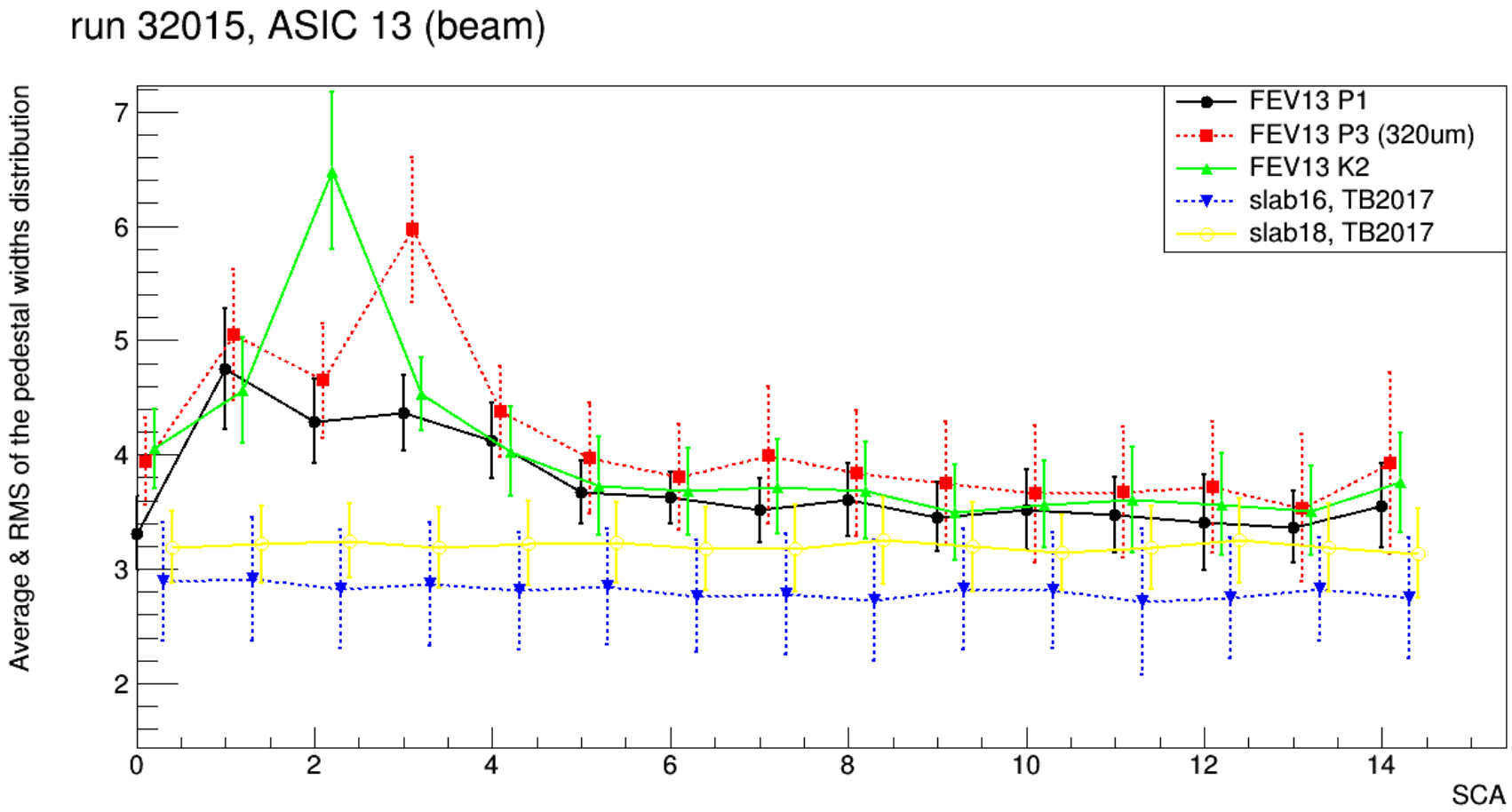
Pedestal calculation: width

- FE13 vs FEV11 (2017, similar run).
- As before, similar behavior between the new and old PCBs.





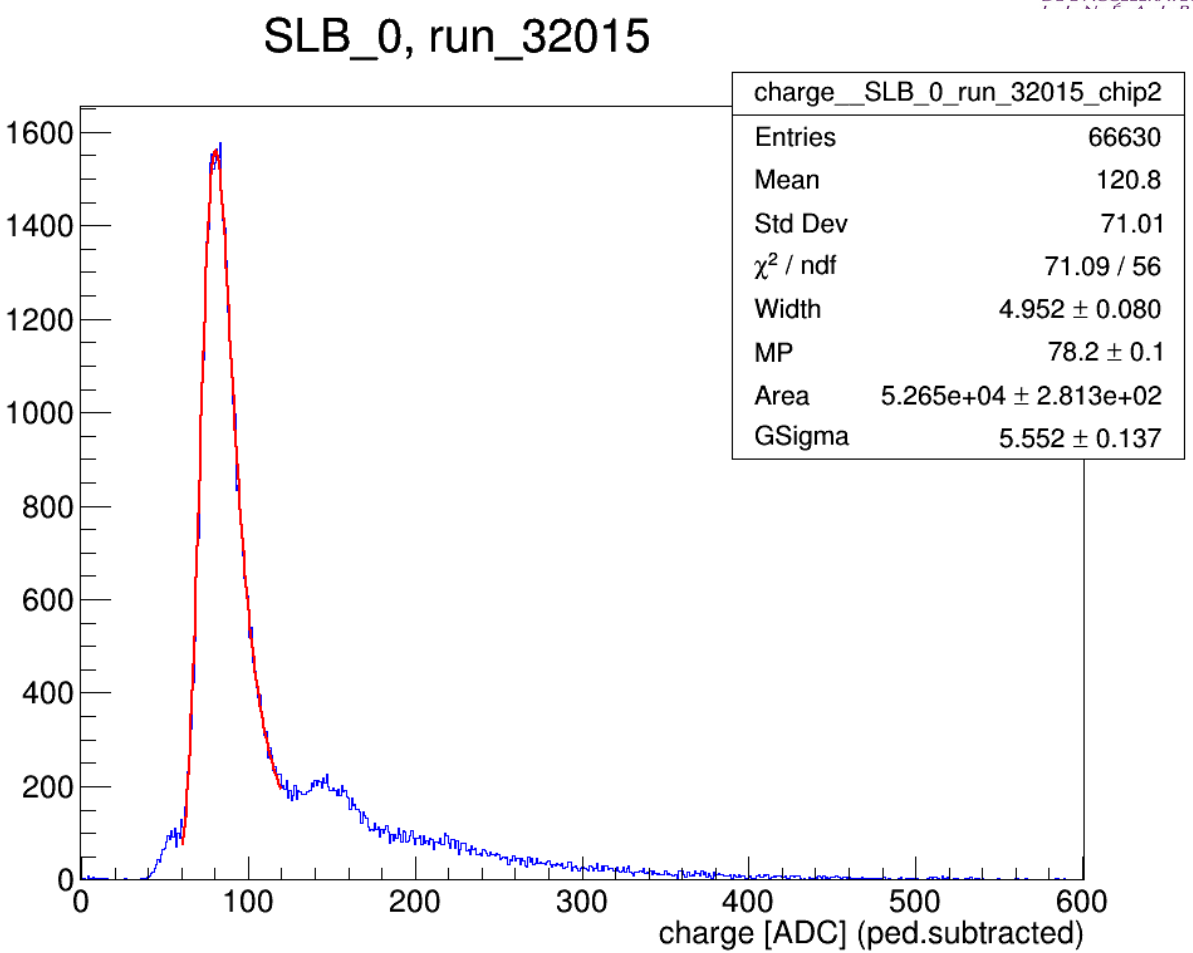
Pedestal calculation: width



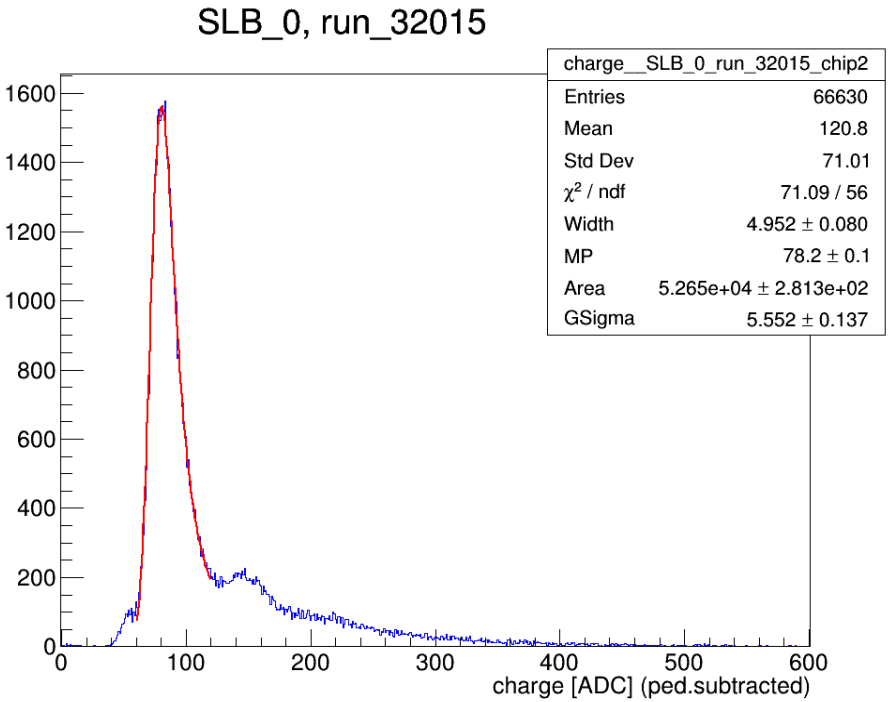
MIP signals

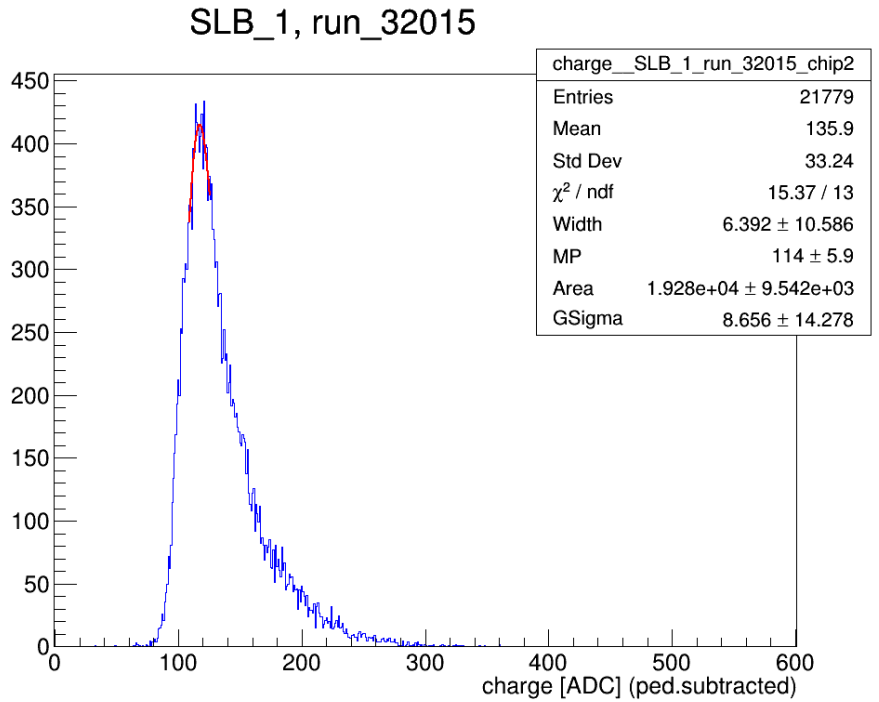
MIP calibration

- Pedestal subratction.
- **MIP spectrum integrating all cells** in ASIC 2 (SLB systems) or ASIC 13 (FEV13 systems)
- FEV11 TB2017:
  - 320um, MIP at ~ 63ADC
- If 500um → MIP is expected at 98ADC
  - Is the ASIC hold value well optimized? To be checked in the laboratory.
  - The gain is correct, I.e.1.2pF?
- If Ped_width ~ 3.2 ADC (previous slides) → **S/N~24,5**



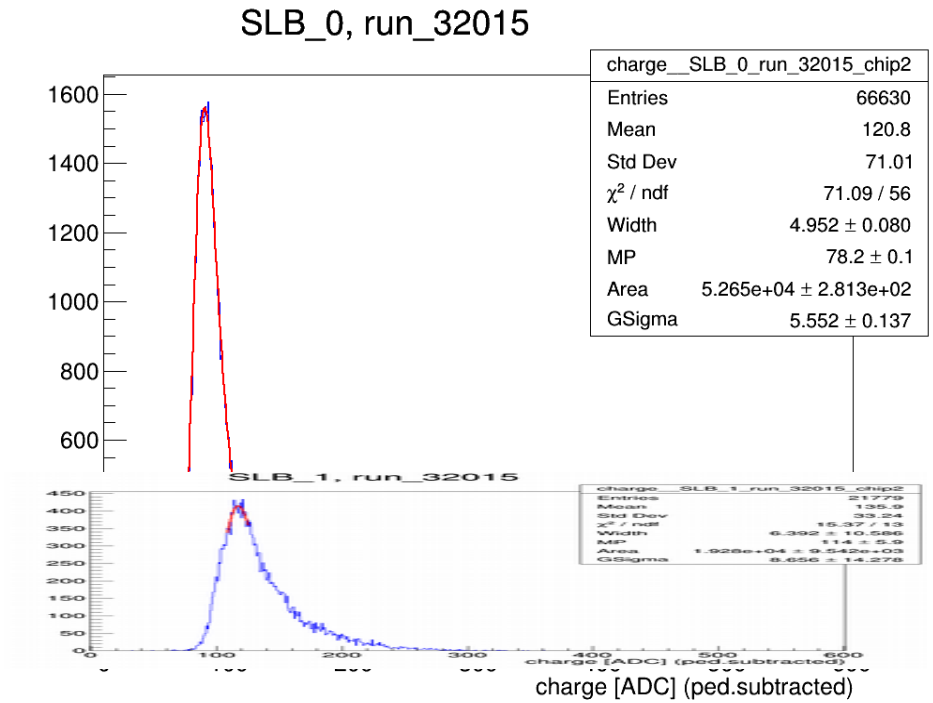
MIP calibration COB vs FEV12

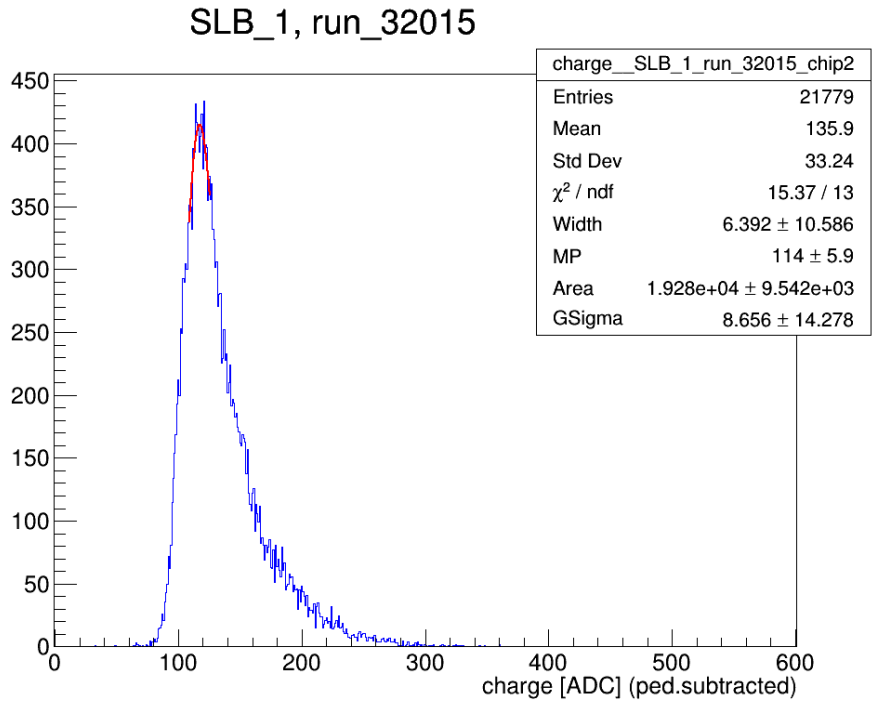




- FEV12 spectrum is strange. It starts only at ~100 ADC.
- It looks like a different threshold + gain configuration → NEEDS CLARIFICATION.

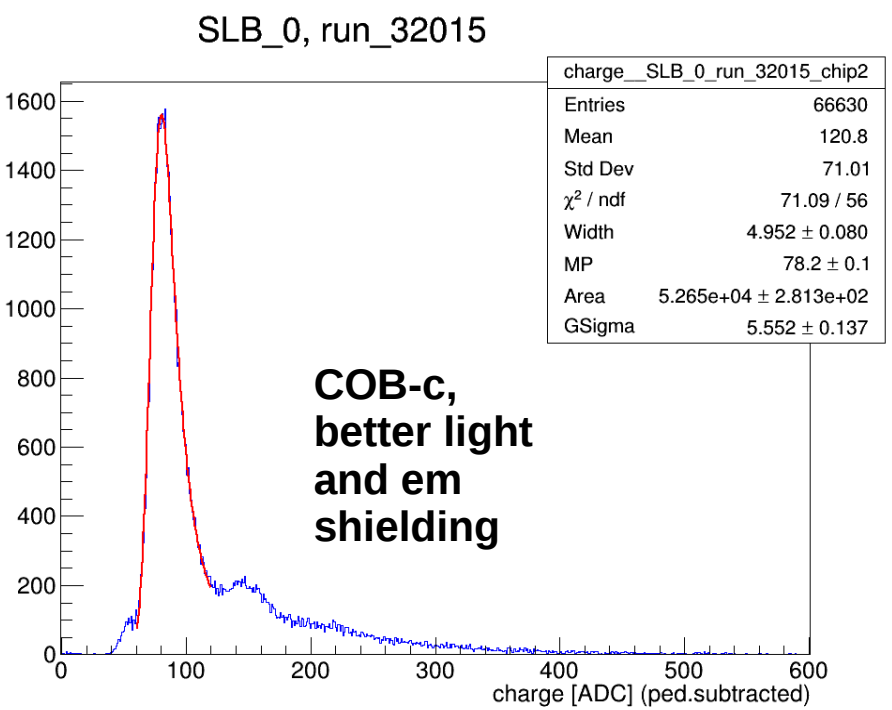
MIP calibration COB vs FEV12

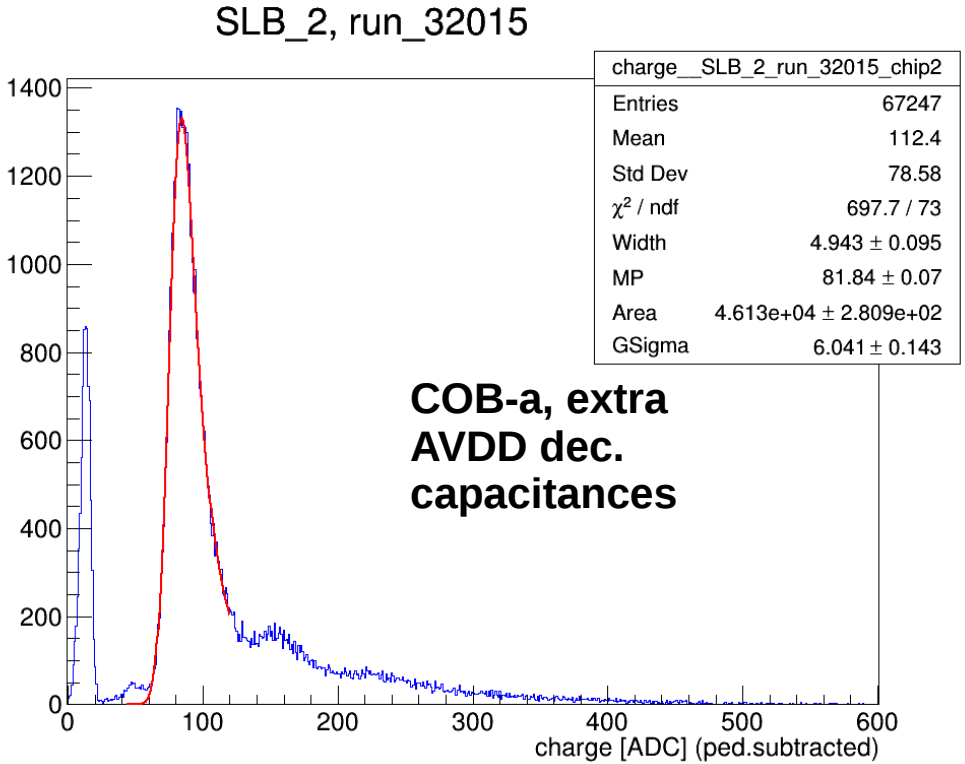




- FEV12 spectrum is strange. It starts only at ~100 ADC.
- It looks like a different threshold + gain configuration → NEEDS CLARIFICATION.

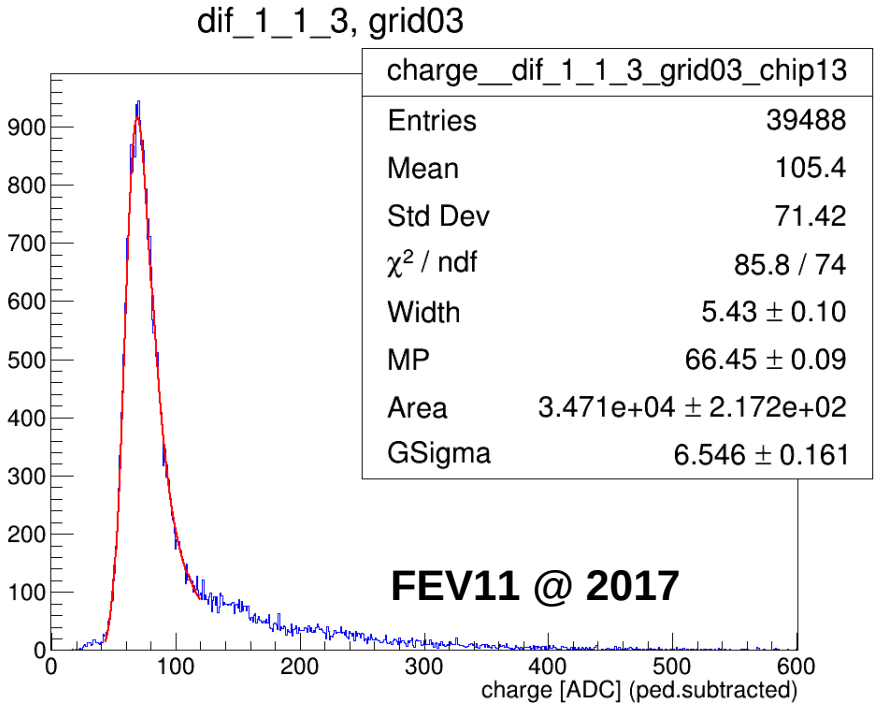
MIP calibration COB-c vs COB-a

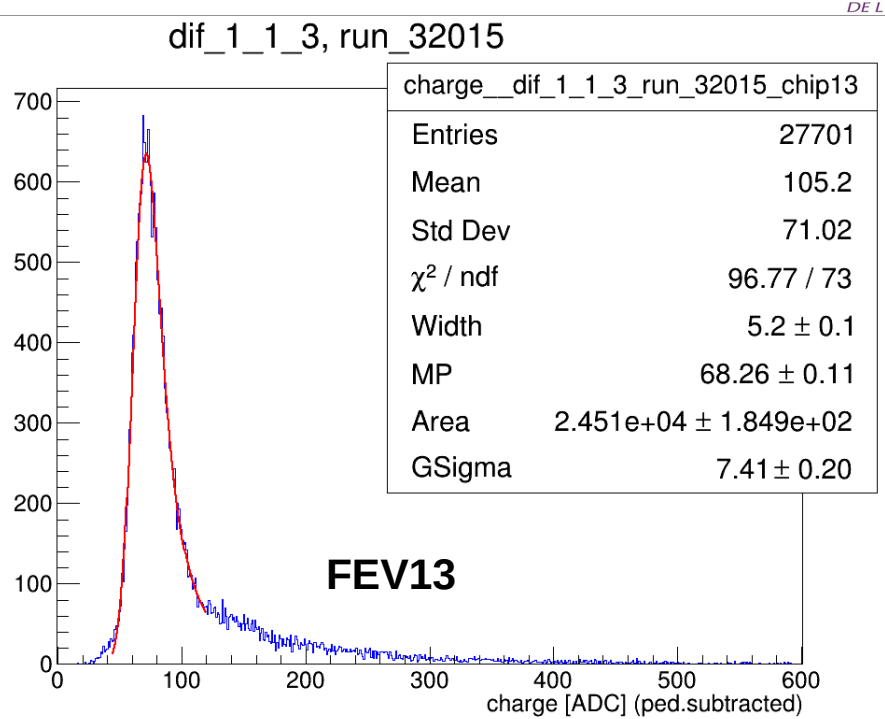




- Comparable spectrums.
- Few noisy channels in the COB-a (peak at 0)
  - optimizable

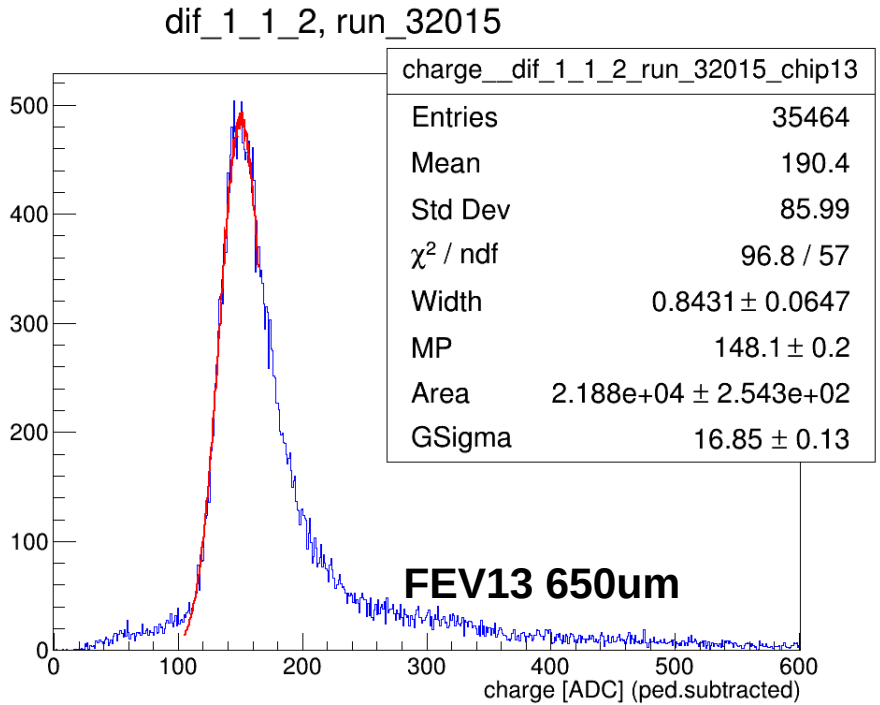
FEV11 vs FEV13 (320um)

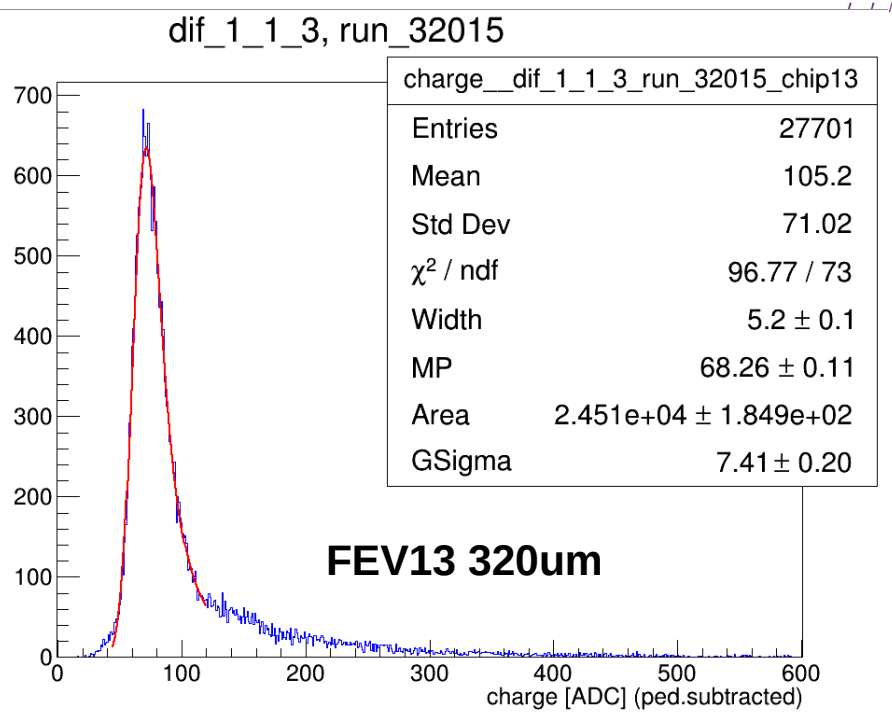




- 320um is well compatible with FEV11 TB2017 expectations.
  - Bit larger Gsigma … due to the slightly larger pedestal width and larger spread between channels?

FEV13 650um vs FEV13 320um





- MIP peak at a bit greater position than expected: 148 ~ 2.2 x 68 DAC

Summary

- The COBs perform as good as all the others PCBs (but with minimal extra components for noise filtering)
  - Decoupling capacitances in the COB are GOOD.
- We still need to understand what happened with the configuration of the FEV12 during the second week.
- COB, FEV11, FEV13 seem to have all similar performances, with slighlty different strengths and weakneses.

- We need to see the evolution of the FEV12 & COB boards now after long time has passed since the gluing.
  - It is also important to clarify the “FEV12 issue”

Back-up slides

ID	Date	Author
2162	Sat Jul 6 14:55:53 2019	Taikan, Yu, Ludovic, Vincent, Adrian

End of the beam test, at 14.30. Start dismounting.

Run numbering:

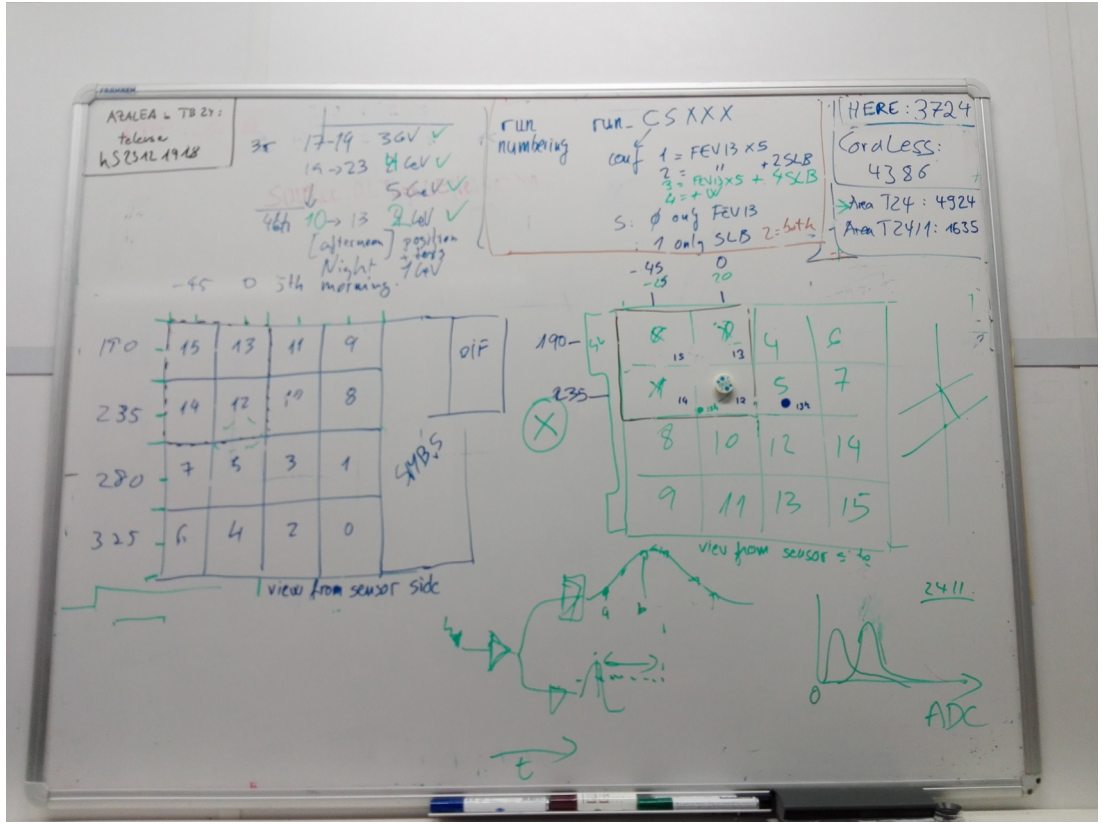
run_CSXXX

- C= configuration
  - 1: only 5 FEV13 in the box
  - 2: 5 FEV13 + 2 SLB (0 and 3) in the box
  - 3: 5 FEV13 + 4 SLB in the box
  - 4: 5 FEV13 + 4 SLB in the box + tungsten plates
- S= system in the DAQ
  - 0= only FEV13
  - 1= only SLBs
  - 2= all

Data location. In the EOS (CERN)

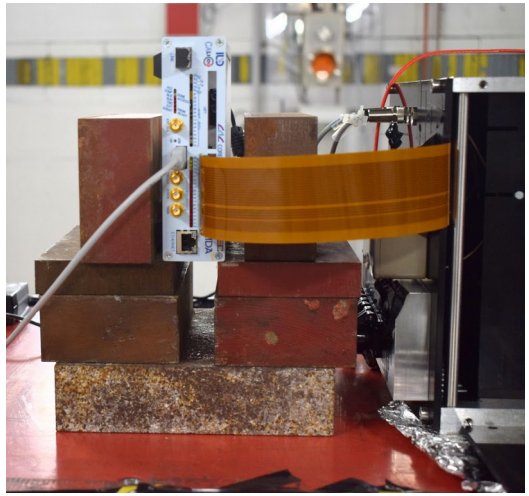
/eos/project/s/siw-ecal/TB2019-06/

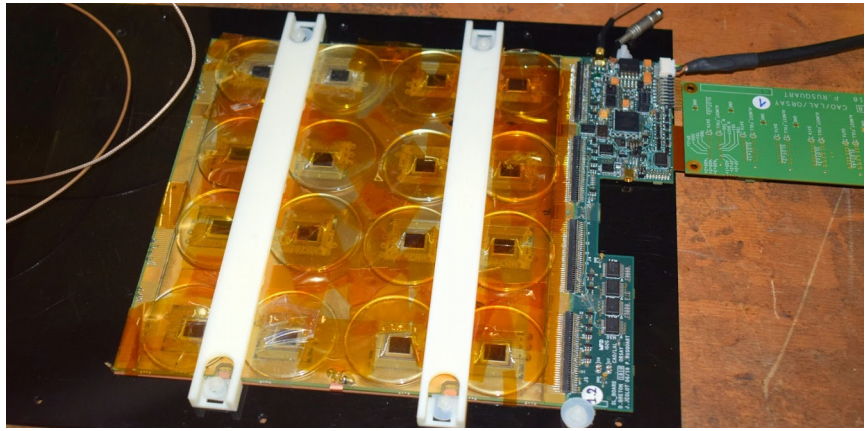
Root files with built events for the common runs are to be prepared.



SLB based DAQ

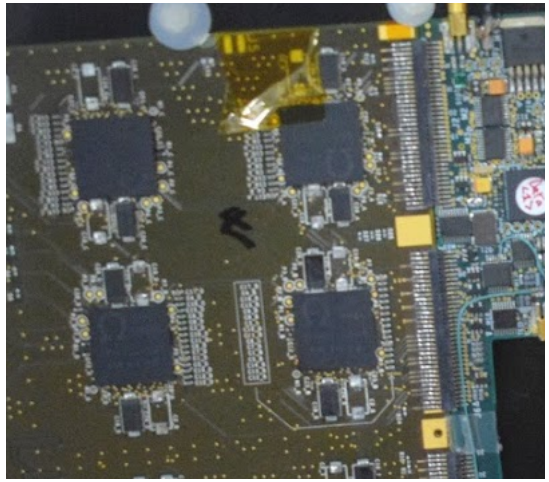
- New Ultra compact Detector Interface (SLboard + Core mother/daughter system)
  - See https://agenda.linearcollider.org/event/8109/contributions/43626/
- Table top system: tests with USB possible with a laptop + 4 V power supply.
- Core Mother / Daughter able to deliver clocks, slow control parameters and control the DAQ (handle of start/stop, busy, data merging)
- DAQ software written in LabWindows (National Instruments but C-based).





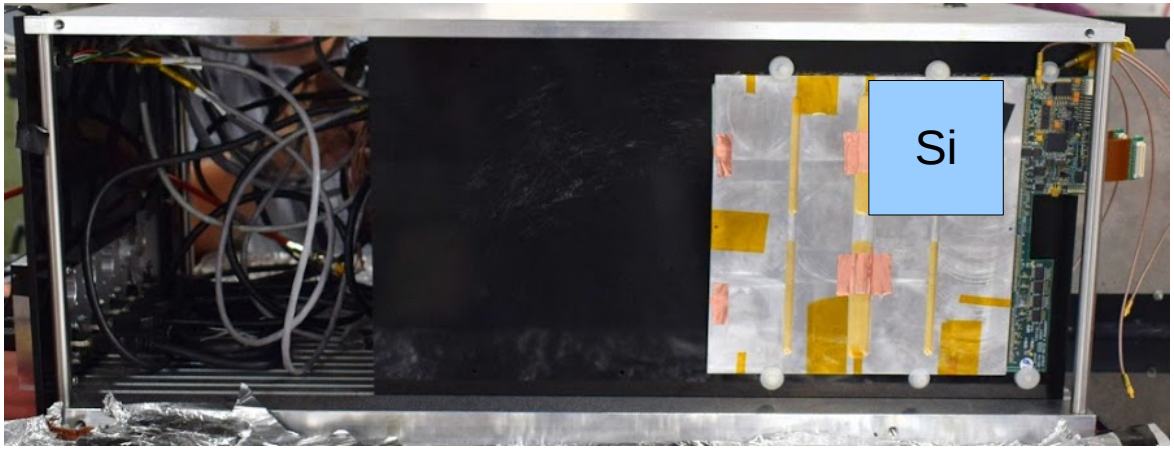
SLB based slabs

- Two COBs with different amount of extra components (i.e. AVDD, DVDD external decoupling capacitances)
  - COB_a started “naked” and ended up with 4 CMS 140uF capacitances
  - COB_c with zero extra components (but an aluminum plate used as a chip protection used during the gluing).
- 2 FEV12 fully equipped with all components



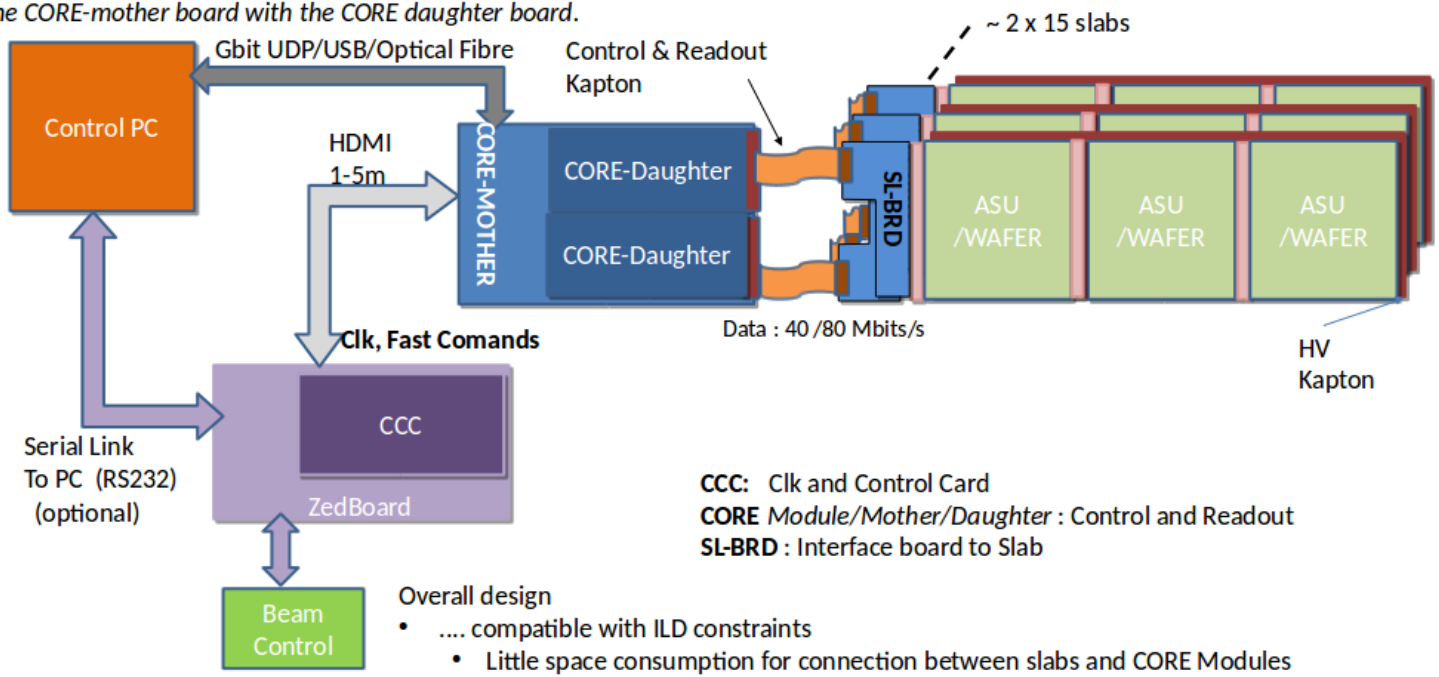
SLB based slabs

- Wafer gluing made at LPNHE. Last board received just the week after the beam test. All wafer in the same position.
  - Experts claim that the optimal lead time to properly stabilize the polimerization of the glue is O(1month). We expect slightly high noise levels, specially at the beginning of the beam test.
- The COB in the current design is not suitable for the automatic gluing procedure using aspiration pipes to mechanically stabilize the modules.
- This was fixed by fabricating a simple mask to transport the vacuum from the pipes to the COB.
- In addition, the mask allows to give the ASUs to LPNHE with connectors in place and provides protection to the wires of the SK2a



Global Architecture Scheme

DIF system for the SiW ECAL is shown with the SL-board, CORE Kapton and the CORE Module consisting of the CORE-mother board with the CORE daughter board.



CCC: Clk and Control Card
CORE *Module/Mother/Daughter* : Control and Readout
SL-BRD : Interface board to Slab

Overall design

- .... compatible with ILD constraints
  - Little space consumption for connection between slabs and CORE Modules
  - CORE Mother can be placed at the forefront of barrel, Daughter between Ecal and Hcal
- ... assures compatibility with other AIDA2020 developments
  => Paves way for combined beam tests (other calos, trackers etc.)
- SL-Board is delivery for AIDA2020 and P2IO/HIGHTEC