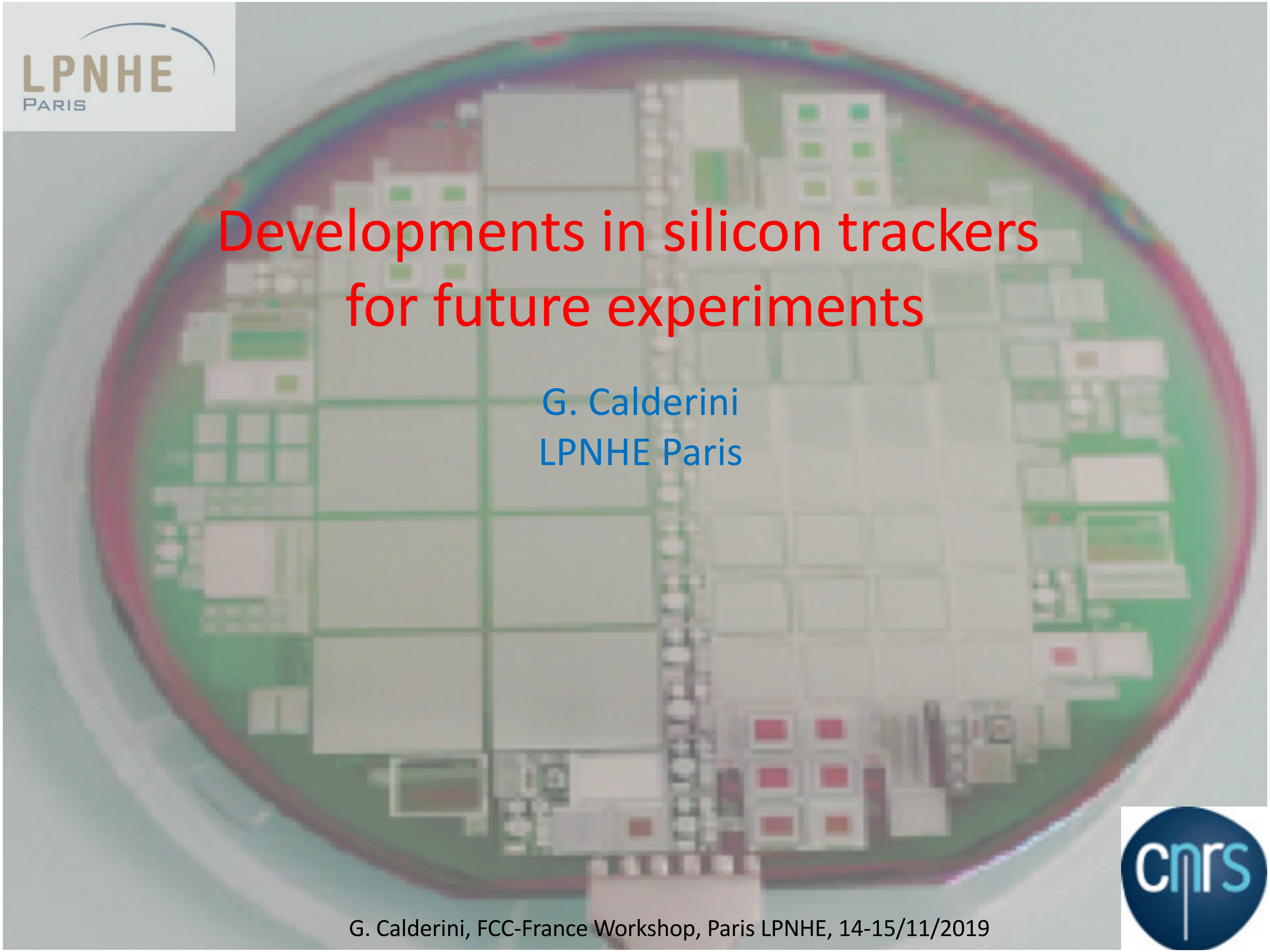


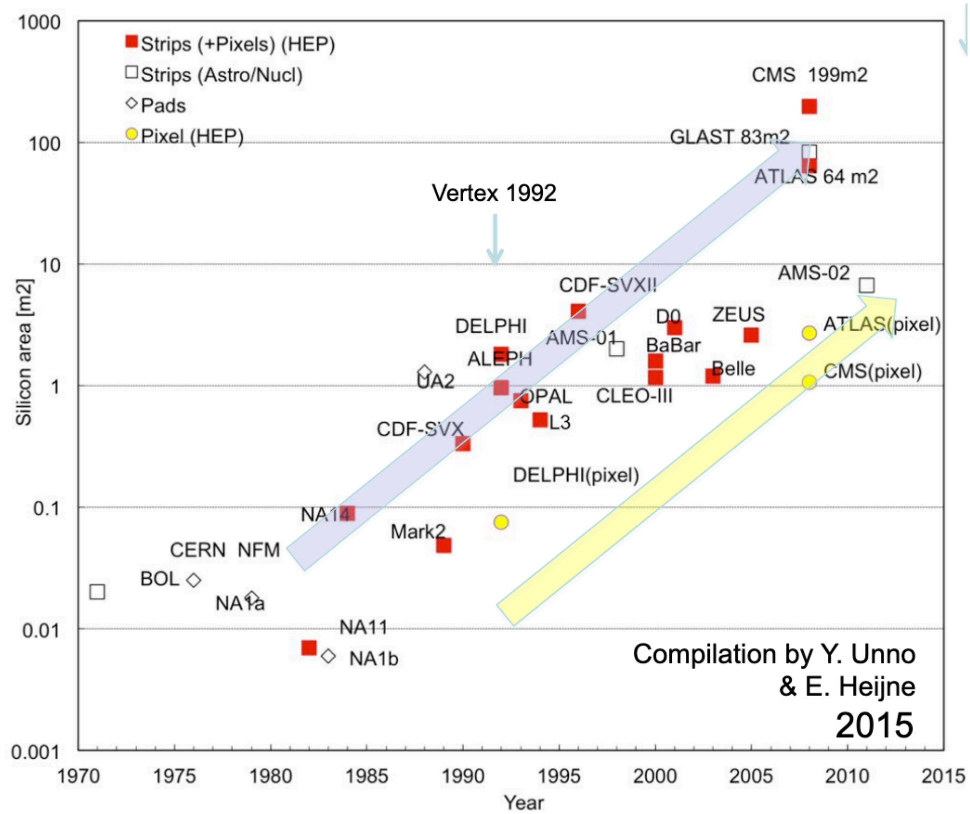
Developments in silicon trackers for future experiments

G. Calderini
LPNHE Paris

Since the '90s, silicon trackers played a crucial role in HEP experiments

Running conditions and detector requirements have changed a lot in these 40 years

Surface has increased exponentially, requirements in terms of dataflow, radiation hardness, material budget, number of channels

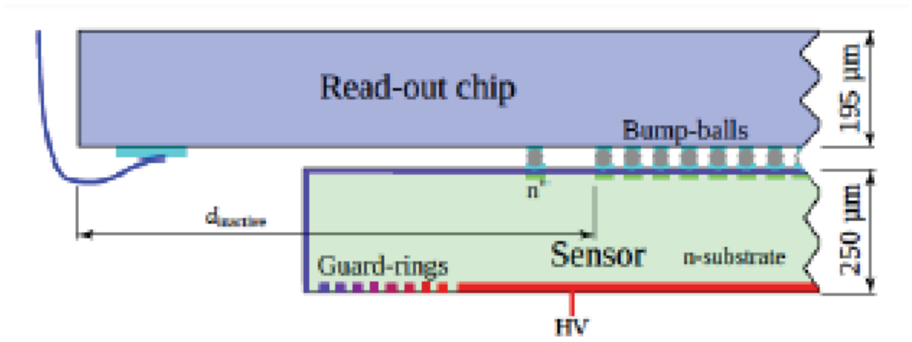


Pixels have been recently the core of most silicon tracking systems, where the running conditions are the most critical

Constant evolution which will continue in the next years for the next experiments

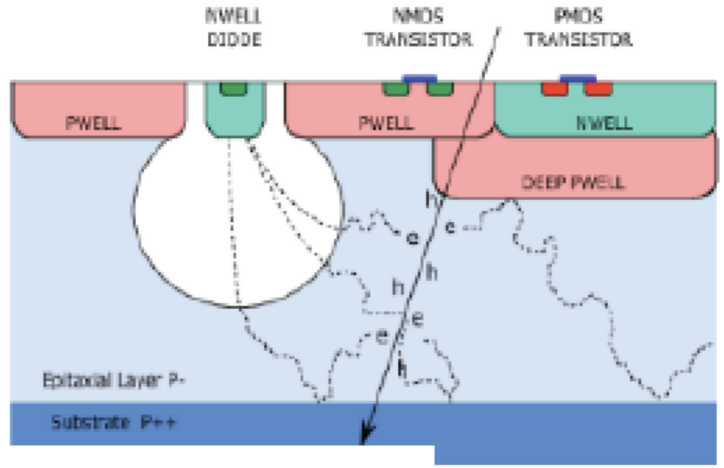
Inner pixel detectors are in general the most constrained part of trackers and went through a rapid evolution

In general, independently of the specific technologies used, they can be classified in two main families



Hybrid

Sensors (whatever technology) and readout chip (whatever technology) are developed separately and interconnected



Monolithic

Single block for sensor and readout system, typically in CMOS process.

Each of the families has intrinsic strong and weak points, often mitigated in more recent developments

Hybrid

Each component (sensor, readout chip) can be developed separately

High resistivity sensors are a good option in terms of radiation hardness

Interconnection is expensive and limits the pitch reduction

Thick in terms of material

Large sensors achievable

Expensive

Monolithic

Industrial process, cheaper for large-scale productions

Charge collection less efficient after radiation damage (mitigated in HVCMOS – DMAPS)

No need for interconnection, small pitch achievable

Light in terms of material

Limited in module size

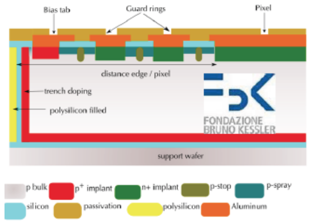
Cost-effective

Recent significant improvements in both of them

The First Family: Hybrid

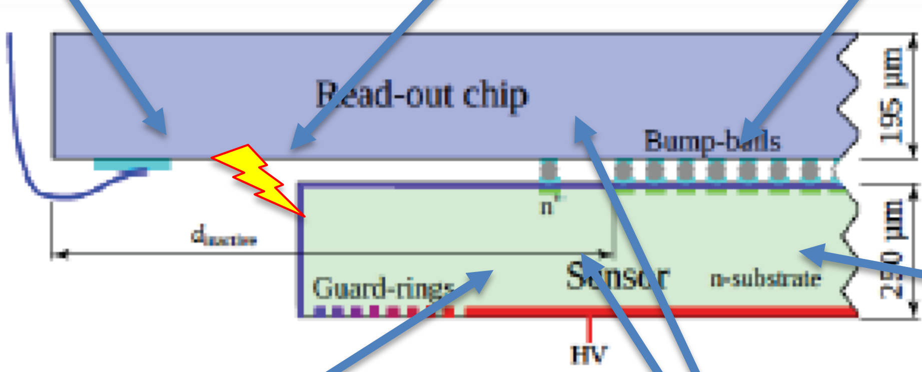
Hybrid detectors: recent highlights

Efforts to improve hit efficiency at the edge (slim-edge / active-edge)

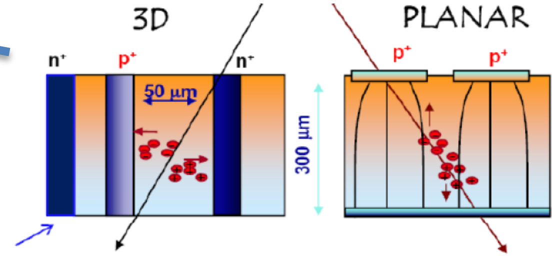


HV protection to avoid possible sparking at the edge

Pixel size/pitch and interconnection technologies

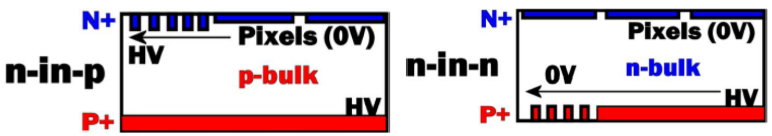


Adaptable sensor technology

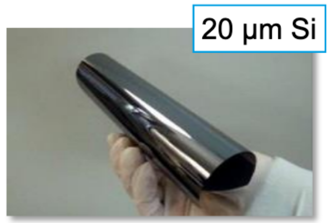


Sensor bulk material

(p-type vs n-type)

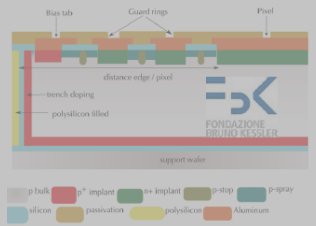


Sensor and FE chip thickness



Hybrid detectors: recent highlights

Efforts to improve hit efficiency at the edge (slim-edge / active-edge)



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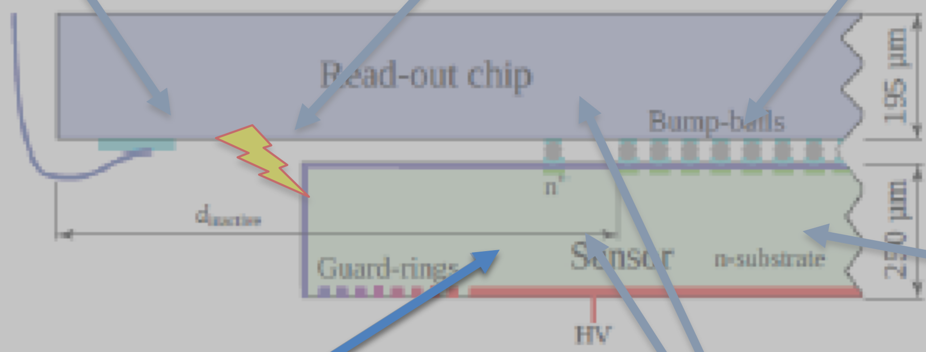
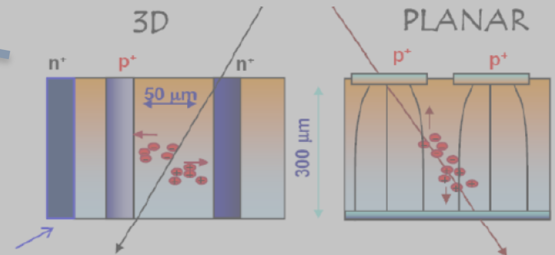


Adaptable sensor technology



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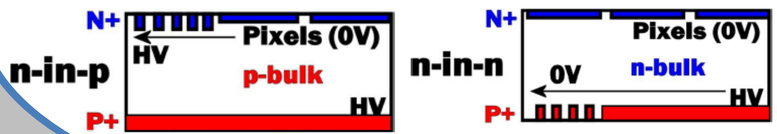
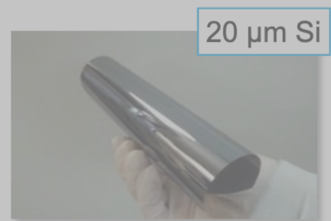
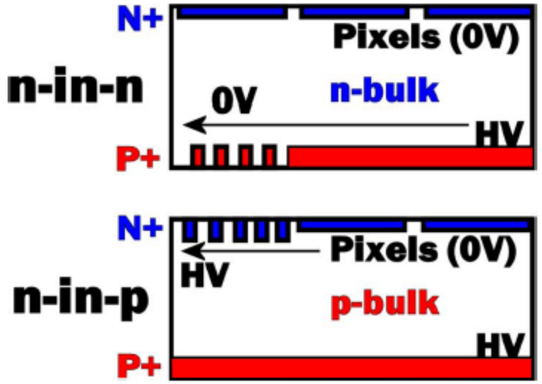


Sensor and FE chip thickness



Sensor bulk material

Option n-in-p already commonly accepted, both ATLAS and CMS will use it for HL-LHC planar pixels



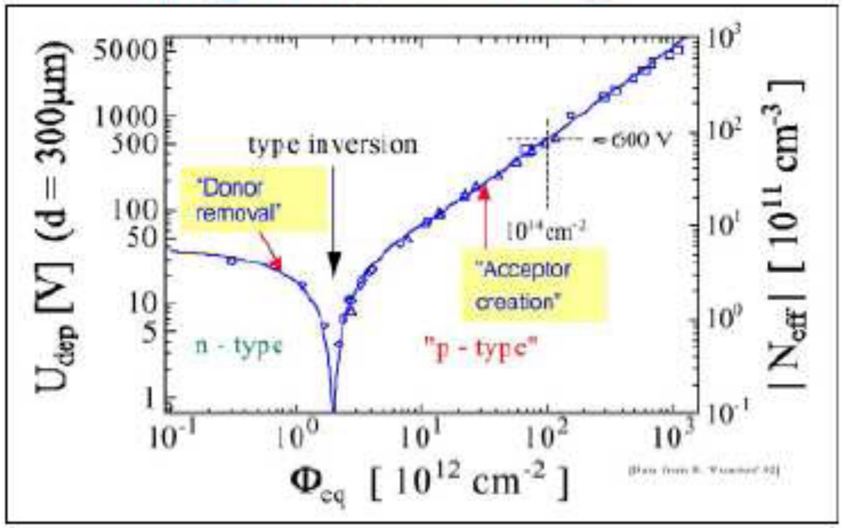
- pixels and guard rings on the same side

➡ Masks needed for the upper side only! Much cheaper than n-in-n

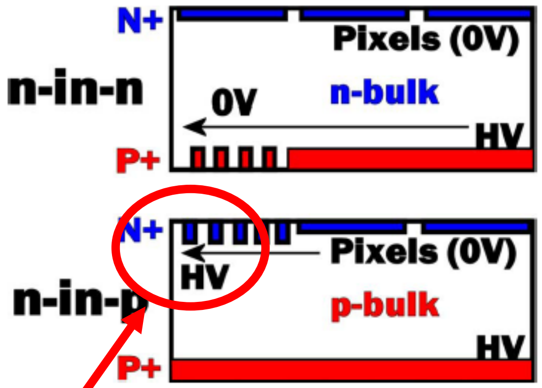
- p-type does not undergo type-inversion with dose

But one non-negligible drawback…

Change of depletion-voltage



Sensor bulk material



Option n-in-p already commonly accepted, both ATLAS and CMS will use it for HL-LHC planar pixels

- pixels and guard rings <u>on the same side</u>

➡ Masks needed for the upper side only! Much cheaper than n-in-n

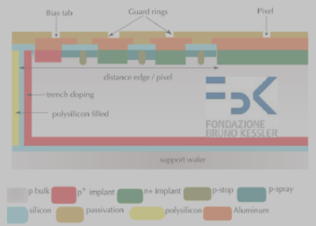
- p-type does not undergo type-inversion with dose

But one non-negligible drawback…

Now the corner of the sensor facing the electronics is at HV, which is at 0 V

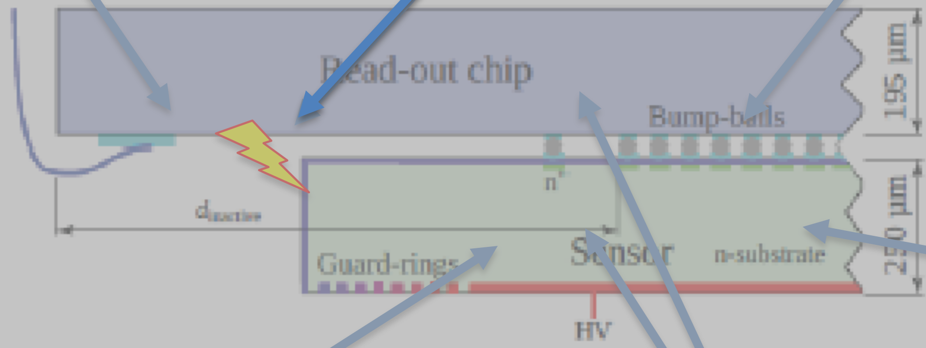
Hybrid detectors: recent highlights

Efforts to improve hit efficiency at the edge (slim-edge / active-edge)

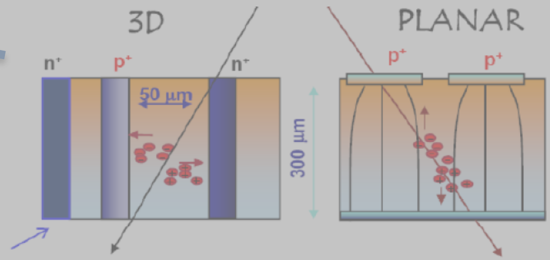


HV protection to avoid possible sparking at the edge

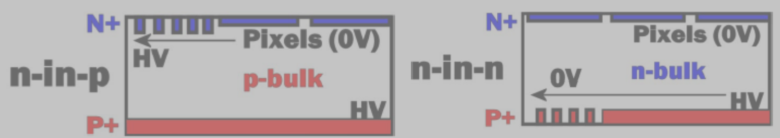
Pixel size/pitch and interconnection technologies



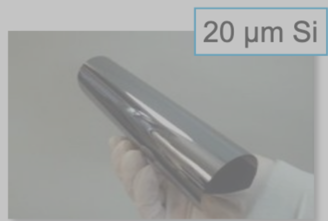
Adaptable sensor technology



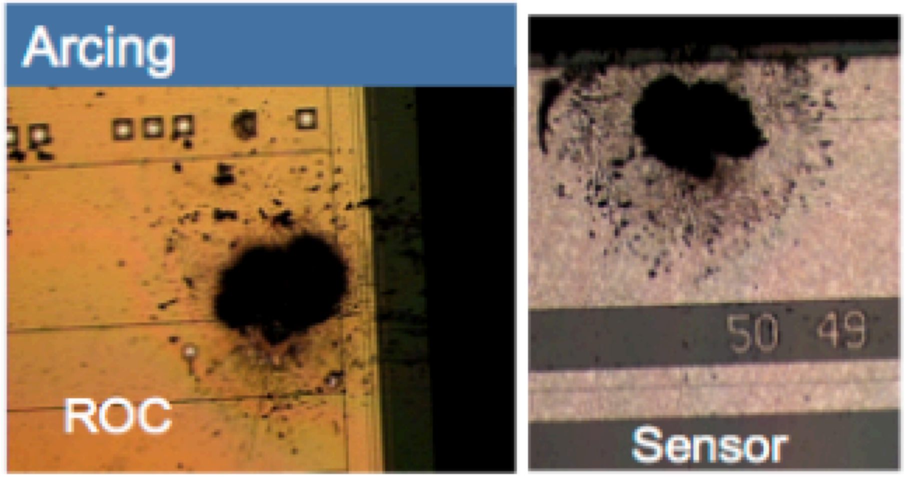
Sensor bulk material (p-type vs n-type)

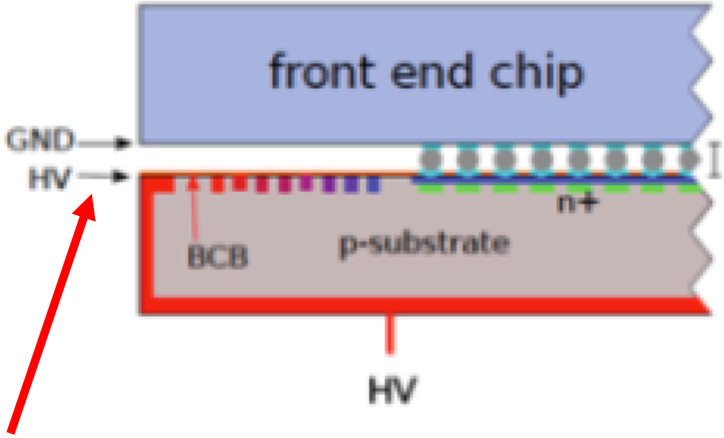


Sensor and FE chip thickness



After radiation, bias voltage may be set at 600-800V





This huge voltage difference generates a strong field across the few μm of sensor-chip separation and can give rise to sparks

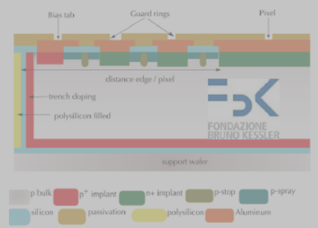
A lot of progress has been made to provide HV protection

- BCB coating deposited on the sensor and/or FE surface with lithography techniques. It can provide an isolation layer.
- Another isolation technique is the deposition of parylene, obtained with exposition to gas atmosphere inside a chamber. Very good isolation results, it also protects the lateral edge. Main drawback is the masking needed to protect everything which must not be coated (contacts, pads, pins, jumpers etc)

Recent studies!

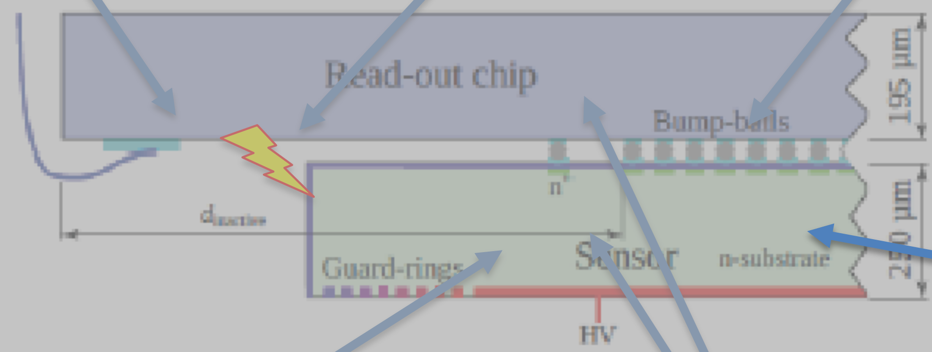
Hybrid detectors: recent highlights

Efforts to improve hit efficiency at the edge (slim-edge / active-edge)

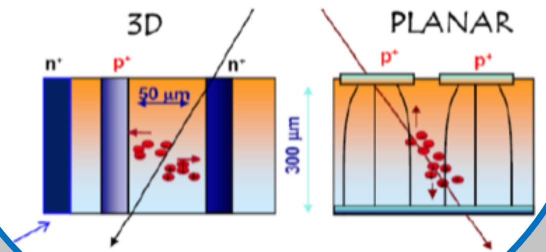


HV protection to avoid possible sparking at the edge

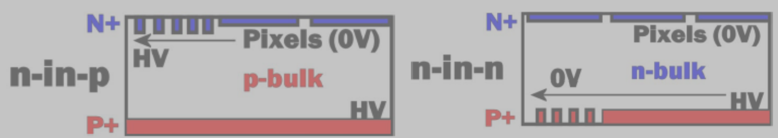
Pixel size/pitch and interconnection technologies



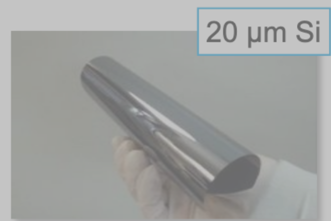
Adaptable sensor technology



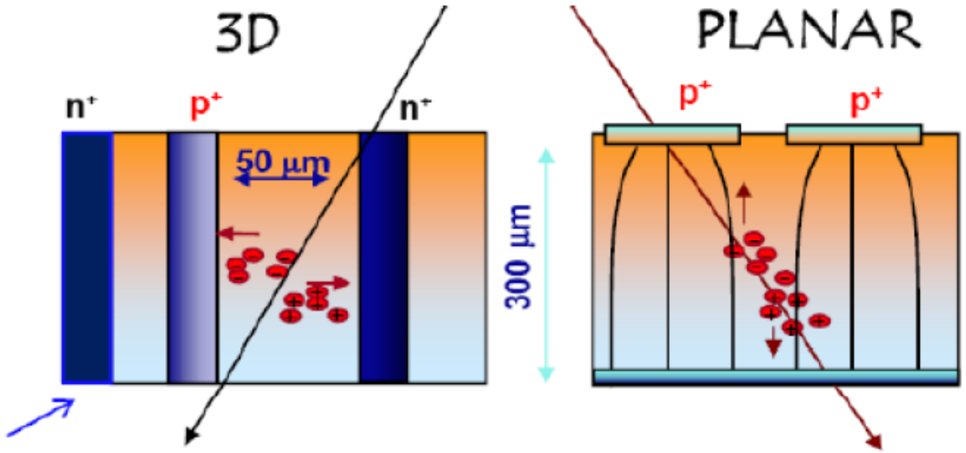
Sensor bulk material (p-type vs n-type)

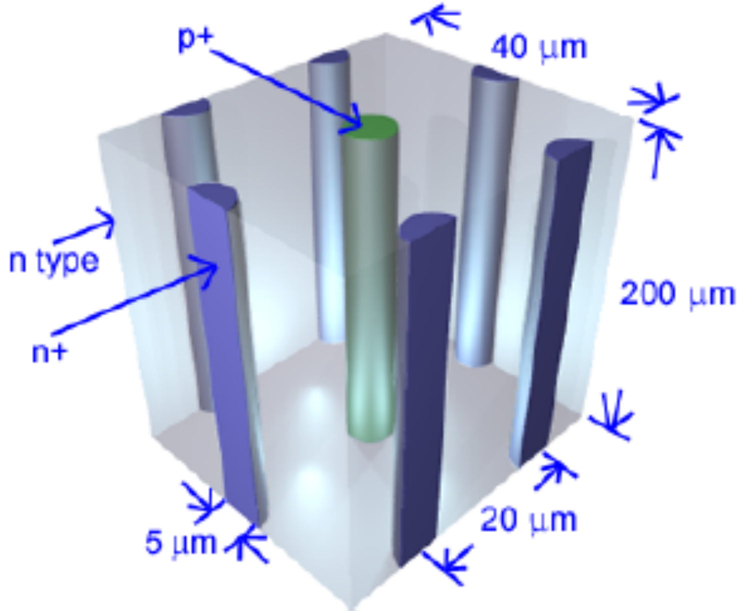


Sensor and FE chip thickness



Sensor technology: 3D Pixels

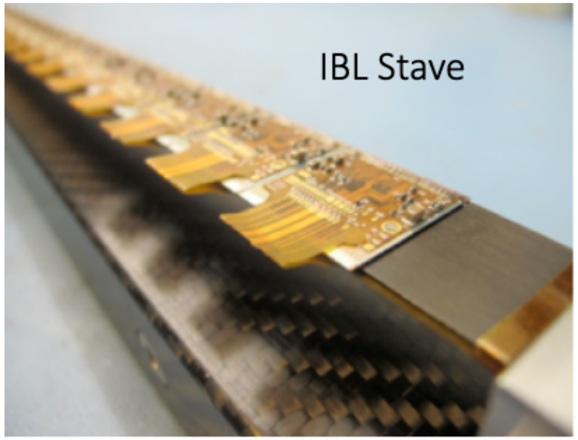




Here the electrodes are columns passing from one face to the other

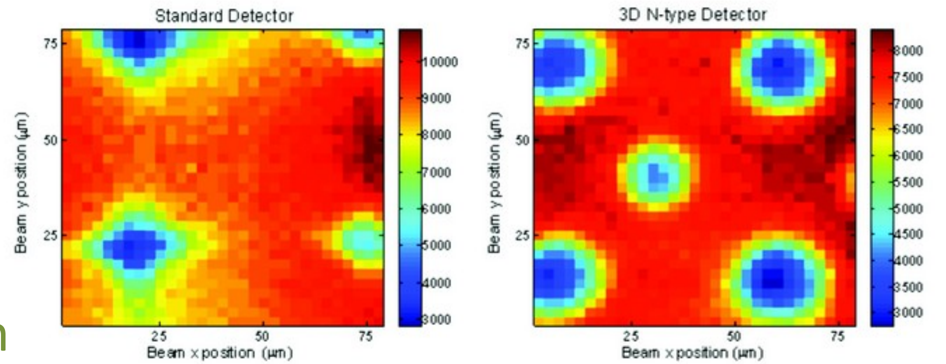
In this way the electric field is parallel to the face of the sensor and the charge drift evolves in a few tens of um

- They are intrinsically more rad-hard with respect to the planars and work at a lower bias voltage (less distance to cover)
- Charge travel distance decoupled from the length of the particle path inside the sensor !



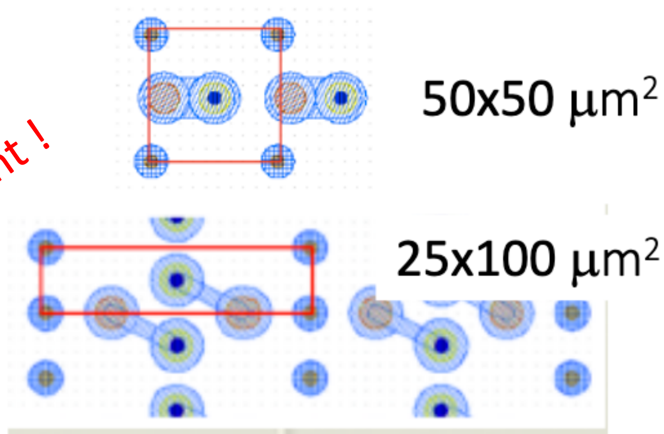
They are used for instance in the ATLAS IBL

- In the first productions, dead (or low-efficiency) regions in the columns and in specific positions! Often mitigated simply tilting the sensor
- In the first productions, limited yield and high prices.



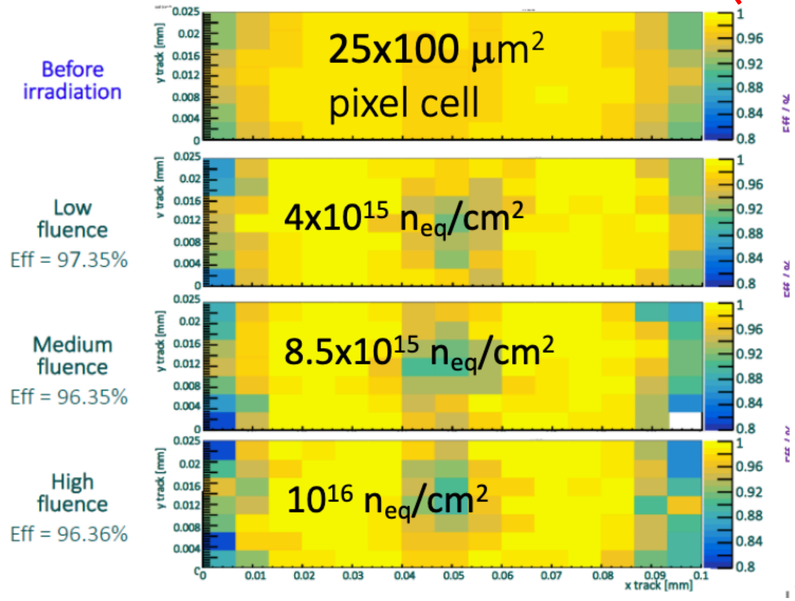
- Recent experience has allowed to reach a yield not too different from planar pixels, ATLAS produced @ O(80%)
- Improvements in the process control allow now to design thinner cells

Recent !



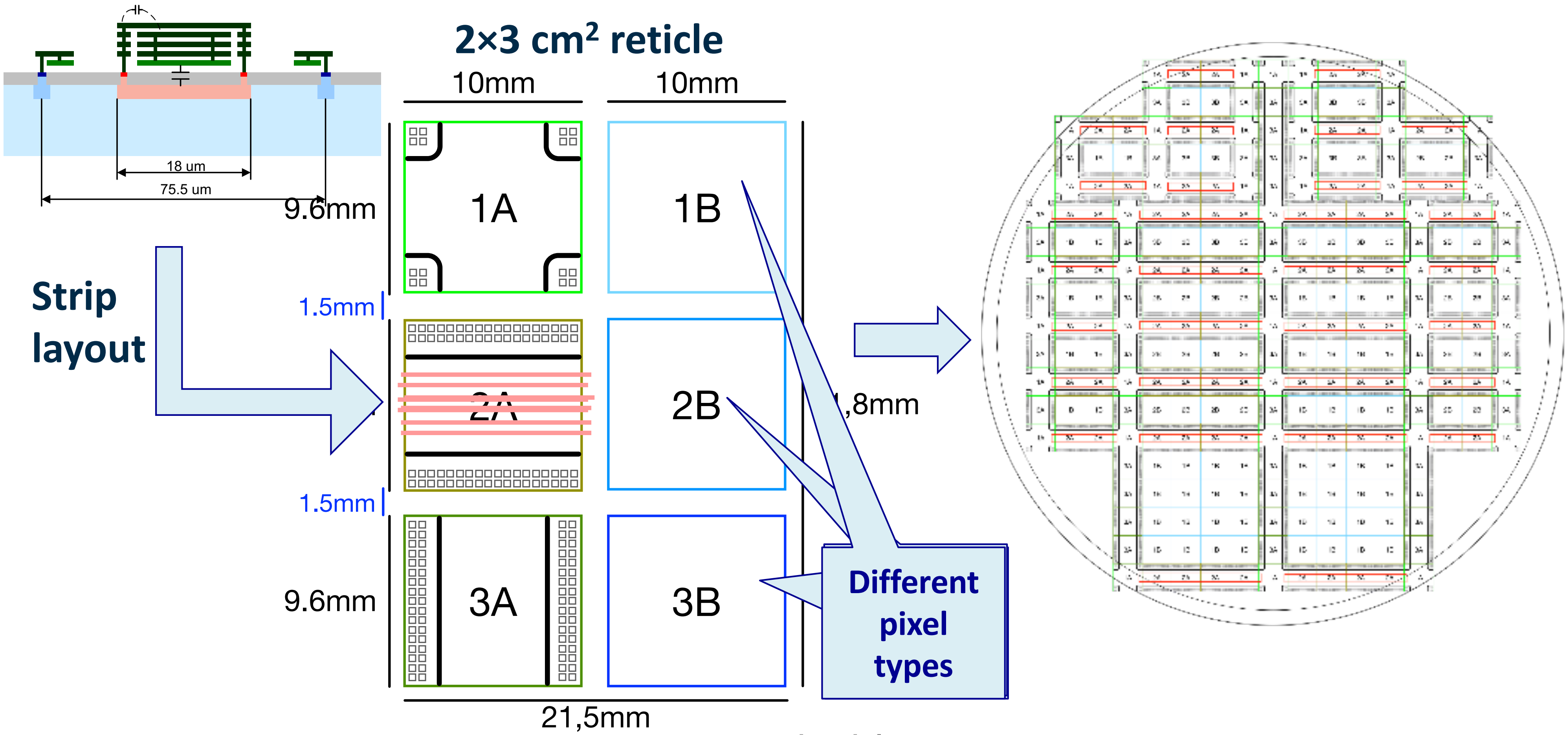
A. G. Alonso et al., IWORID 2019, Irradiated 3D RD53A modules

Recent !



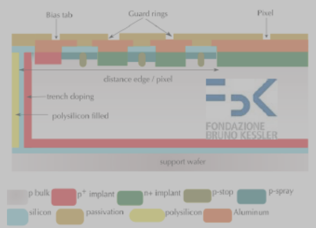
Sensor technology: passive CMOS

- Implement passive structures in standard CMOS processes on high resistivity substrate
  - Alternative fabrication process for standard strip and pixel sensors: **“fast and cheap”**
  - **Stitching** to build large area sensors: **example of submission: Lfoundry 150 nm (ATLAS)**



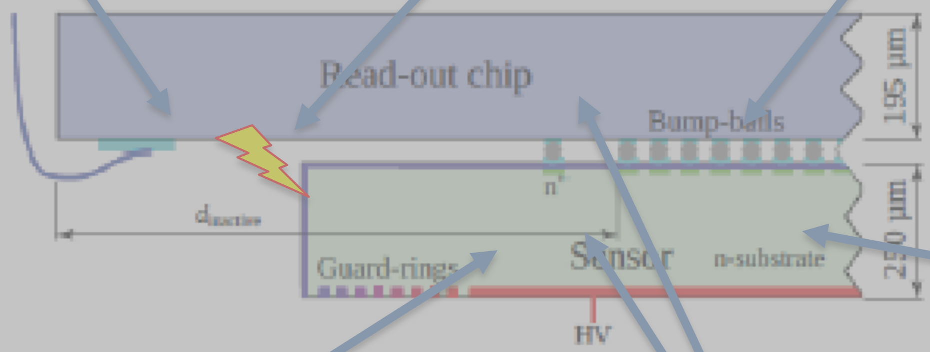
Hybrid detectors: recent highlights

Efforts to improve hit efficiency at the edge (slim-edge / active-edge)

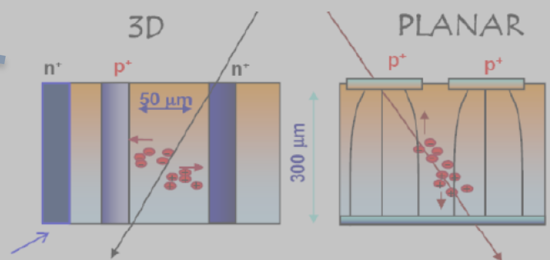


HV protection to avoid possible sparking at the edge

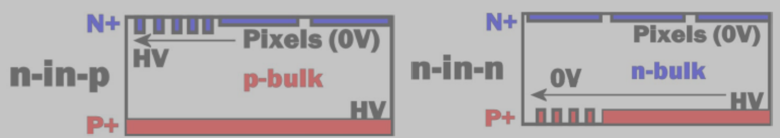
Pixel size/pitch and interconnection technologies



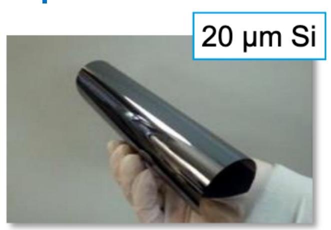
Adaptable sensor technology



Sensor bulk material (p-type vs n-type)



Sensor and FE chip thickness

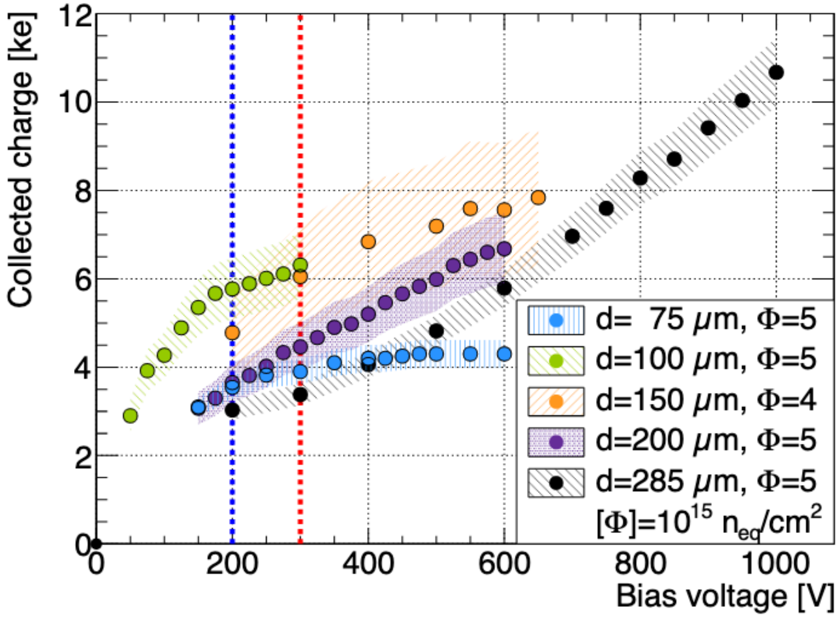


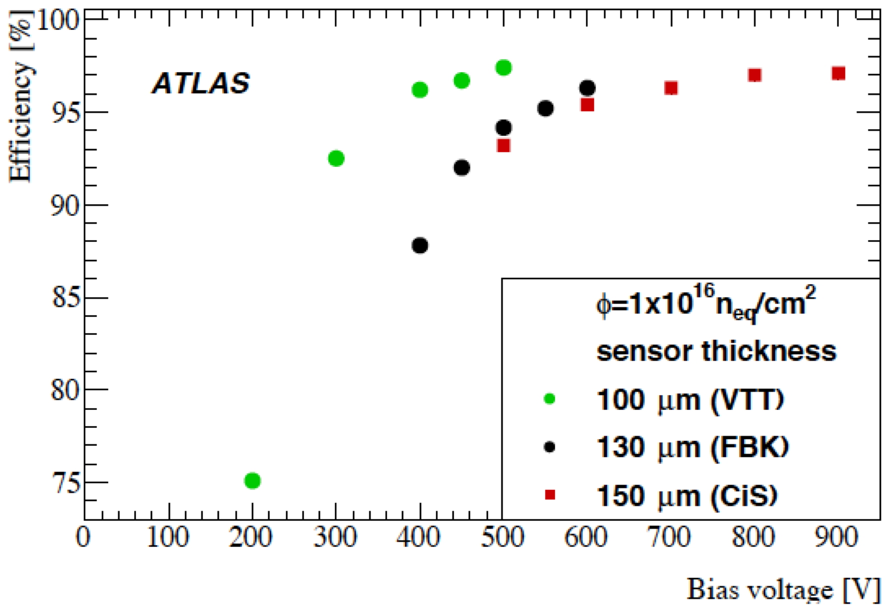
Thin sensors

After heavy irradiation the bulk cannot be fully depleted anymore. Interest to go thin!

- After irradiation, reduced collection distance, thin sensor can be optimal
- Stronger electric field, faster collection
- Lower power dissipation
- Lower occupancy at high eta
- Less material budget

arXiv:1612.01281

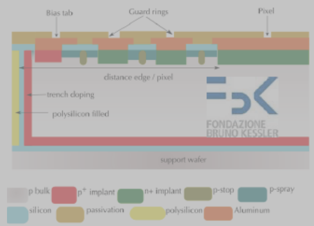




Even at very high fluence (for planar pixels), thin sensor can guarantee an excellent hit reconstruction efficiency

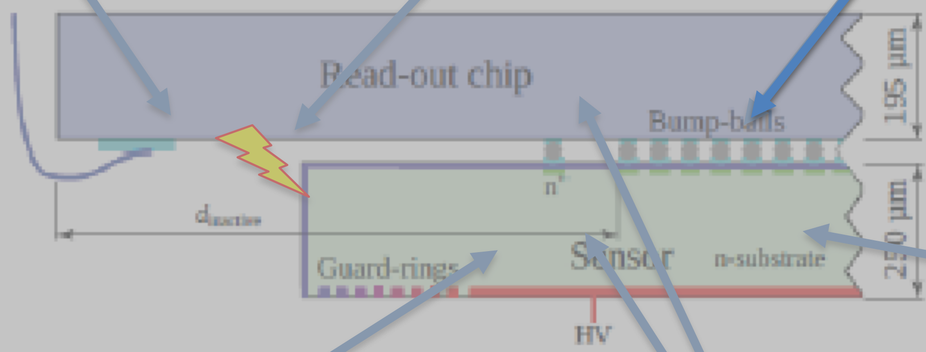
Hybrid detectors: recent highlights

Efforts to improve hit efficiency at the edge (slim-edge / active-edge)

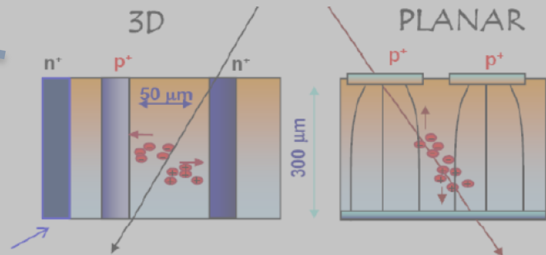


HV protection to avoid possible sparking at the edge

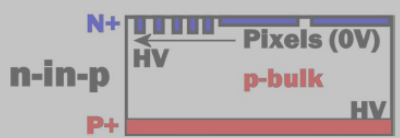
Pixel size/pitch and interconnection technologies

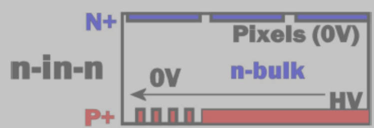


Adaptable sensor technology

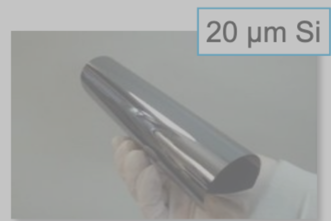


Sensor bulk material (p-type vs n-type)





Sensor and FE chip thickness



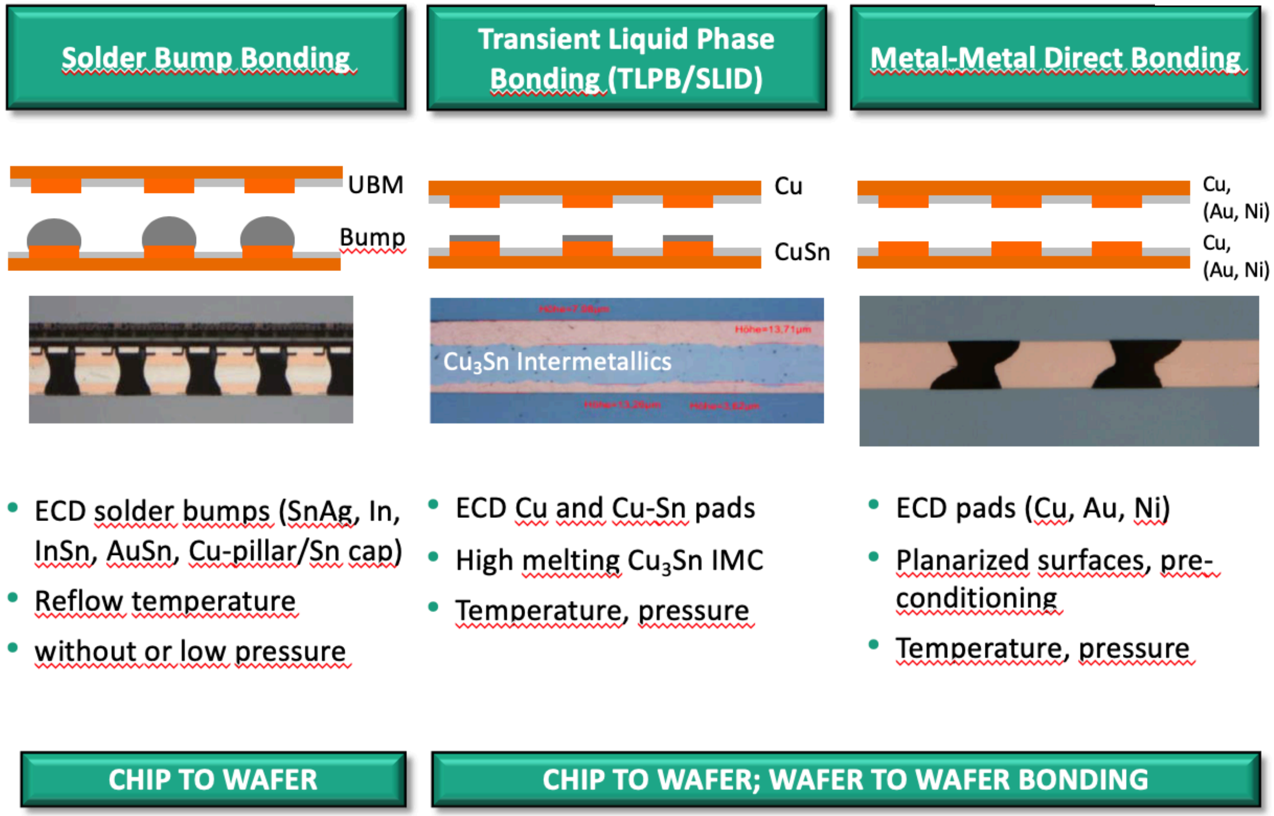
Small pitch

Small pitch could limited by interconnection techniques

Standard solder bump bonding, but also copper pillars, is in general limited to a pixel dimension of at least few tens of microns

Advanced techniques can be used to overtake this limit

Fraunhofer IZM



T. Fritzsch, AIDA-2020 workshop

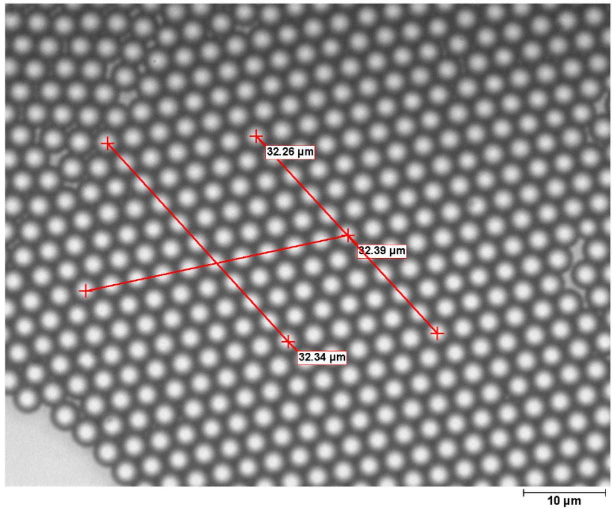
Anisotropic conductive films (ACF)

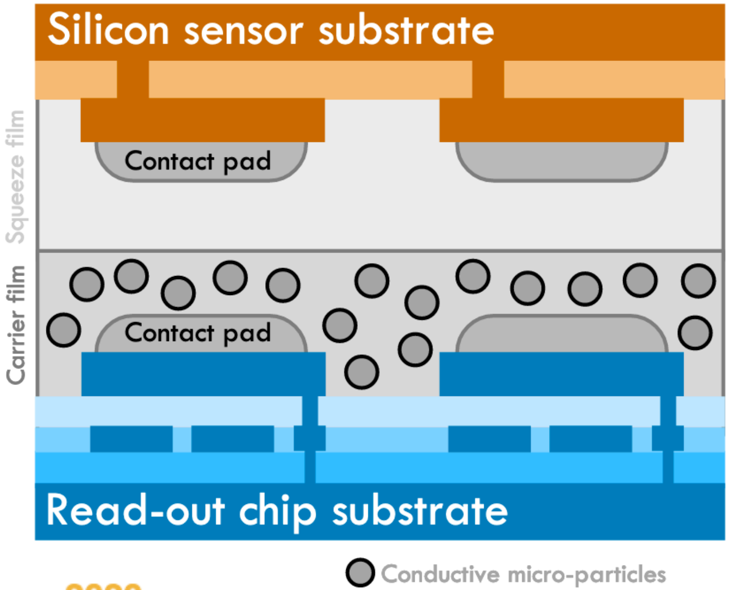
Anisotropic conductive films can also be used as interconnection technique

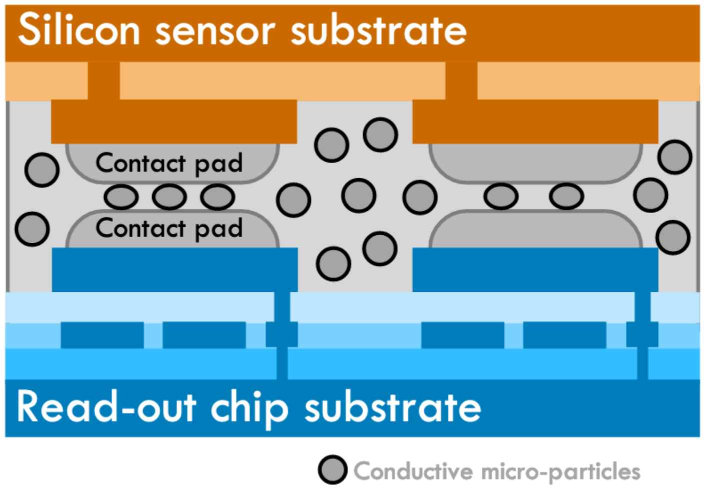
Application potentially important also from the cost point of view

Bump-bonding represent a significant fraction of the hybridization cost of pixel modules

Development is also part of AIDA++ proposal in the hybrid detectors Working Package





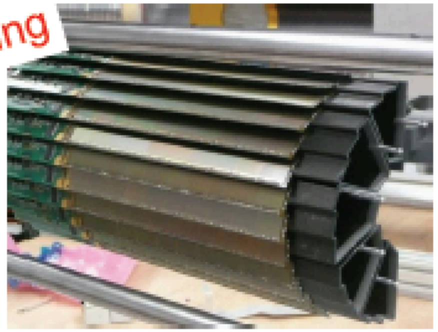


M. Vicente, D. Dannheim et al.

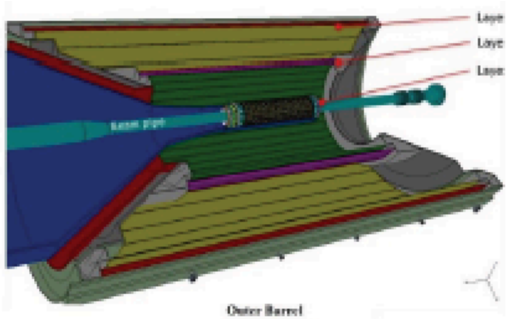
The Second Family: Monolithic

Monolithic detectors: recent highlights

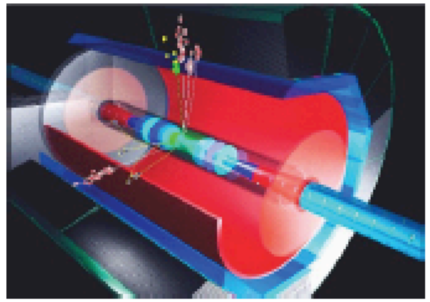
running



STAR HFT



ALICE ITS upgrade

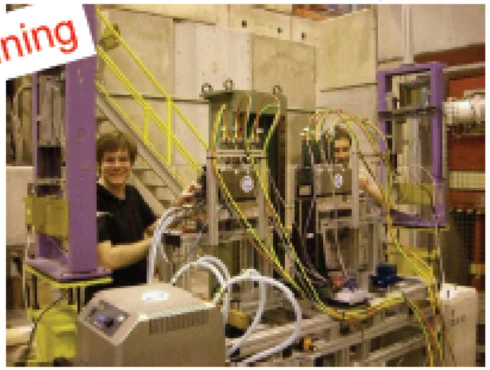


ILC

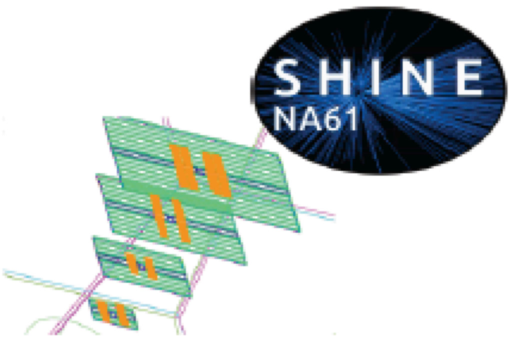
IPHC
Institut Pluridisciplinaire Hubert CURIEN STRASBOURG

2008 2014 2016 2018 2021

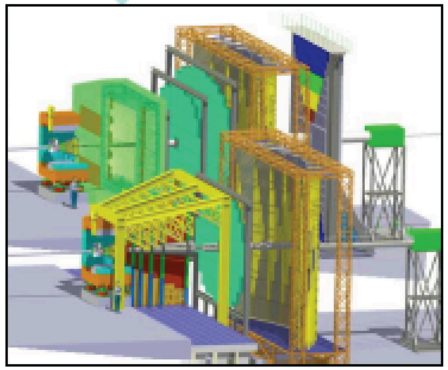
running



EUDet Telescope



NA61 SAVD

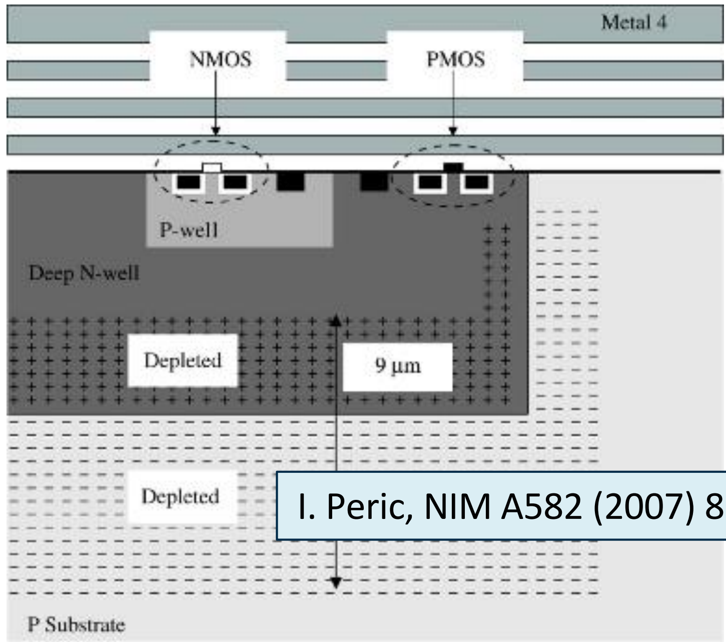


CBM - MVD

Depleted CMOS monolithic detectors

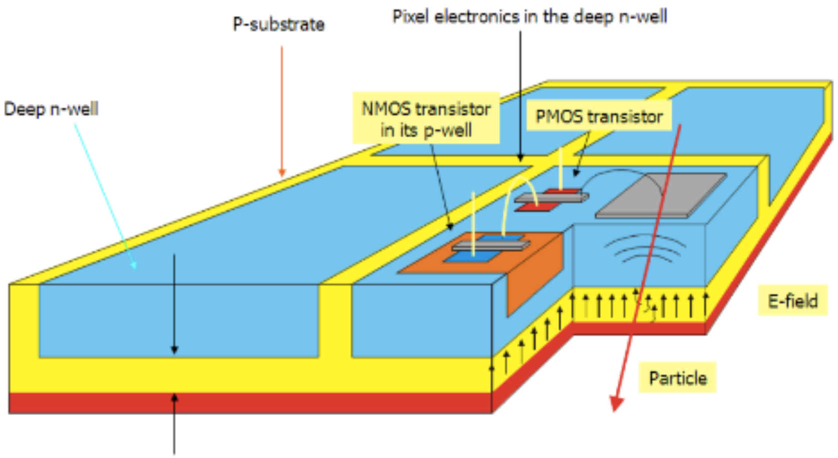
- **"Natural" choice for pixel layers:**
  - Monolithic architecture minimizes detector thickness
  - *e* produced in the depleted layer are collected quickly by drift providing adequate time resolution

$$d = \sqrt{\varepsilon_{\mathrm{Si}}\varepsilon_0\mu_{\mathrm{carrier}}\rho\left(V + V_{\mathrm{BI}}\right)}$$



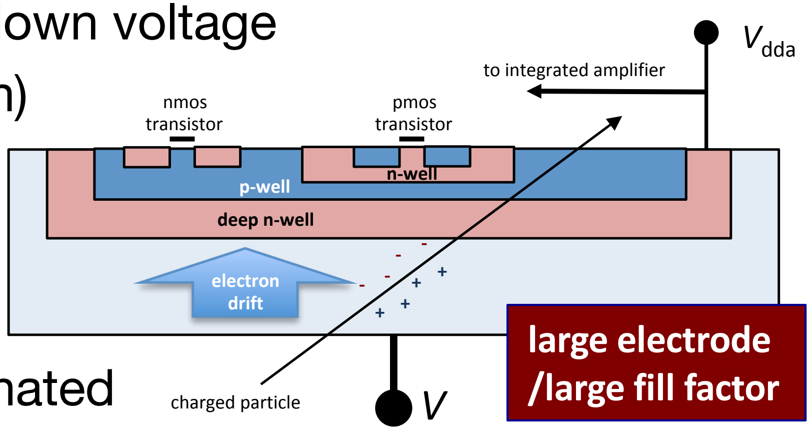
I. Peric, NIM A582 (2007) 876

- Enabling technologies:
  - **High Voltage** processes
    - Availability of processes with high voltage capability, driven by automotive and power management applications
  - **High Resistivity** substrates
    - Foundries accepting or qualifying wafers or epitaxial substrates with mid/high resistivity
  - **130-180 µm feature size**
    - deep submicron technologies needed for the design of radiation hard electronics
    - multiple well process to decouple front-end electronics from the sensitive region

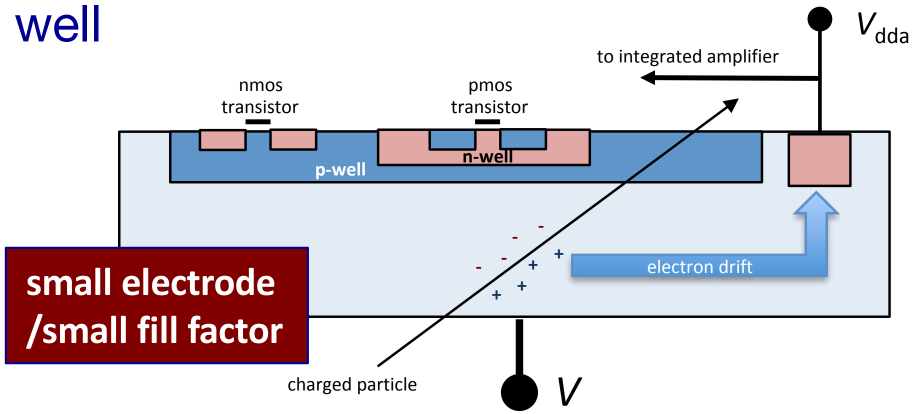


Depleted CMOS monolithic detectors

- Depletion zone built either in a 10-30 µm mid-resistivity p-type epitaxial layer or high resistivity substrate
- Collection electrode is a deep n-well or a buried n-layer, implanted onto a p-type substrate
  - Size of depleted region limited by the breakdown voltage
  - Signal up to 10-20 ke (varying with irradiation)
- Front-end electronics **inside** the collecting well
  - **uniform charge collection**
  - **short drift path → less trapping**
  - **large electrode capacitance** ~100 fF, dominated by parasitic capacitance between the deep wells

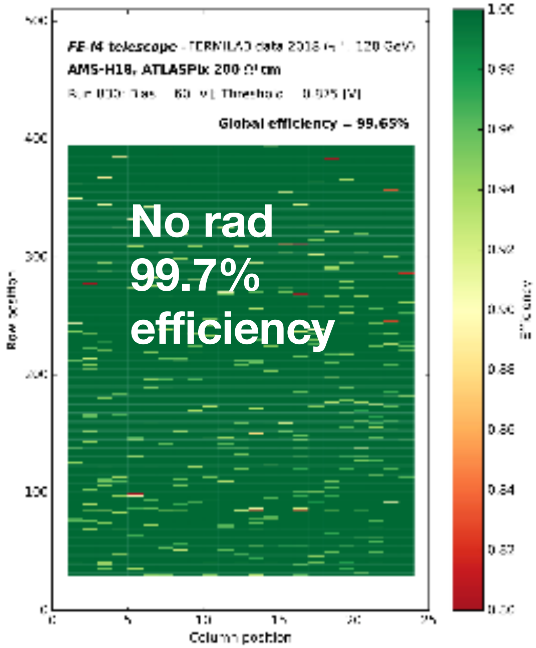


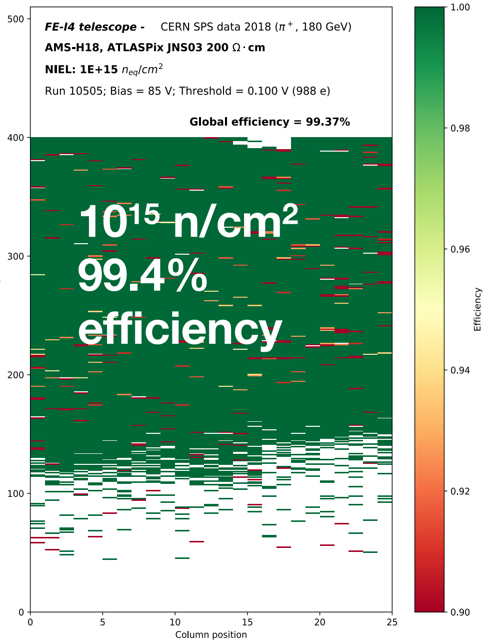
- Front-end electronics **outside** the collecting well
  - **non uniform drift field**
  - **long drift path → more sensitive to trapping**
  - **small electrode capacitance** <10 fF



ATLASPIX3

- **AMS 180 nm HV** technology **now moved to TSI** (USA) compatible process
- Sensor radiation hardness verified on several prototypes till 2×10^{15} n/cm^2





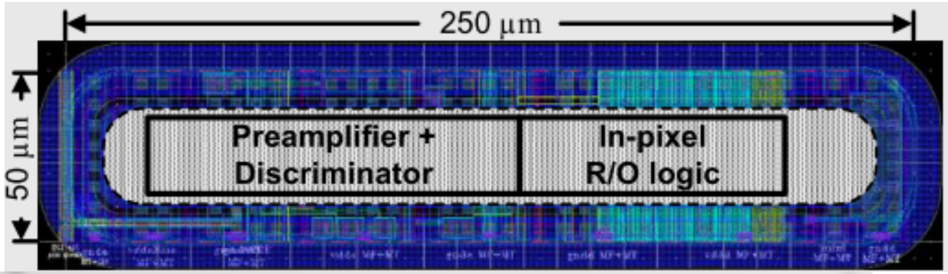
- Full size matrix: 20.2mm x 21mm
- Compatible with most ATLAS requirements:
  - 50×150 µm^2 pixel size, **large fill factor**
  - Column drain readout (FE-I3 like)
  - Compatible with RD53A serial powering schema and readout protocols
- **Submitted to TSI in April**

LFoundry MONOPIX

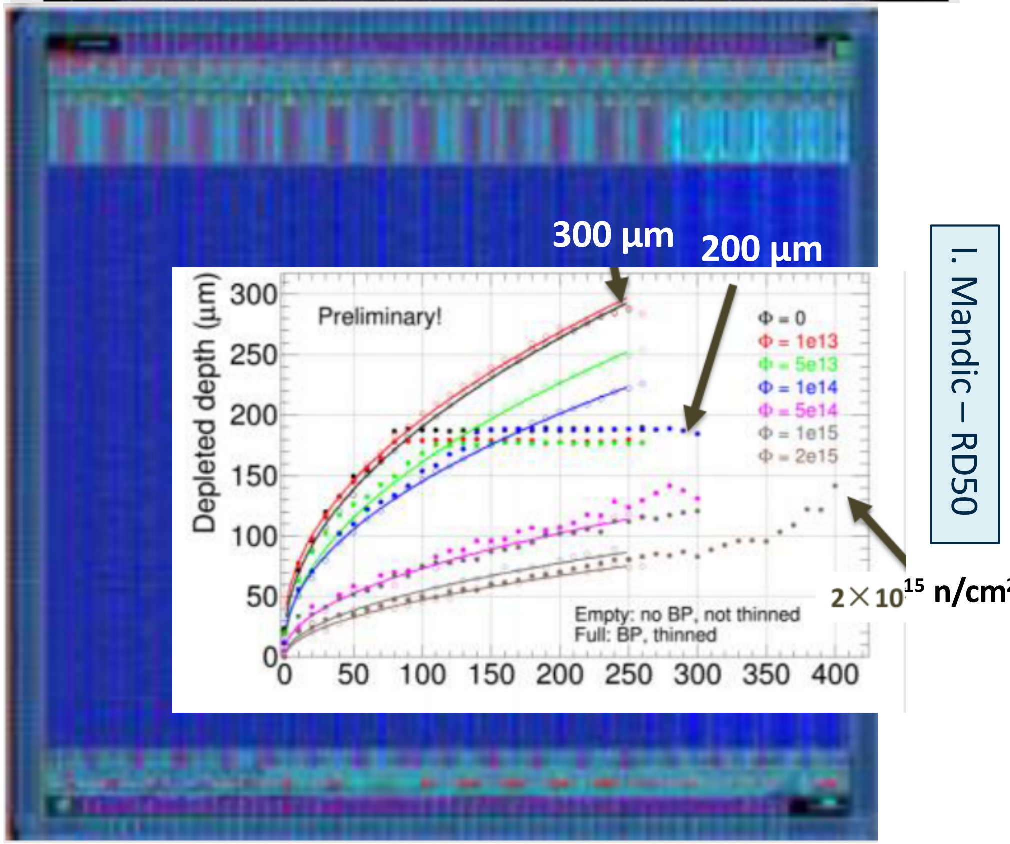
Material from T. Hemperek
Future Tracker Workshop - Oxford 2019

- **L-Foundry 150 nm** process (deep N-well/P-well)
  - Up to 7 metal layers
  - Resistivity of wafer: >2 kΩ·cm
  - Small implant customization
  - Backside processing

CPPM · Irfu - CEA Saclay, Institut de recherche sur les lois fondamentales de l'Univers · UNIVERSITÄT BONN



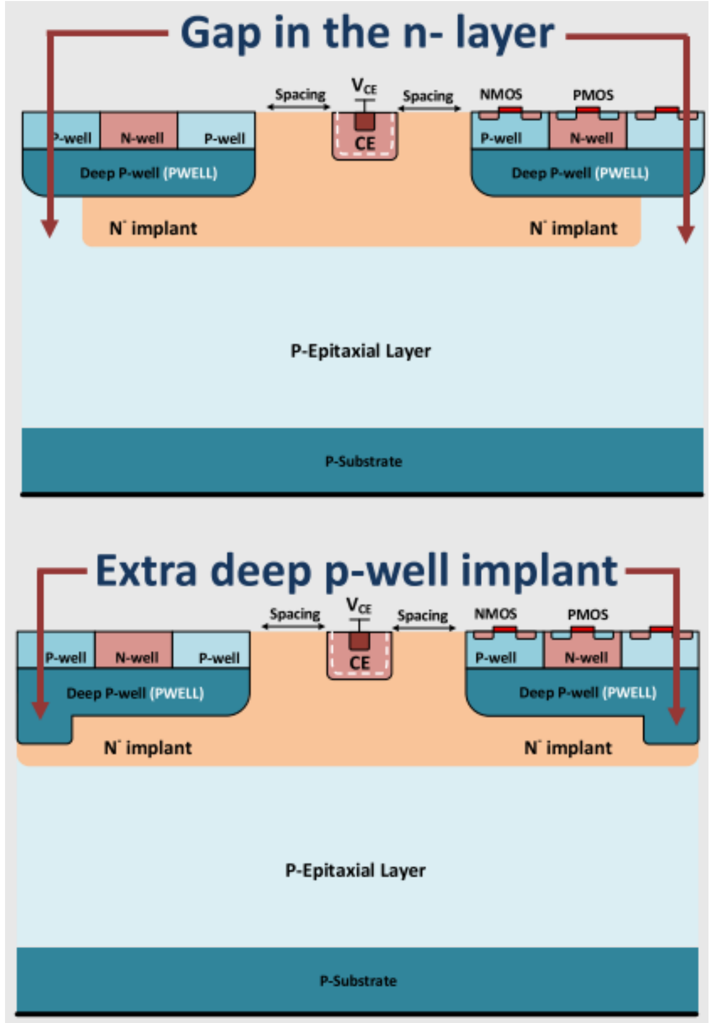
- **LF-Monopix**
  - Pixel size: 50 μm x 250 μm
  - Chip size: 10 mm x 10 mm
  - Column drain readout
  - 200 μm and 100 μm version thickness
  - Measured good >99% MIP detection after high neutron radiation
  - Breakdown >280 V
- **LF-Monopix2** in preparation
  - Pixel size: **50 μm x 150 μm**



I. Mandic – RD50

TowerJazz: MALTA-MONOPIX

- **TowerJazz 180 nm** CMOS CIS
  - Deep Pwell allows full CMOS in pixel
  - Derived from ALICE development (CERN)
  - Epitaxial-layer thickness: 18 – 40 μm
  - High resistivity: 1 – 8 kΩ·cm
  - Modified process to improve lateral depletion
- **MALTA** (asynchronous) and **TJ-Monopix** (column drain) implementing **small fill factor** designs
  - 36×40 μm^2 pixel size
  - Very low noise (10-15 e^-) and threshold dispersion (30-40 e^-)
  - Pixel design submitted in 2017 had charge losses due to low field region at pixel corners
- New cell design submitted in 2018, being tested now on small size prototype
- **Large scale arrays probably submitted end of 2019**

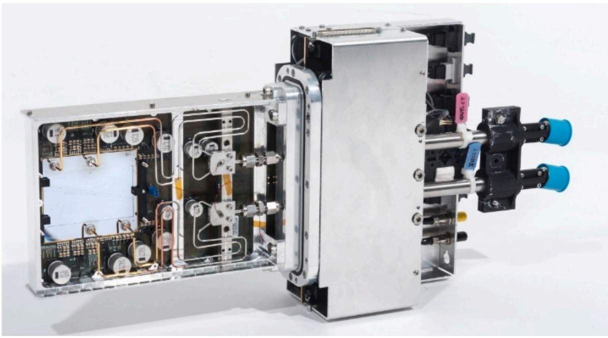


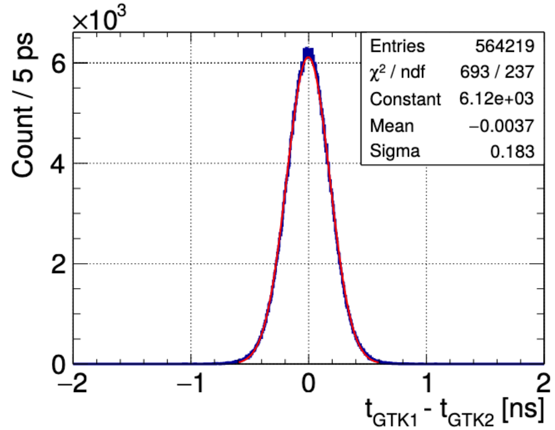
Importance of 4th coordinate: Timing

Fourth dimension is the next step of the new generations of trackers

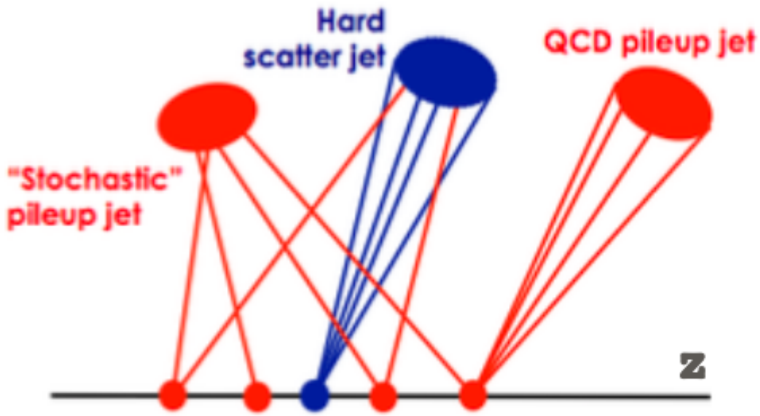
Will be able to solve ambiguities due to fast bunch crossing or pileup

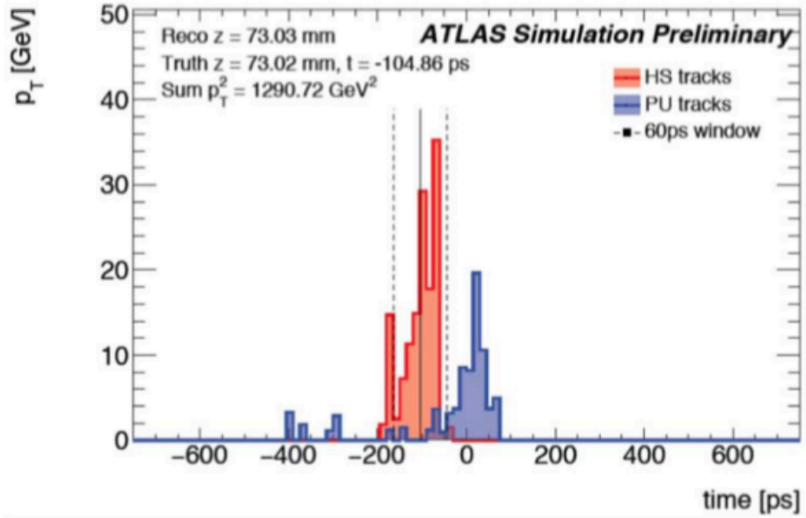
NA62 Collaboration led the path, with a resolution per station of the order of 180 ps





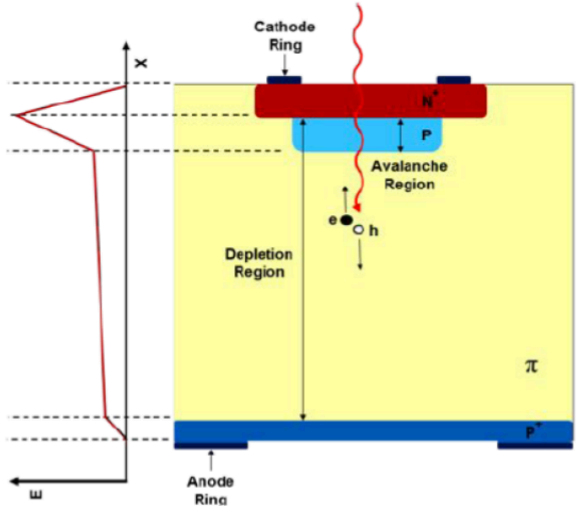
ATLAS/CMS developing timing layers





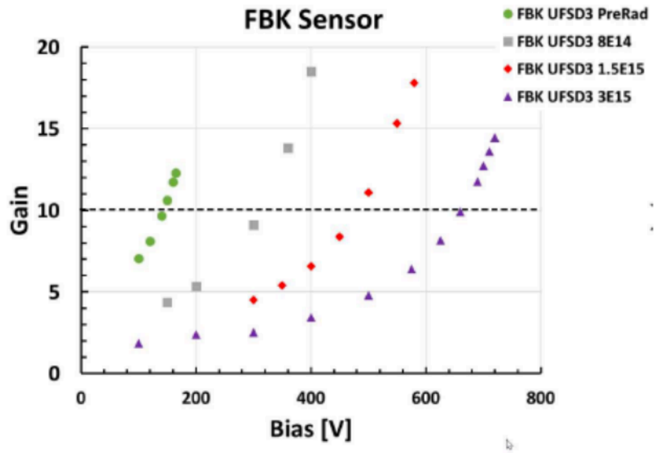
LGAD – Low Gain Avalanche Diode

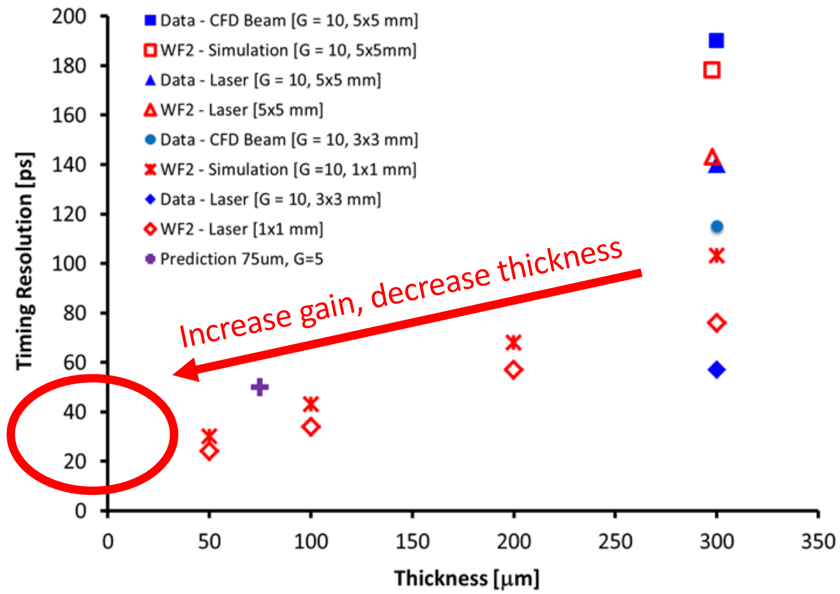
- Highly doped p+ region below the n+ implant
- This generates a multiplication layer
- Internal gain factor from 10x to 30x (before irradiation)
- Low thickness to maximize slew rate: dV/dt



$$\sigma_t \sim \frac{t_{rise}}{S/N}$$

- Gain decreases after radiation (de-activation of the gain layers)

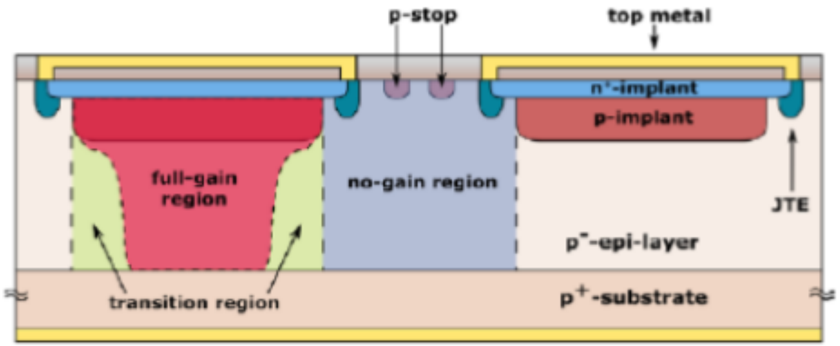




- Options under study: Gallium or Carbon co-implantation

Inverted LGAD - (I-LGAD)

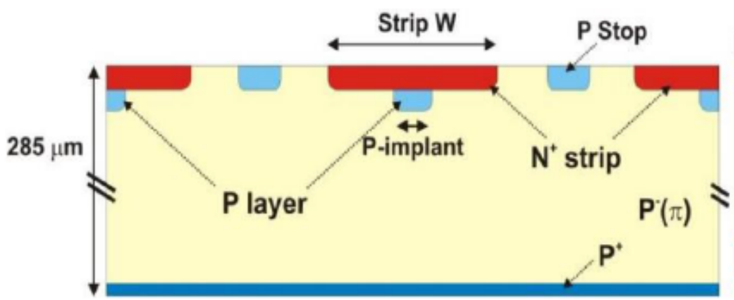
In standard LGADs, the presence of a multiplication layer prevents the use of small pixel implants due to the width of the no-gain region

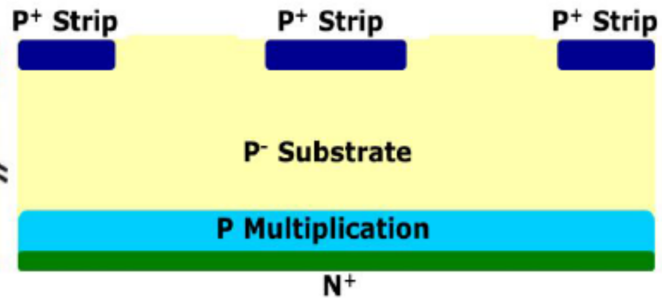


A few techniques are available to avoid this limitation: one is the use of Inverted-LGADS (I-LGADs) where the multiplication layer is on the opposite face

Multiplication layer divided into strip
Collects negative carriers (e)
Simple single side process

Multiplication layer extended over the electrode
Collects positive carriers (h)
Complex double side process





Recent !

LGAD N on P microStrip

P on P microStrip **iLGAD**

https://indico.cern.ch/event/666427/contributions/2881813/attachments/1603622/2544525/20180219_iLGAD_IvanVila.pdf

Conclusions

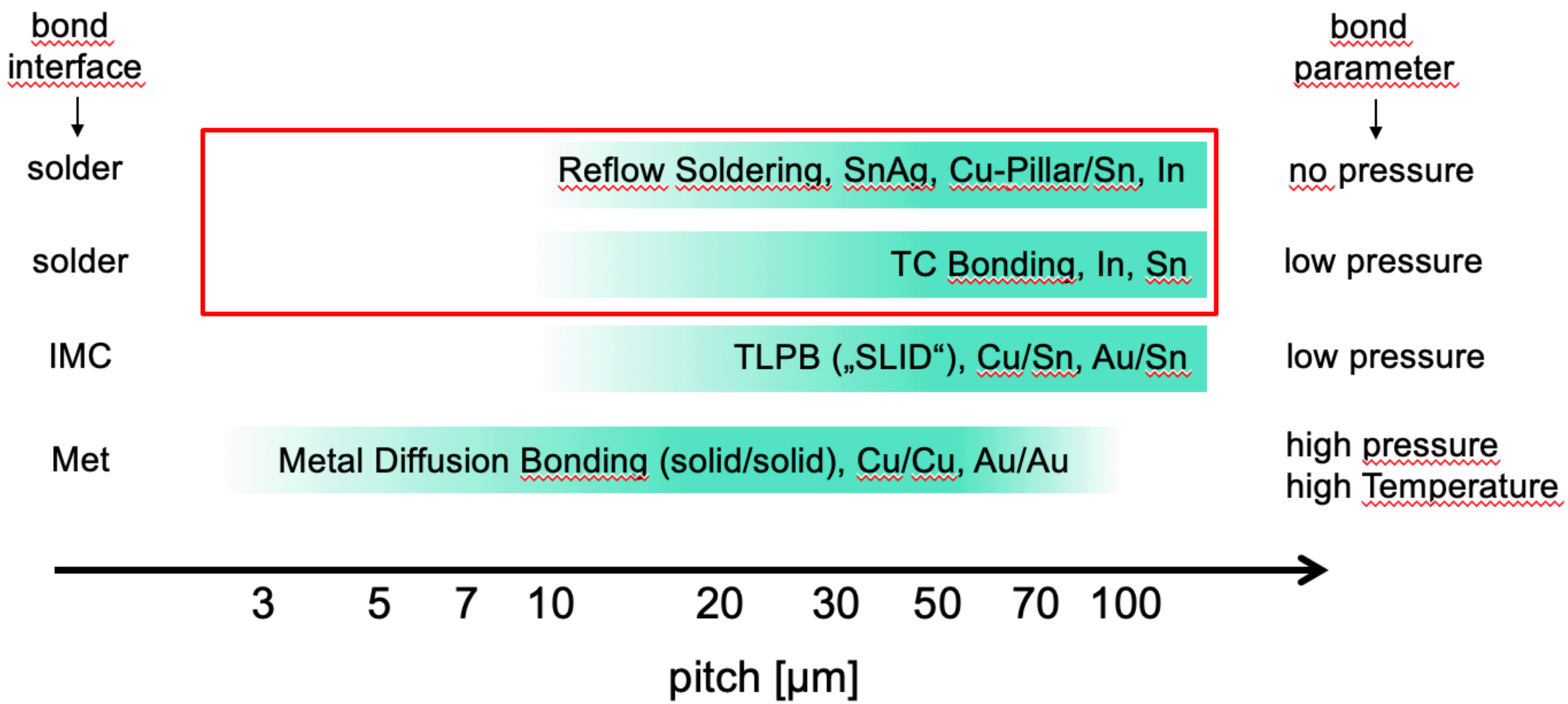
The data-taking conditions at colliders have evolved towards challenging tracking environments over the last 30 years

In parallel, a lot of technological progress has been made in detectors and in silicon trackers in particular, to cope with these new conditions

Different families of devices have been developed to match specific contexts and they have been differentiating more and more

I tried to give snapshots of some areas in which there were significant recent improvements, but there are many more!

For each future machine there is already a tracker solution which is developing, but technology will evolve even more in the meantime


bond interface
solder
solder
IMC
Met
Reflow Soldering, SnAg, Cu-Pillar/Sn, In
TC Bonding, In, Sn
TLPB („SLID“), Cu/Sn, Au/Sn
Metal Diffusion Bonding (solid/solid), Cu/Cu, Au/Au
bond parameter
no pressure
low pressure
low pressure
high pressure
high Temperature
3 5 7 10 20 30 50 70 100
pitch [µm]