Prague Integration Workshop 2019

Extraits choisis

Milestones

Pixel integration sequence in time in SR1

Main Milestones

SR1 ready for integration of Itk Pixel (from Common and Pixel)	16/09/2022	
Outer Barrel ready for Outer System integration	23/05/2025	*
Outer EndCap C delivered at CERN	31/01/2025	
Outer EndCap A delivered at CERN	31/01/2025	**
Outer System Ready for insertion into ITK	27/08/2025	***
Inner Replaceable Layers halves at CERN	05/04/2024	****
Inner System Assembled at CERN ready for Insertion in ITK	25/06/2025	
Outer System completed and inserted into ITK	10/11/2025	
Inner System completed and inserted into ITK	29/01/2026	
Pixel detector completed and inserted into ITK	29/01/2026	
Pixel detector completed, inserted and tested into ITK	26/02/2026	

****Milestones IS

Assembly line set up at CERN	07/03/2023
First Inner quadrants arriving, last ones	15/05/2023 05/04/2024
Inner System integrated	26/07/2024
Inner System Cold Tested	06/06/2025
Inner System ready for dressing in ITk	27/11/2025

** Milestones EC

Endcaps in SR1	31/01/2025
Endcaps on OS integration tool (Integration of Endcaps on Outer System tool)	C: 18/04/2025, A: 16/05/2025

*Milestones OB

Arrival of first parts	27/10/2022
Start of half-layer integration	12/01/2023
OB half 1 ready	19/09/2024
OB half 2 ready	23/05/2025

*** Outer system integration (OB and ECs) and test

- Continuously system test in DAQ/DCS development bench in operation

30.09.2019 SR1 Schedule Pixels - Susanne Kuehn 2

Risques

Schedule risks for Pixels with external dependencies

1. **Lack of integration space in SR1:** More in detailed slides on Tuesday in Pixel session
2. **Delay due to overlap of required cooling with ITk Strips:** Input was collected by Martin Doubek to be followed-up. More in cooling session on Tuesday? (spare slides)
3. **Insertion platform not fully functional for pixels:** Are specifications of this tooling available?
4. **BCM' late in installation**: many details missing, general problem for ITk Pixel not only for integration. Integration of BCM' to happen at SLAC
5. **QC equipment not available in large enough quantity for parallel integration sites:** part of equipment for SR1 purchased via common. Within pixel components to be selected and ordered, payment by Common. Correct?
6. **FELIX readout systems incl. FW/SW/DCS not available for QC in production:** later slide
7. **Late installation of test equipment for Pixel inner system and Pixel Outer Endcaps in SR1**: Technical support for installation of cables, PP2, LV, HV etc in SR1 not only needed before 09/2022 but also in 04/2024 and 01/2025. More on next page
8. **Phase-II FELIX readout systems not available for sub-system QC in production:** Mitigiated with more Phase-I FELIX systems
9. **Space for System Test, DAQ&DCS development bench**: see later slide
10. Damage in transport or lowering due to load of type-1 data services → move to Common/TC?

Felix / DCS

FELIX readout systems incl. FW/SW/DCS not available for QC in production

Component readiness for Pixel integration

Phase 1 FELIX and PC's first batch available	0 days	Tue 31/12/19
Phase 1 FELIX and PC's second batch available	0 days	Tue 29/12/20
Phase 2 FELIX and PC's available	0 days	Tue 22/08/23
Phase 2 FELIX and PC's available	0 days	Tue 22/08/23
ITK Interlock Pre-Production complete	0 days	Fri 31/12/21
ITK Interlock Pre-Production complete	0 days	Fri 31/12/21

Availability of DAQ/DCS for various integration setups
In total 14 sites which need support

Close work of teams performing QC during pixel integration with ITk software and ITk readout team and TDAQ needed

DAQ/DCS to be ready for integration from 06/2022

In SR1 about 54 FELIX boards foreseen to be run in parallel from 01/2025 (25 boards from 05/2023)

Integration sites / QC

https://indico.cern.ch/event/829117/contributions/3580349/attachments/1917521/3171238/SurfaceTesting-Pixel-Prague-v1.pdf

Different electrical test classes

- **Full electrical test/performance test**: Scans like noise, threshold, ToT, disconnected bumps to compare results to earlier results in production chain
  - Deploying standard ITk Software scans.
  - Are scans like minimum threshold tuning, double trigger implemented
- **Electrical connectivity test**
  - SP-chain powering and configuration of FEs,
  - Check all up-links and down-links
  - Check mapping
- **Electrical functionality test**
  - SP-chain powering and configuration of FEs,
  - Check all up-links and down-links
- **Continuity test**:
  - Resistance for LV and HV. LV with very low current, no low power mode needed, depends on PSU and FE I-V curves.
  - No check of data lines. No cooling.
  - Check of DCS, Tilock lines

→ **Tests in detail to be defined**
→ **All except continuity need cooling with CO_2**
→ **Use DAQ/DCS bench (system test setup) in SR1 for preparation and verfication of tests**

01.10.2019 Pixel surface commissioning and slice test 3

Low Power Mode / QC

https://indico.cern.ch/event/829117/contributions/3580349/attachments/1917521/3171238/SurfaceTesting-Pixel-Prague-v1.pdf

Testing in low power mode

- Special mode of operation foreseen in front-end of pixels
- Under implementation for ITkPixV1 FE which is foreseen to be submitted end Nov 2019
- Allows basic readout checks by powering only pixel chip periphery
- Power consumption to be seen, estimated to have a 1.3 W/cm^2 (40 % of nominal) in the periphery and about 0.025 W/cm^2 (~7 % of nominal) in the pixel matrix. Corresponding e.g. 86 W for L3 longeron compared to 450 W in nominal operation.
- Implementation in FEA to check thermal behaviour not available yet. Will mostlikely not requiring CO_2 cooling but to be seen if convective cooling needed.

- Requires 10 kHz (2 V) external signal which is routed up to PP1

- Still to be discussed further within Pixels
  - How much testing time would be saved?
  - Would signal to PP2 be useful?
  - Is LP mode operation without convective cooling possible? (Inhomogenous heaters in preparation to measure)

https://indico.cern.ch/event/829117/contributions/3587045/attachments/1918785/3173975/SummaryQuestionsReadThese_V1.pdf

Questions and conclusions Prague workshop (system)

- It must be investigated what hardware can be installed prior to LS3
  - If the loop from primary on surface to manifold in ATLAS is present we can do a full commissioning of that particular plant. (Primary slice + 2PACL plant + Surface storage + accumulator + transfer line + manifold)
  - We should investigate how we can have at least one of this full loop in place to start early commissioning
  - If we wait for the installation after the C3F8 decommissioning and CV room refurbishment we will not have sufficient commissioning time.
    - This will result in a not well debugged system with possibly many future operational errors.
  - For plant testing with swap scenario a minimum of the spare plant + 2 other plants are needed
    - Can this space be freed prior to LS3 by removing C3F8 compressors? Ideally 3 out of 8 compressors need to be removed in an EYETS period.
    - This need to be discussed soon with TC and ID to see the possibilities.
- Plant commissioning is a time consuming process but can be done with the detector attached in a later stage, need to agree on sharing time
- There is confusion about the coldest temperature and the qualification temperature
  - The system is designed for -40°C at PP1 at full load. With the current design a plant cooling temperature of -45°C is needed.
  - If the load has disappeared the pressure drop lowers (less vapor!) so the detector temperature drops. The cooling cannot be adjusted quick enough to avoid this (in 10 minutes time scale it could)
  - Qualification of staves need therefore be done at -45°C at least = SR1 cold cooling temperature