

Summary of the test beam at DESY 2019 for SiW-ECAL

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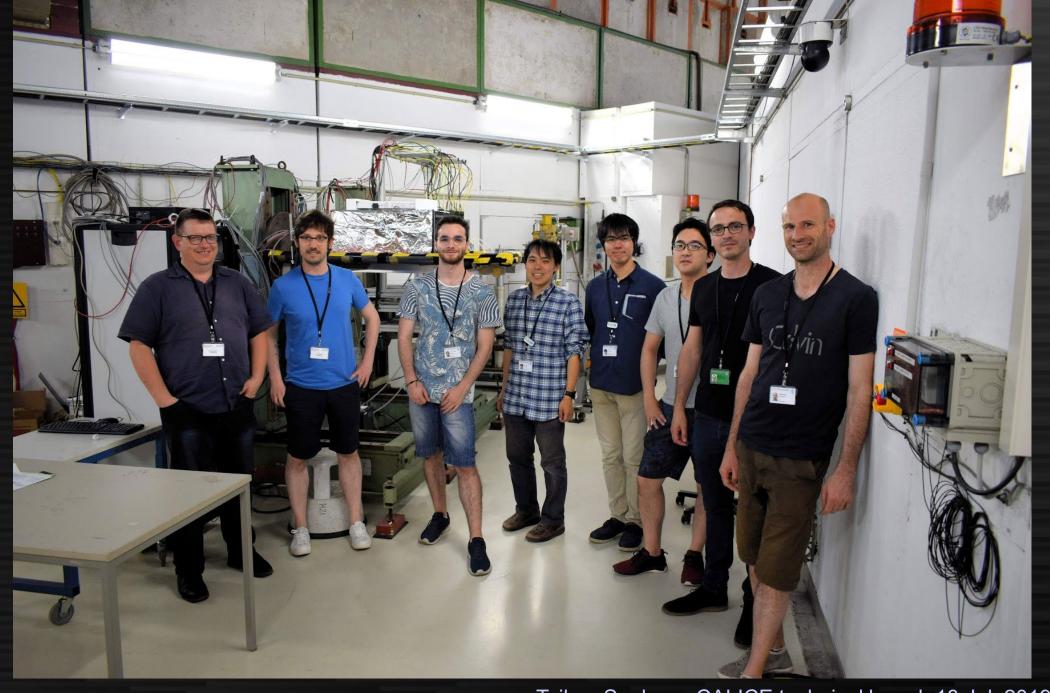






Test beam: overview

- 24 June 6 July, TB24 at DESY
- 9 layers
 - 5 x FEV13 from Kyushu, 2 x FEV12BGA + 2 x COB from LAL
 - This talk only covers FEV13 part
- 3 GeV for MIP, 1-5 GeV for shower
- 3 from Japan (Y. Kato (Tokyo), K. Goto (Kyushu) and TS)



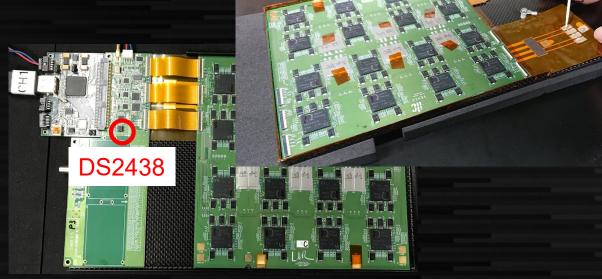
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FEV13 layers

- Modification/improvement from previous TB @ CERN
 - Replace the backing plate / cover
 - Newly made carbon sheets
 - No problem on HV connection any more (except for the fragile MMCX connector)
 - Temperature monitoring on SMB
 - Implemented last year but not used
 - Separate script to acquire the temperature every 1 min
 - 5 MHz clock (with new firmware)
 - Power-pulsing delay tuned (not done in the previous TB)

Old (reused from FEV8)

new



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Assembly to the LAL box



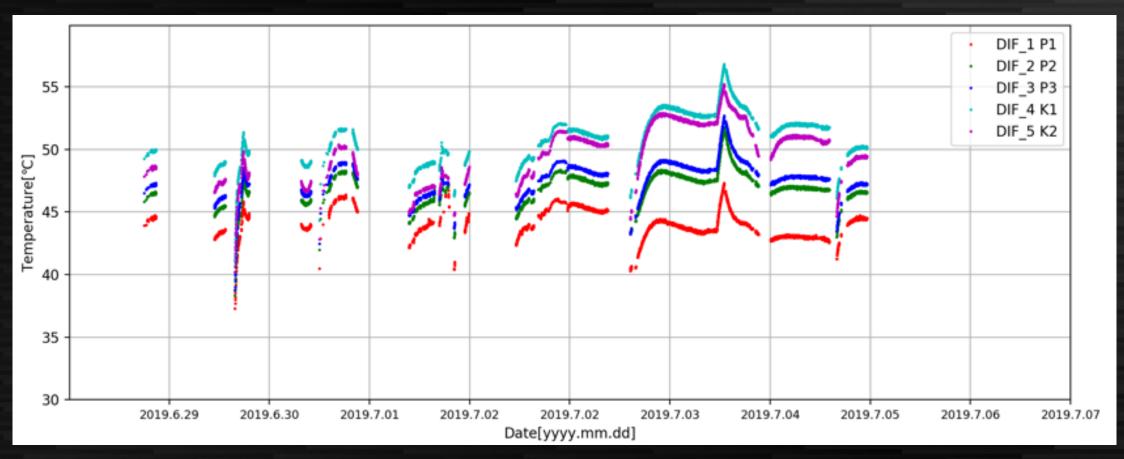


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Technical issues

- HDMI connection
 - Data loss or corruption sometimes occurs
 - Once: replace DIF to a spare (thanks to a stock from LAL)
 - Need to support the heavy cables (partially done with cable ties)
- HV connector (MMCX) easily broken at SMB
 - Needed to re-solder several times
 - Should be replaced in the next design
- Imperfect insulation of new carbon frame (HV: 180/150 V)
- Cable connection complicated
 - 1 HV + 1 SMB + 1 DIF (loose) + HDMI / layer

Temperature



Quite high at center of the box – no air flow (fan is placed outside) Kyushu layers are power-pulsed: LAL layers are not Leakage current increase also seen (but not 100% correlated)

Leakage current



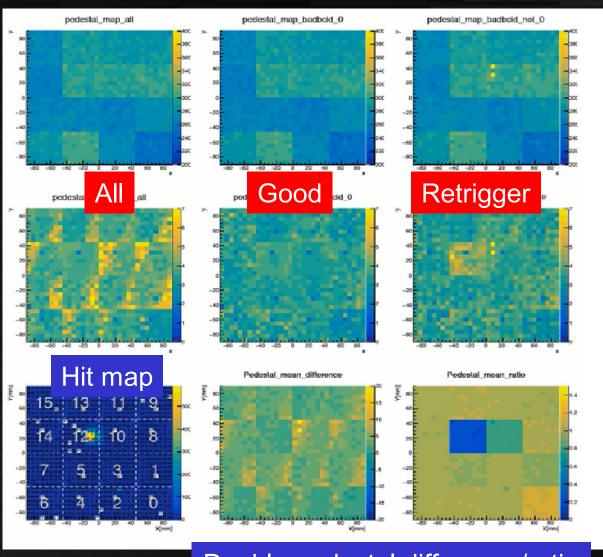
Program

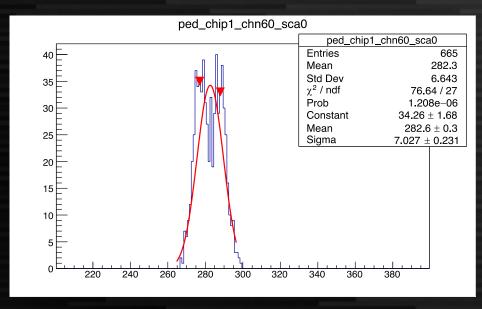
- MIP programs
 - Position scan
 - S-curve
 - Angle beam (to calculate active thickness)
 - TDC
 - Retriggering / double pedestal
- Shower program
 - TDC / autogain
 - Retriggering
 - Edge effect

Quick view: pedestal

Pedestal mean

Pedestal width

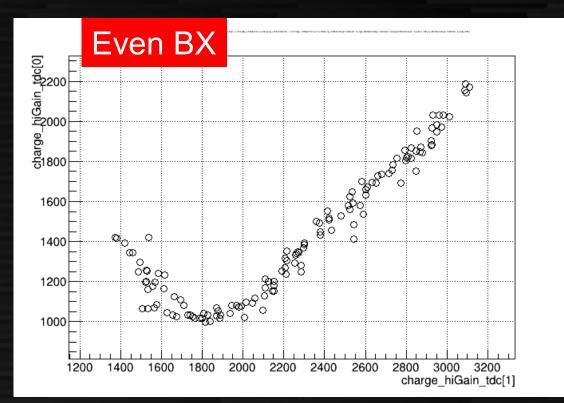


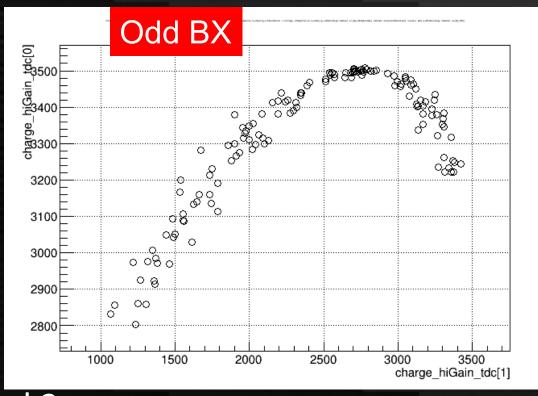


Double pedestal

Double pedestal difference/ratio

Quick view: TDC with MIP





- Correlation of TDC between slab 1 and 2
- Select 1 ch (at the center of the beam), 450 < ADC < 500 (to avoid timewalk)
- ~10 / 1 ns at the normal slope: timing resolution ~ a few ns?

To do for analysis

- Target: analysis will be completed by end of this year
 - Common event display for Kyushu+LAL layers
 - MIP analysis
 - Tracking: efficiency
 - Effect of threshold and retriggering
 - Gain variation
 - TDC: timing resolution and calibration
 - Effective thickness
 - Shower analysis
 - TDC: timing resolution vs signal height and sensor thickness
 - Energy resolution with comparison to simulation
 - Edge effect

- Summarize chip/PCB issues for the next production
- Shower analysis for paper

To do for hardware

- Optimize HV connection (and consider slab-slab HV connection)
- Optimize power-pulsing structure
 - Minimum delay time (and minimum power-on for A/D/DAC/ADC)
- 8-inch wafers (2020)
 - Including some modification on PCB design
- Connection to SL-board (after linux-based DAQ prepared)
 - Temperature measurement?
 - Connection needs to be modified
- Power-pulsing capacitor (current one already discontinued)