Development and characterization of novel electronics for the search of dark matter for DAMIC-M

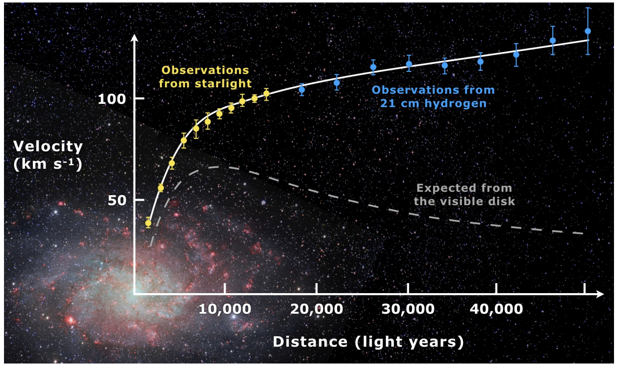
Giorgos PAPADOPOULOS
DAMIC-M
LPNHE, Sorbonne University, Paris

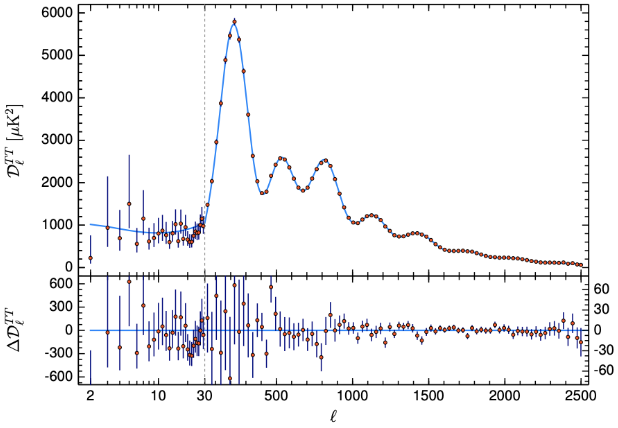
JRJC 2019

Dark Matter (DM) motivation

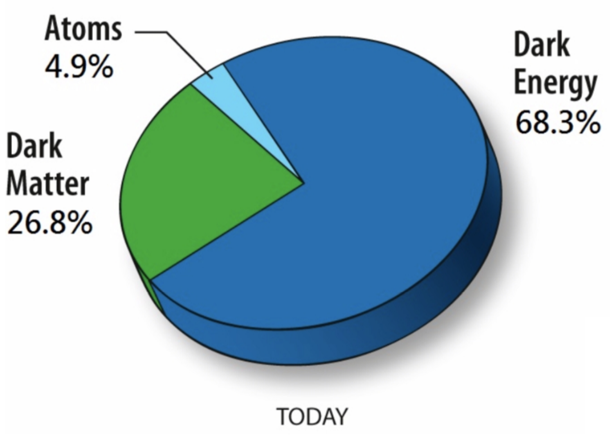
Evidence:

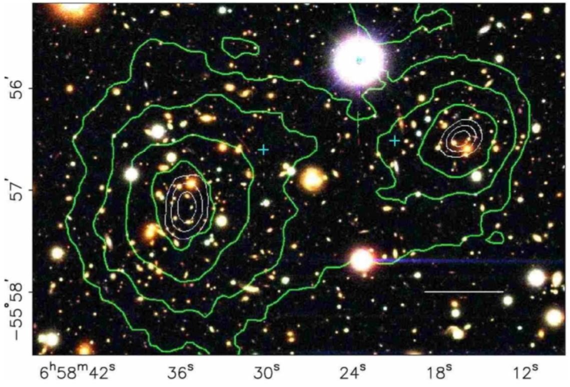
- Galaxy rotation curve
- Weak field lensing of colliding galaxy clusters
- CMB power spectrum
- Mass to luminosity ratio

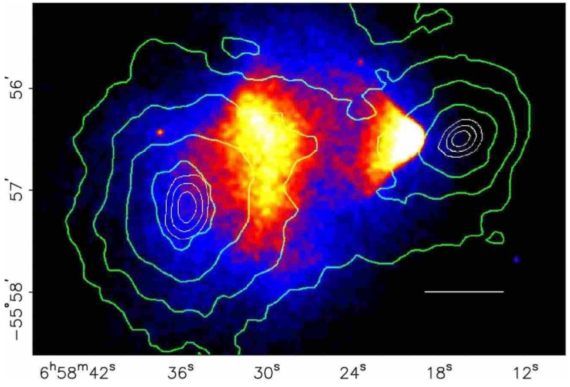




Up to date "beliefs":



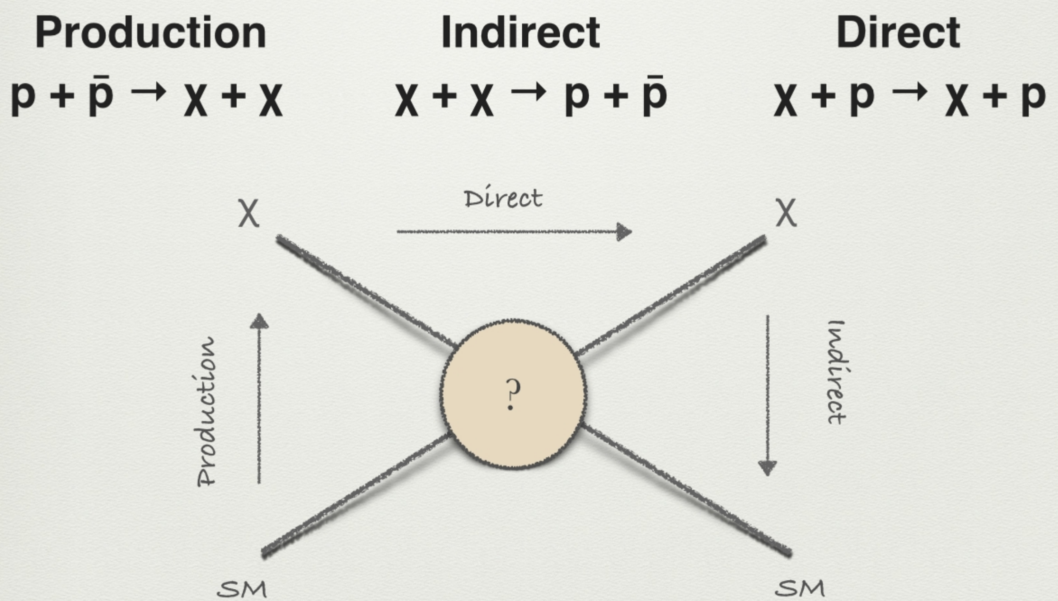




DM detection method motivation

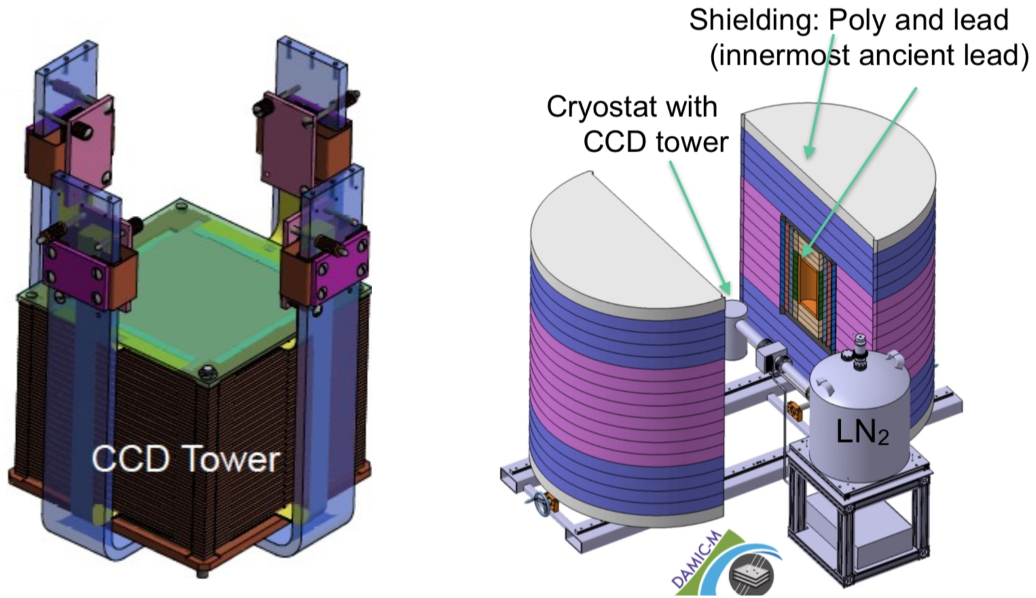
Indirect methods only enhance the DM existence (AMS-02)

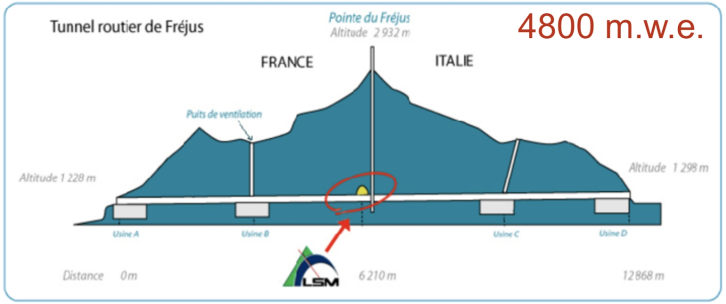
Production has been unsuccessful to reveal the nature of DM in the GeV-TeV mass range (LHC, CERN)



Multiple experiments give an effort in the detections of DM. Current results can only exclude regions for the mass or cross-section of possible DM particles.
→ Light wimps

DAMIC-M Overview





DArk Matter In CCD at Modane (DAMIC-M):

- 50 scientific Charge Coupled Devices (CCDs) made of ultra-pure Si with Skipper readout
- 36Mpix large and ~20g each, a total kg-size target mass
- Sub-electron resolution
- 0.1 dru background

- R&D of the electronics to control the CCD
- Simulations of the detector design and shielding
- Underground Laboratory in Modane (LSM). ~2km of rock to stop cosmic background.
- Low Background Chamber (2020) test detector to evaluate new CCDs and measure background
- Final experiment data taking will start in 2022.
- DAMIC-M will pioneer in the low mass WIMPs and hidden-sector DM research.
- ERC grant

CCD Operation

Exposure
charge generation
and collection

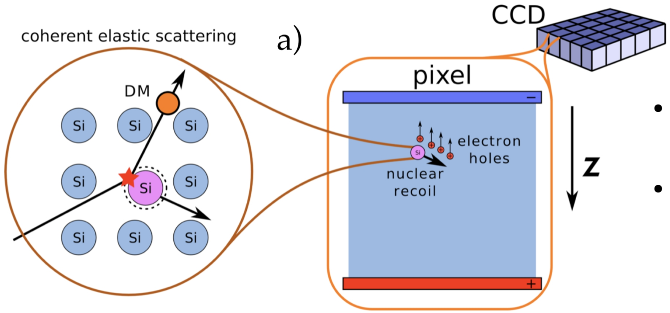
* Static condition of the detector

→

Readout
charge transfer
and recording

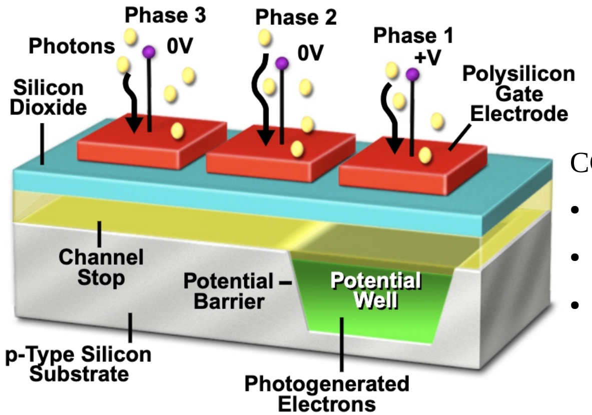
Charge Coupled Device (CCD)

1. Charge generation - Exposure



- CCD made of silicon and separated in pixels.
- Incident particles deposit energy in the bulk

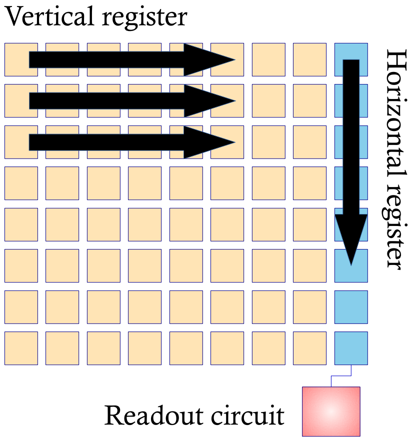
2. Charge collection - Exposure

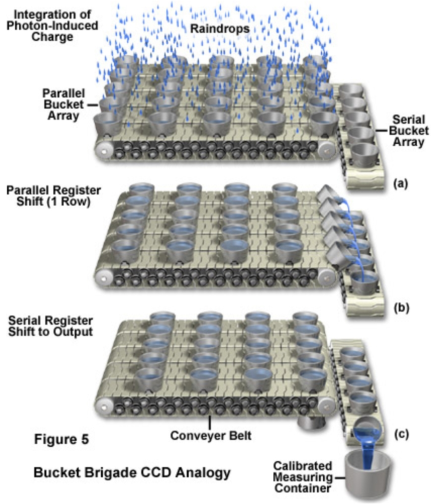


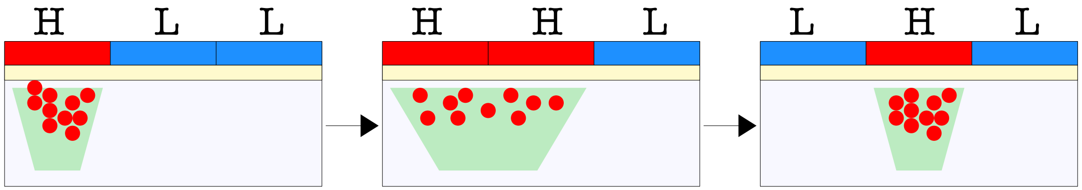
CCD single pixel.

- 15μm x 15μm
- 3 electrodes: 1 "active"
- Charge collection under the active electrode

3. Charge transfer - Readout



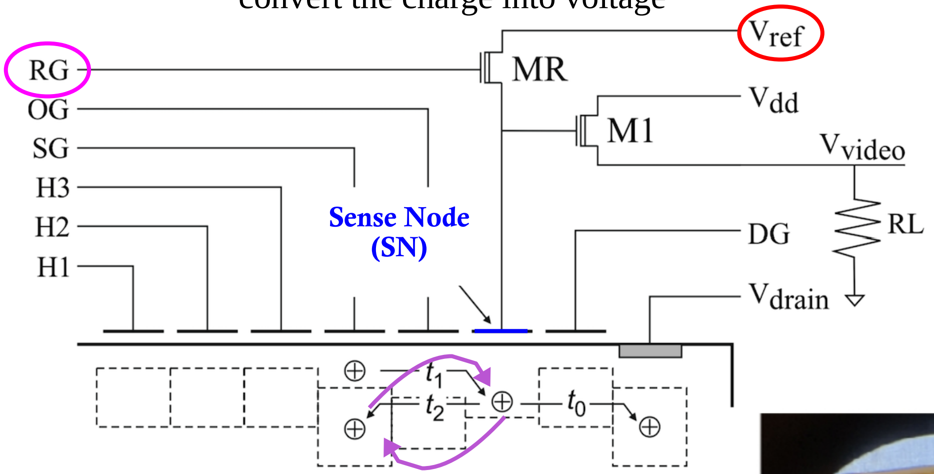


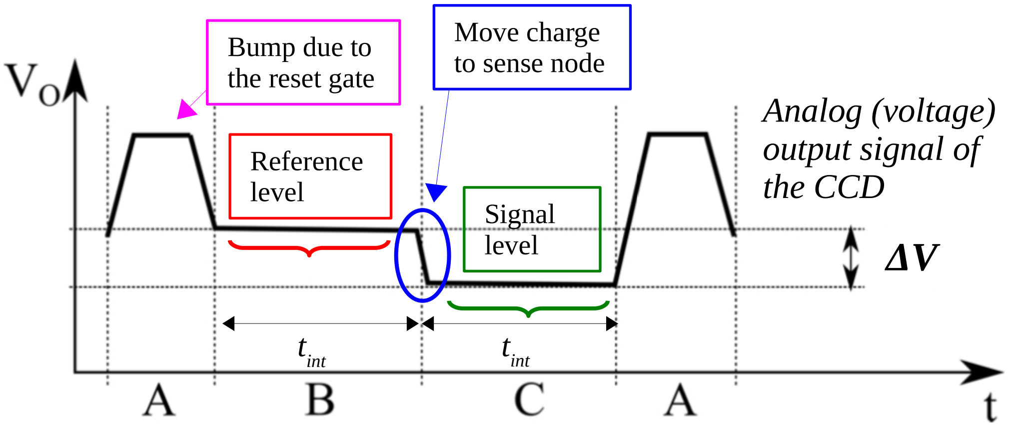


- Move the charge by alternating the voltage of the electrodes
- An analogy of this operation is the bucket brigade

CCD Readout (Skipper)

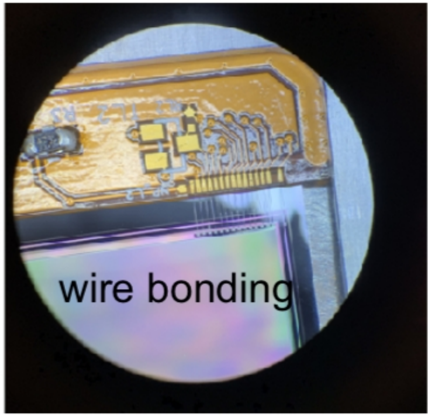
Reaching the end of the CCD, there is a circuit that will convert the charge into voltage





Analog (voltage) output signal of the CCD

Skipper technique allows for a Non-Destructive Multiple pixel charge measurement (NDCM) which results the electronic noise to follow the 1/√NDCM (→A. Matalon talk)



- Before moving the charge under the sense node (SN), the Reset Gate puts the sense node to a Reference voltage.
- A bump will occur in the output signal of the CCD
- Then, the charge is moved to the SN.
- ΔV is the voltage change due to the charge following

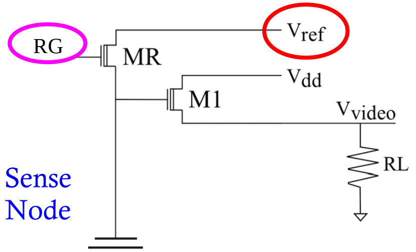
$$\Delta V = \frac{Q}{C_{SN}}$$

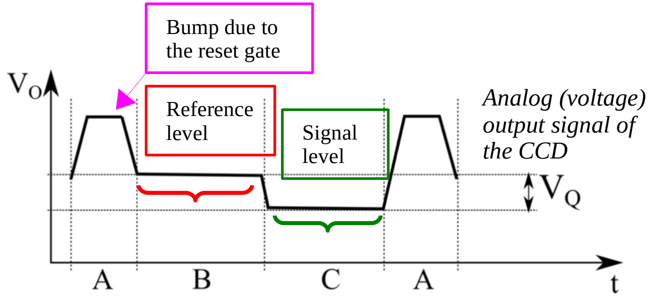
where C_{SN} is the capacity of the sense node

Noise sources

Reset noise (or “kTC” or “kT/C” noise)

- The reference level is not always the same after every reset due to thermal noise generated by the resistance of the reset FET
  - *Correlated Double Sampling* (CDS): measure both the reference and signal levels and subtract them
  - The longer time we measure each, the better the resolution
- Low frequency noise (or “1/f” noise) dominates, changes the reference level
- Total readout time increases linearly with pixel readout time





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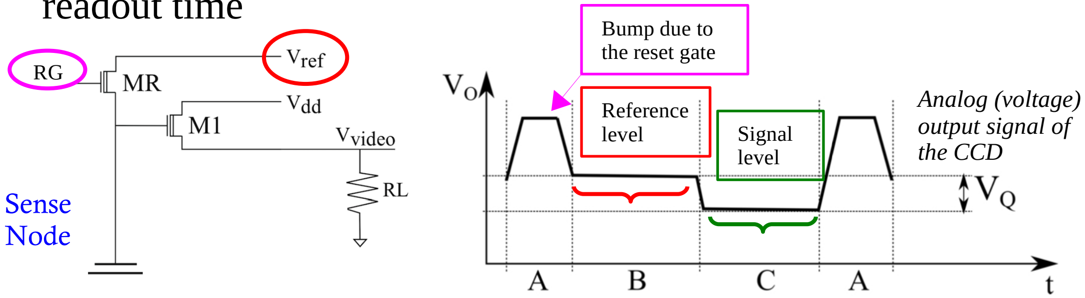
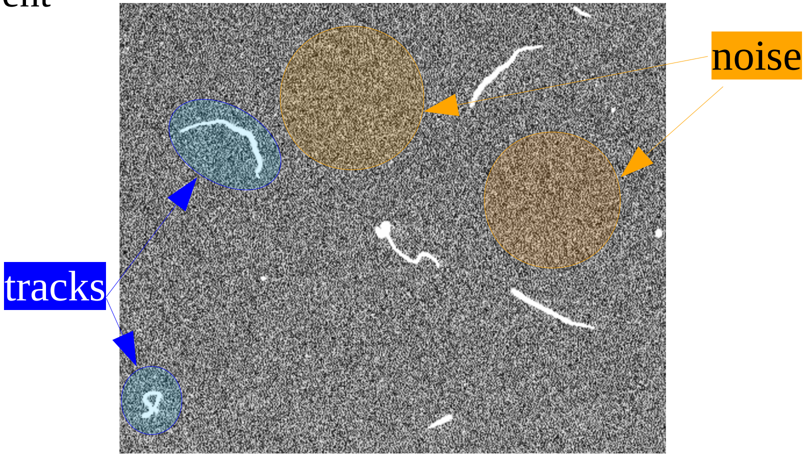


Dark current

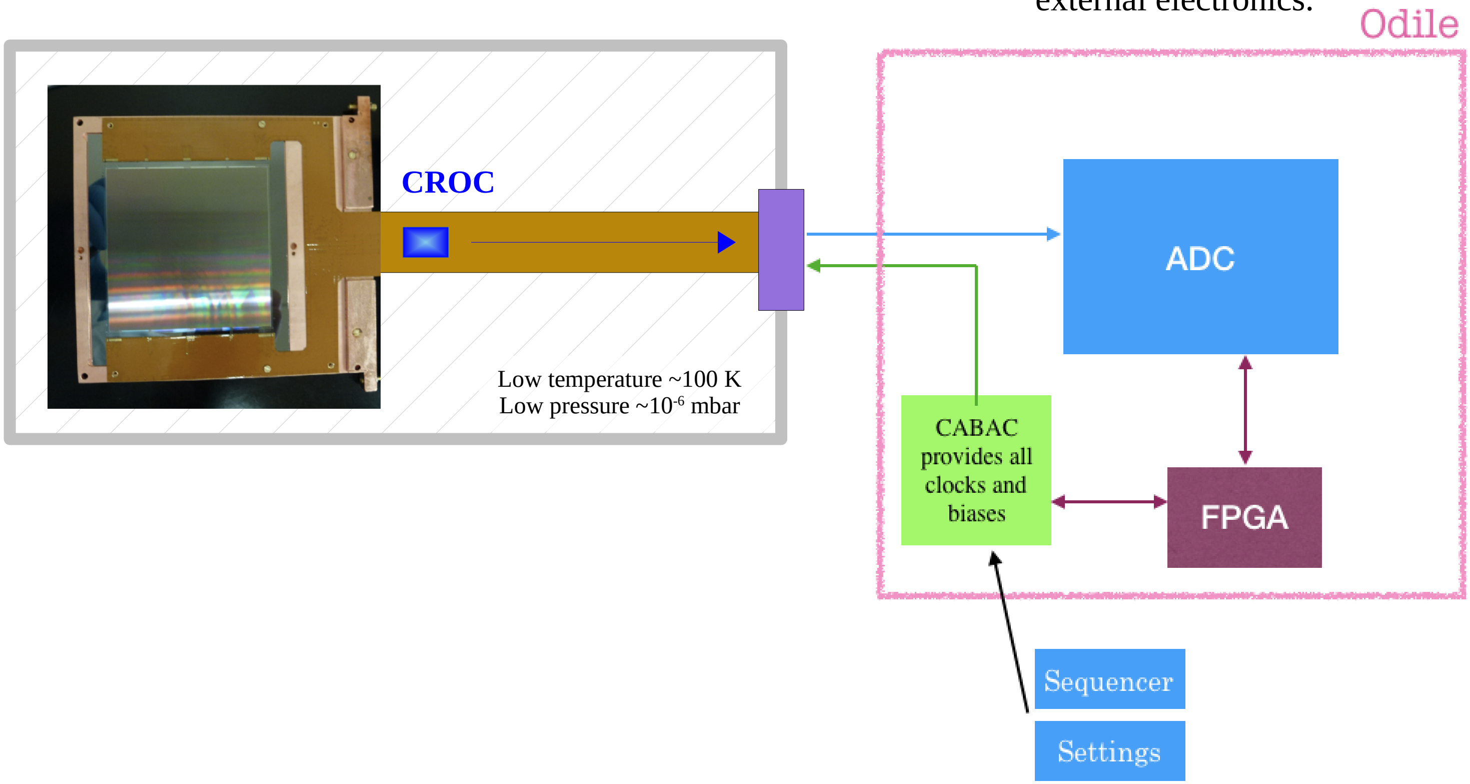
- Thermally generated electrons in the bulk of the CCD
- Depends linearly on the time
- Limits the exposure time
- The longer the exposure time, the worse the Signal to Noise Ratio
  - Lower the temperature (~100K) to decrease the dark current



Real CCD image on surface level

Full Setup & Electronics

A CCD will be supported by external electronics.

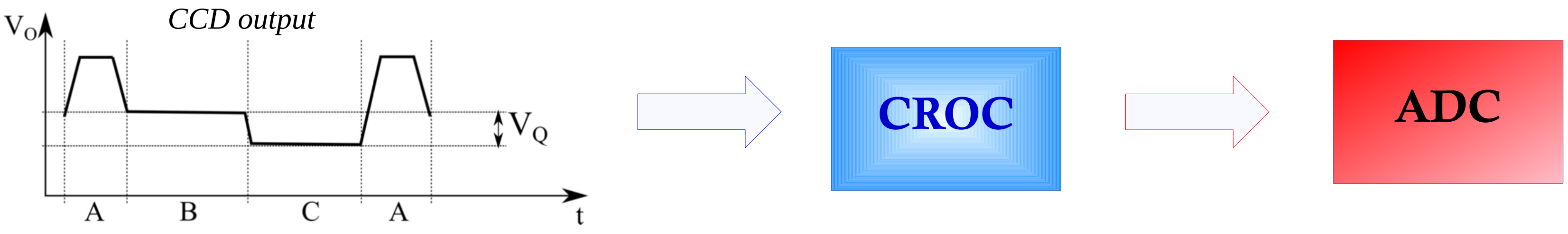


- All voltages and clocks during the expose and readout phases will be provided by the **CABAC** board.
- The **CCD ReadOut Chip** (**CROC**) will preprocess the signal to improve the Signal-to-Noise Ratio.
- An **Analog to Digital Converter** (**ADC**) will preform the transition from the voltage domain to the digital. The ADC can only apply the conversion in certain specified moments.
- Everything is going to be controlled by the FPGA, the brain of the, so called, ***Odile*** motherboard

CROC: Introduction

CCD ReadOut Chip

- CROC processes the CCD output signal and the ADC will perform conversion from analog to digital
- Placed as close as possible to the CCD output to improve the SNR. Amplifying the signal soon, minimizes the effect of any introduced noise until the ADC.
- Single ended input to differential output (CCD output is single ended)
- Dual Slope Integrator (DSI) & Transparent (Digital Correlated Double Sampling - DCDS) modes
- First version under evaluation at room temperature



CROC: DSI mode

The DSI is the dominating mode to be used for the pixel charge measurement. The DSI method combines a *Correlated Double Sampling* and a CCD signal integration.

1) A **reset pulse** sets the CROC input to a voltage reference. Same principle as for the CCD conversion of charge.

2) As the reference level stabilises, the CROC amplifies and **integrates** this level for an integration time t_{int}

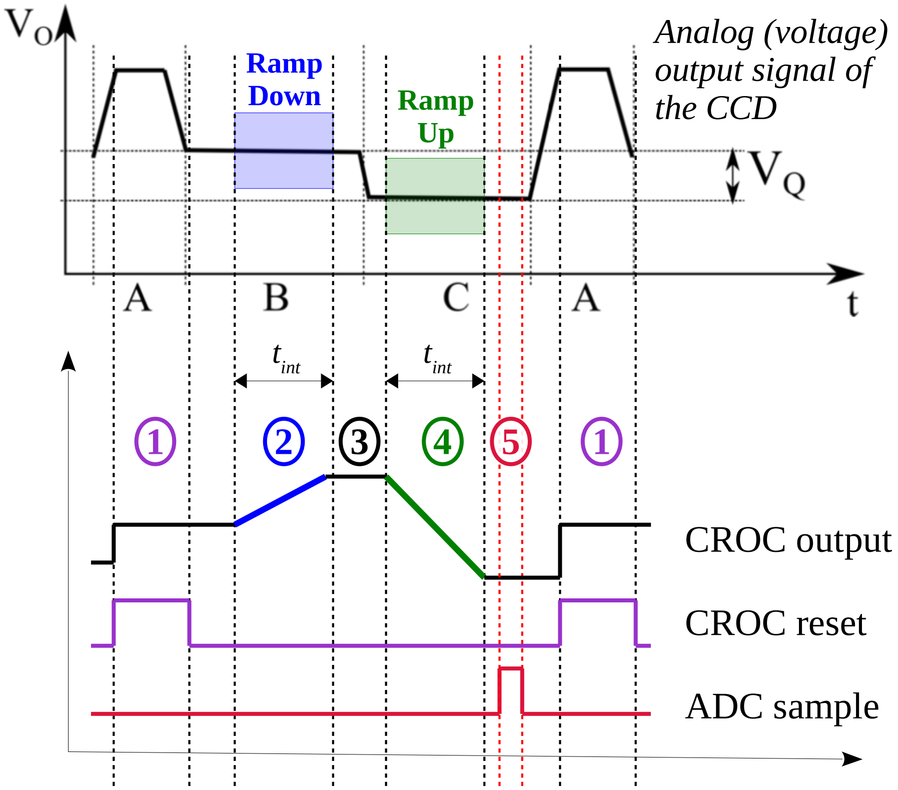
3) The CROC input is isolated while the pixel charge is injected to the Sense Node of the readout circuit.

4) When is stable, the signal level is **integrated** for the same integration time with **reversed polarity** *with respect to the reference level (achieving the CDS)*

5) The **ADC measures** the output of CROC.

- New measurement with a new **reset pulse…**

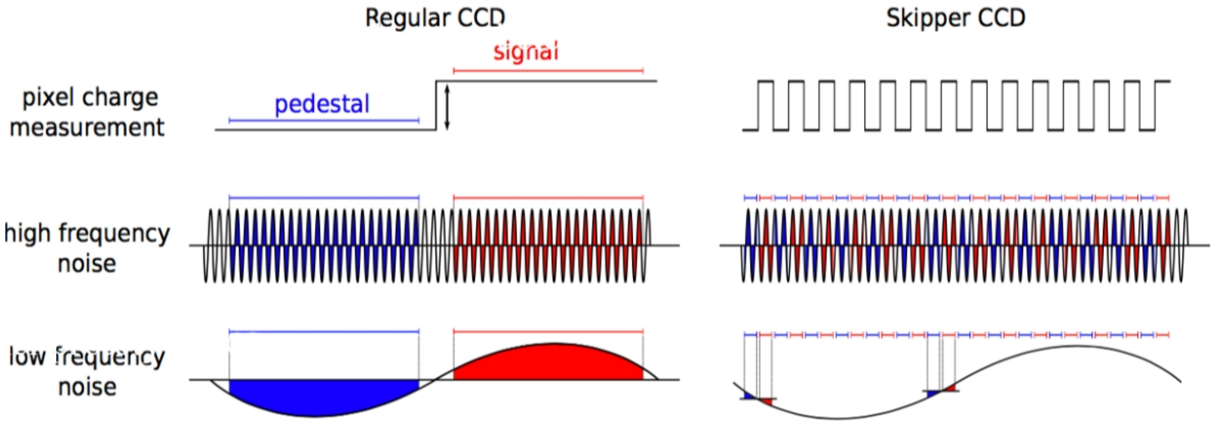
Set reference → measure reference → measure signal → Sample with ADC



CROC: DSI mode

- Regular CCD: integration time $O(10\mu s)$ → high frequency noise is eliminated → low frequency noise dominates
- Skipper CCD integration time $O(1\mu s)$ → low frequency noise eliminated → Small integration time increases the output noise.
- ➢ Multiple measurements of the pixel charge decreases the noise as $1/\sqrt{NDCM}$

- Optimization parameters → integration time
- ADC requirements → sampling frequency ~0.5-1 MHz for integration time ~1μs



CROC: Transparent mode

Alternative method to measure the CCD signal: *Digital Correlated Double Sampling* (DCDS).

- Simpler method, yet more demanding
- CROC operates as a simple single-to-differential gain amplifier, so the CROC output signal will be similar to the CCD's.

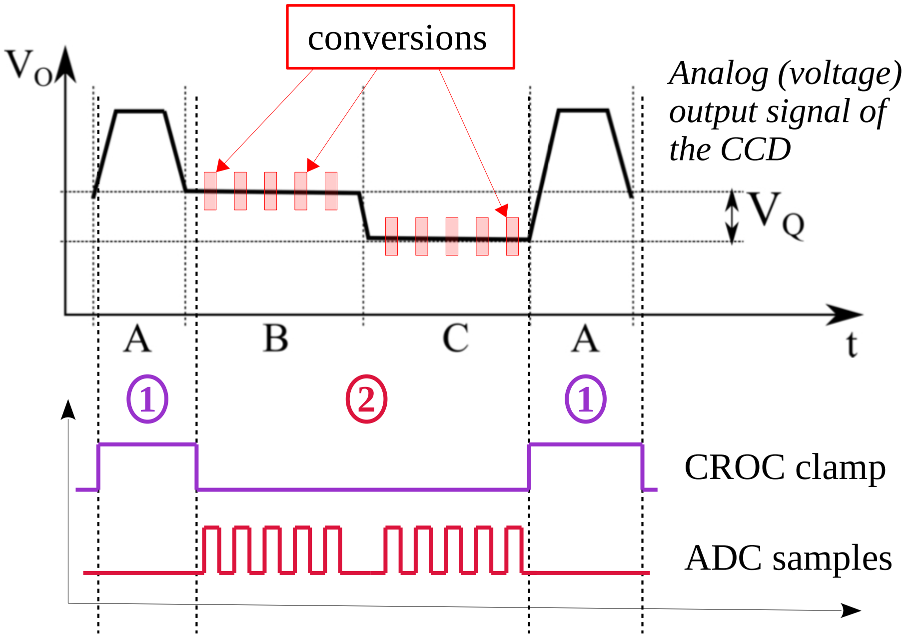
1) Set a reference level to CROC input
2) The ADC oversamples the signal

Advantages

- Digitally determination of the reference and signal level by averaging a sufficient number of samples.
- Further digital analysis is possible.
- High sampling frequency → low frequency noise is eliminated

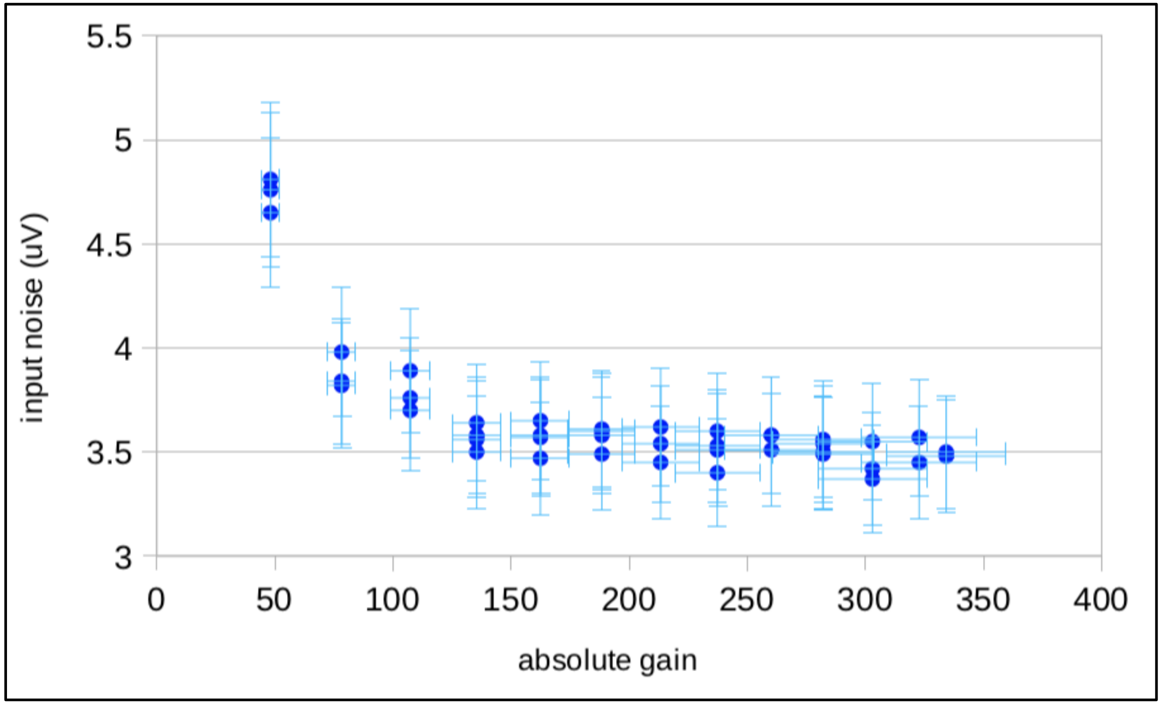
Disadvantages

- Low frequency noise could affect the measurement.
- Fast ADC is necessary → >10MHz.
- The higher the speed of an ADC the lower resolution (N-bits).



CROC: Preliminary results

- Input noise of CROC in Transparent mode at room temperature.
- Input noise = 3.5 μV = ~1-2 e^-



Analog to Digital Converter (ADC)

Transfer from the analog domain (volts) to the digital (ADUs: Analog to Digital Units)

- 3 ADC candidates for the DAMIC-M:
  - AD4020, 20-bit 1.8 MSps 10V_{pp}
  - MAX11905, 20-bit 1.6 MSps 6V_{pp}
  - LTC2387-18, 18-bit 15 MSps 8.192 V_{pp}
- Rapide 4-ADC differential input board

Four aspects are evaluated:

1. Intrinsic noise
2. Linearity – DC input
3. AC input
4. Cross-talk

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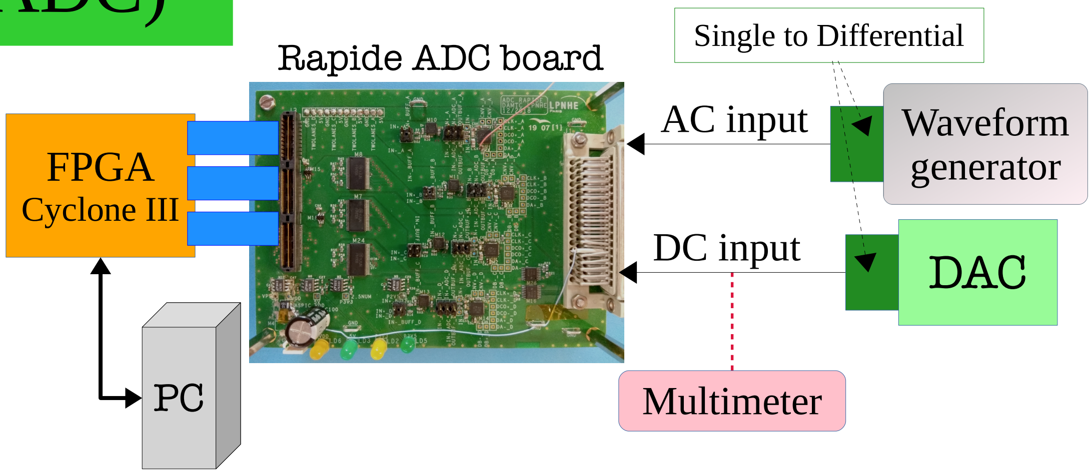
ADC evaluation setup

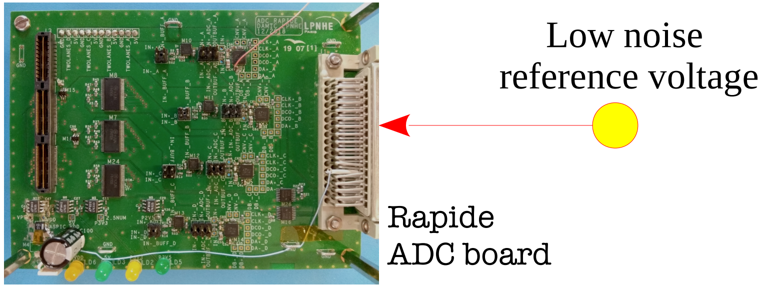


Setup:

- An FPGA to control the ADC
- A low noise *Digital-to-Analog Converter (DAC)*
- A high resolution multimeter
- A waveform generator
- A *Single to Differential Converter* (StD)

1. Intrinsic noise (or transition noise)

* From the 4 ADCs or channels (0, 1, 2, 3) on the board, channel 2 is not working, so the results will include *Ch0,1,3*

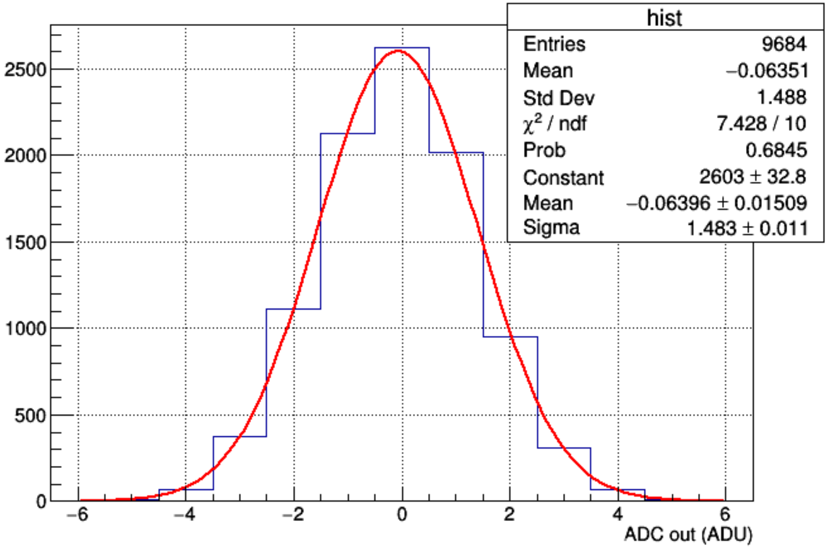


Sort the (+) and (−) of the differential inputs and connect them to a very low noise reference voltage.

For 10 000 samples at a sampling frequency $f_S = 9.091\ MHz$:

Channel	Noise (ADU)
Ch0	1.598 ± 0.012
Ch1	1.591 ± 0.011
Ch3	1.483 ± 0.011

- Expected noise = 1.4 ADU.
- The 1.6 ADU maximum value corresponds to 50 μV input noise.



Histogram of the noise for Ch3

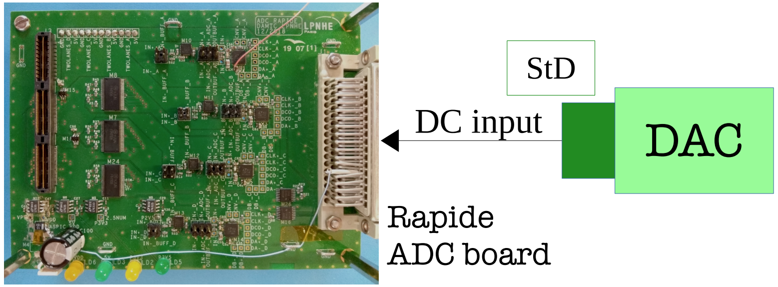
2. Linearity – DC input

Use a DAC to cover the ADC input range. The linearity of the ADC can be presented as the ADC output vs the DAC input. One can calculate the 1 ADU of the ADC in volts from the slope of the linear fit:

$$1\ \mathrm{ADU}^{\mathrm{ADC}} = 31.24\ \mu\mathrm{V}$$

Theoretical resolution of this ADC: 1 ADU = (input range)/2^n

$$1\ \mathrm{ADU} = 31.25\ \mu\mathrm{V}$$



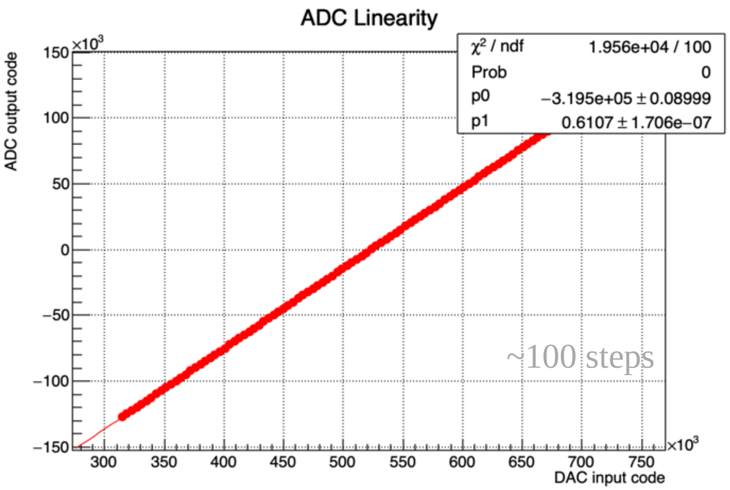


Figure 1. Linearity plot

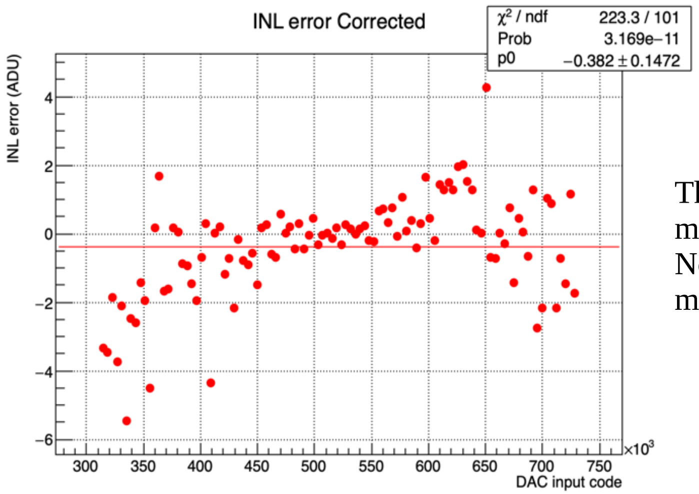


Figure 2. INL error

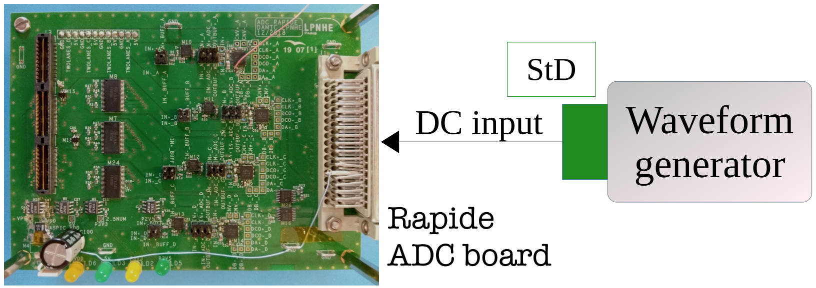
The deviation from the expected value is measured ± 4-5 ADU, while a typical Integral Non-Linearity is expected 0.3 ADU with maximum ± 3 ADU.

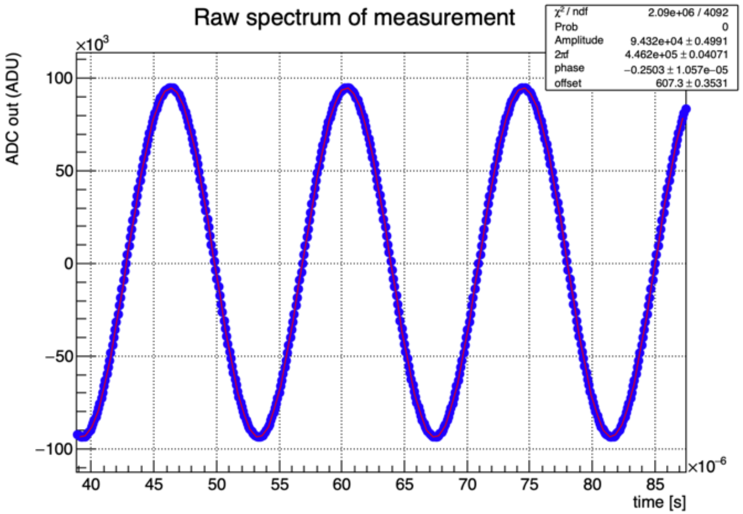
3. AC input – sinusoidal signal

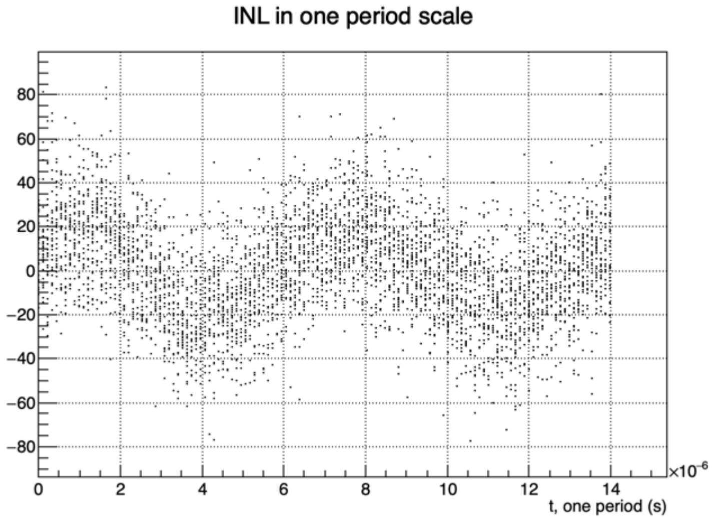
Sinusoidal signals are inserted to the ADC

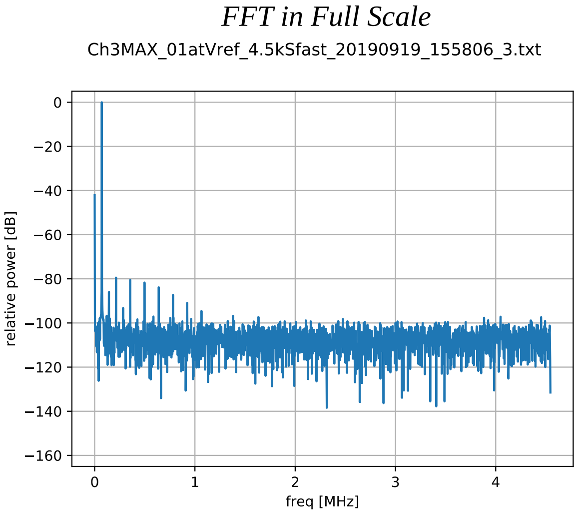
Sampling frequency = 9.091MHz

- Good general response for AC signals
- Some unexplained phenomenons in noise
- High effect of the harmonics in Fourier Transformation plots (peaks at multiples of the input signal frequency)









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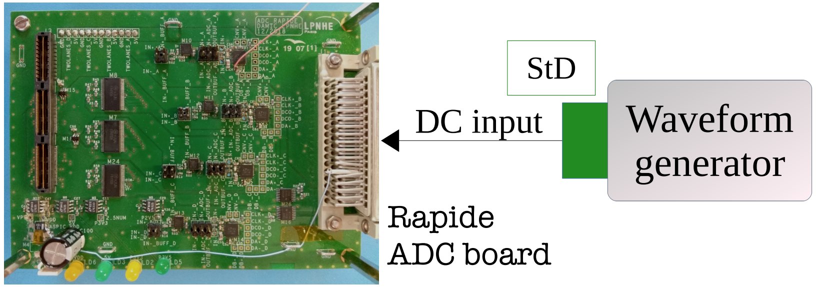
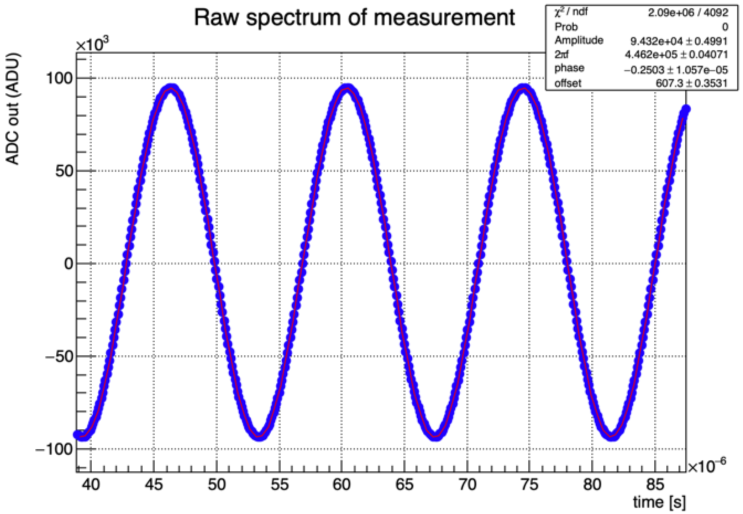
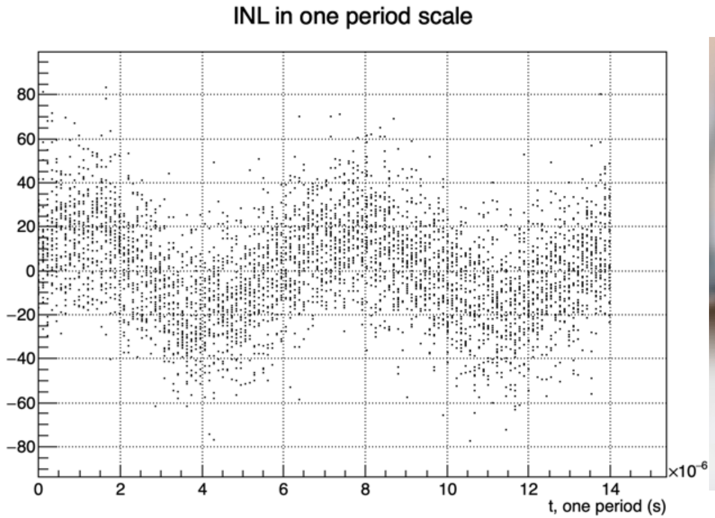


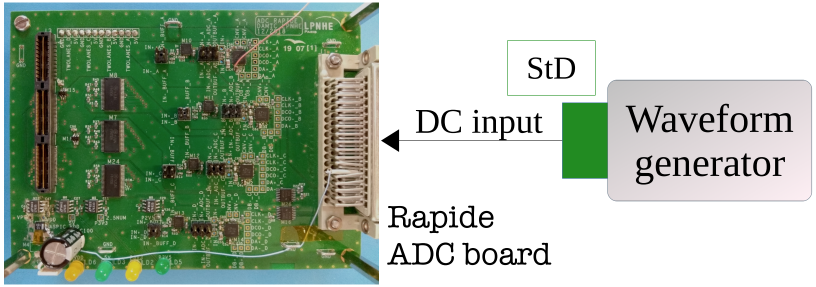




4. Cross-talk

Send signal to a channel and check the rest of the channels for noise increasing or signal pattern output.

- No cross-talk effect is observed.

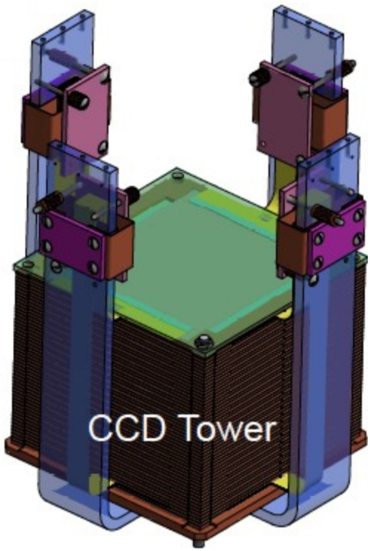


		Signal to:		
		Ch0	Ch1	Ch3
Read signal from:	Ch0	inp signal	1.527 +/- 0.017	1.521 +/- 0.016
	Ch1	1.605 +/- 0.018	inp signal	1.622 +/- 0.019
	Ch3	1.469 +/- 0.016	1.509 +/- 0.018	inp signal

Conclusion

- The CROC chip is operational with very low noise introduction
  - Tests in low temperature
  - Tests with CROC integrated in a CCD setup for real CCD signal as input
  - New upgraded design CROC is under work

- A fast ADC board was evaluated and could support the final experiment
  - New design is under work compatible with CROC
  - Tests in a CCD setup

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DENKAUJA
NENACHALHYA
SIKOMO
MINMONCHAR
MERASTAWHY
GAEJTHO
TAVTAPUCH
MEDAWAGSE
AGUYJE
FAKAAUE
ATTO
LAH

Backup

For “CROC: Transparent mode” slide

Optimal digital correlated double sampling for CCD signals, Stefanov and Murray, 2014

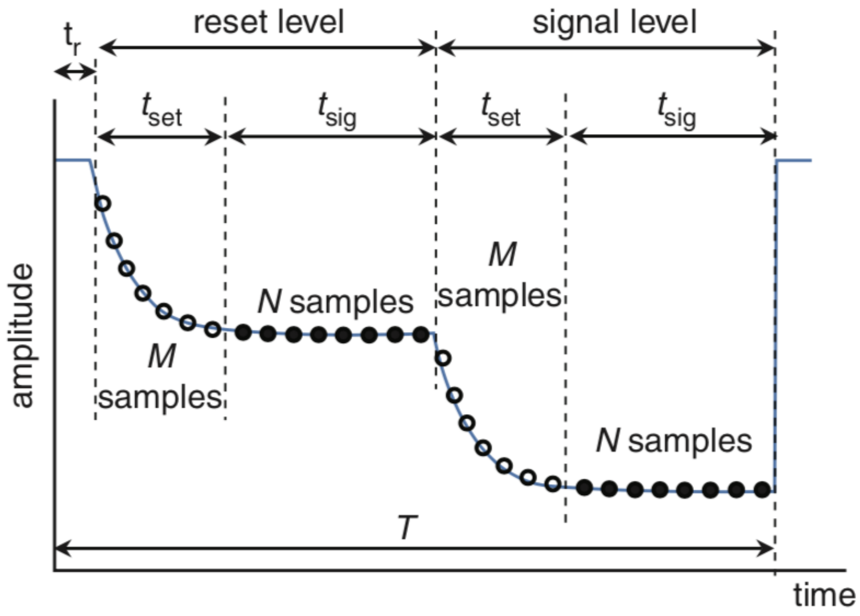

Fig. 1 *Timing diagram of CCD output signal*

Output noise vs integration time