Specifications

Yoshinari Hayato for WG4

High voltage PS requirements

Major requirements

- Positive output
- Voltage 0 ~ 2600V
- Peek current may exceed 500mA
- Resistance ~ 6Mohm nominal 200 ~ 300mA
- Power consumption

Item	Requirements
Output voltage	0 to 2600 V
Accuracy	$< 0.2\%$ (1500 to 2500 V) < 3V (0 to 1500V)
Output current	> 0.5mA/channel
Output stability	$< 0.2\%$ / year
Accuracy of voltage monitor	$< 0.2\%$
Accuracy of current monitor	$< 0.5\%$
Ramp up/down speed	Tunable from 100 to 500 V/s
Ripple noise level	$<$ 10mV p-p at 10kHz
Temperature dependence	50ppm/K
Failure rate (per channel)	$< 1\%$ / 10 years
Power consumption	<~1W / channel @ nominal

Digitizer requirements

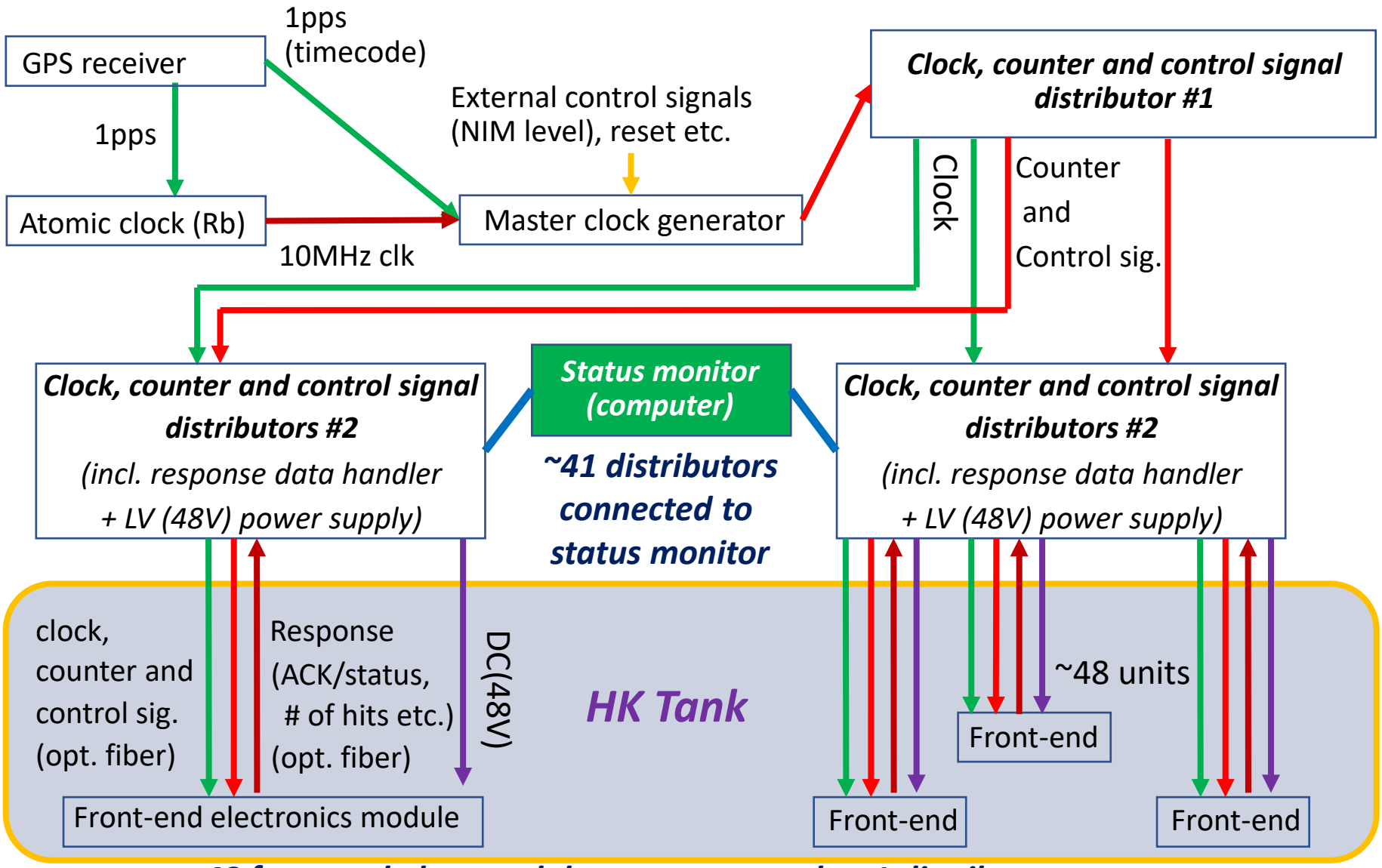
Major requirements

- Self triggering per channel.
- Wide dynamic range.
- Continuous A/D conversion.
- Small channel deadtime (<1us) is acceptable.
- Good timing resolution.
- Low power consumption.

Current baseline option
Charge to time converter (QTC)
CLC 101 (Iwatsu/ICRR)

Item	Requirements
Trigger	self triggering for each channel
PMT impedance	50Ω
Signal reflection	<0.1%
Discriminator threshold	<0.25 p.e. (well below 1 p.e.)
Processing speed/hit (channel dead time)	<1 μs
Maximum hit rate	>1 MHz for each channel
Charge dynamic range	0.1 to 1250 p.e. (0.2 to 2500 pC)
Charge resolution	RMS$\sim$ 0.05 p.e. (below 25 p.e.)
Timing LSB	<0.5ns
Timing resolution	RMS <0.3ns at 1 p.e. RMS <0.2ns above 5 p.e.
Power consumption	<1W per channel

Schematic diagram of the synchronization system



48 front-end elec. modules are connected to 1 distributor

There will be ~41 distributors #2. (#1 and #2 could be identical)

Timing system requirements

Major requirements #1 clock

- Distribute 125MHz (62.5MHz?) clock to all the front-end electronics modules.
- Transmission via Multi-mode optical fiber
- Jitter have to be smaller than ~100ps.

- Reference clock is provided by an external GPS receiver. (10MHz?)
- Delay compensation scheme is necessary.
- However, fixed delay of a few ns is acceptable.
- Delay or phase change is not allowed even after the reset or power cycle.

Timing system requirements

Major requirements #2 counter

- Distribute 32bit counter and auxiliary information to the front-end electronics modules.
- Counter is generated in the master module. Reset is requested by the DAQ system.
- Auxiliary information includes TDC reset, reset and FPGA firmware, i.e. distribution of the new firmware, etc.

- Each front-end electronics module sends back status information, like # of hits in 17 micro sec. (=TDC counter reset interval), status of the module, LV and HV monitor values etc.