The WaveCatcher Systems: a Family of Powerful and Low-Cost Digitizers

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The WaveCatcher systems:

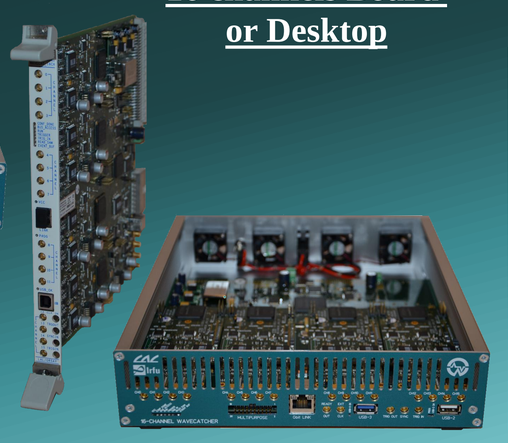
2 to 64-channel 12-bit 3.2GS/s oscilloscope-like digitizers, close to the picosecond level in timing precision

- **Based on the SAMLONG Analog Memory ASIC**
- **Sampling rate ranging between 400 MS/s and 3.2GS/s.**
- **1024 samples/channel**
- **12 bits of dynamic range, working on 14 bits**
- **Small signal bandwidth > 500MHz**
- **Sampling jitter < 5 ps rms at the system level**
- **Up to 64+8-channel synchronous system**
- **Advanced Oscilloscope-Like Software (Plug and Play)**
- **Embedded feature extraction: Baseline, Peak, Charge, CFD (TDC-like mode) …**

2 channels USB powered

8 channels Desktop

16 channels Board or Desktop

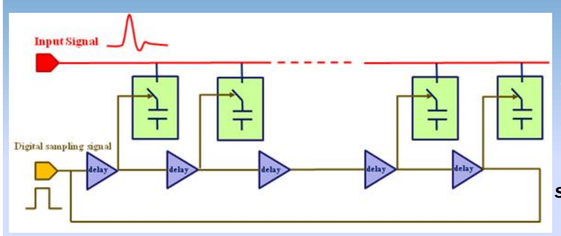


64 channels Mini-Crate

CAEN : 8 to 16 channels

Why Analog Memories

Modern high-end ADCs have broken the GS/s frontier but their implementation becomes difficult. Their companion FPGAs have to be high end and the cost per channel explodes.
The use of analog memories like **SAMLONG** makes it possible to perform high quality digitizing at low cost and with a low power consumption.

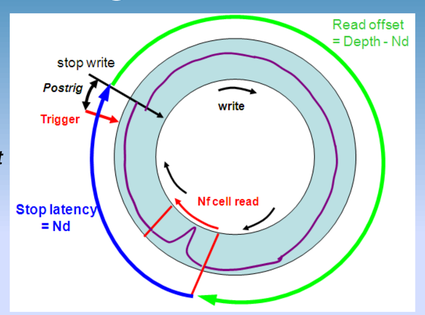


An analog memory: a write pulse is running along a folded delay line (DLL). It drives the recording of signal into analog memory cells.

The Sampling MATRIX

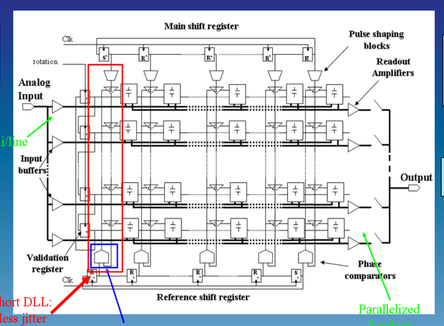
Our sampler chip is made of a matrix of **L lines** and **C Columns** of analog memory cells. Its main clock doesn't exceed 200 MHz. It is virtually multiplied by 16 inside the chip thanks to the 64 vertical **servo controlled** delay line loops (DLL). The input signal is split in 16 branches, each housing a voltage buffer. The chip behaves like an **analog circular buffer**
.

Principle of circular buffer: readout can target an area of interest, which can be only a subset of the whole channel



Sampling at 3.2GS/s

Structure patented in 2001

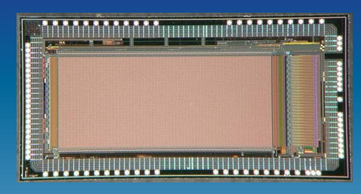


Readout: 12 to 14 bits **10 to 20 MHz**

ADC

Some advantages of the matrix structure:
- Servo-controled DLLs permit **accurate timing**, stable with temperature.
- Input amplifier : stable **high input impedance**.
- 1 Amplifier/Line : better Bandwidth/ Consumption Factor Of Merit
- Channel information spread over numerous lines permits **fast readout**.

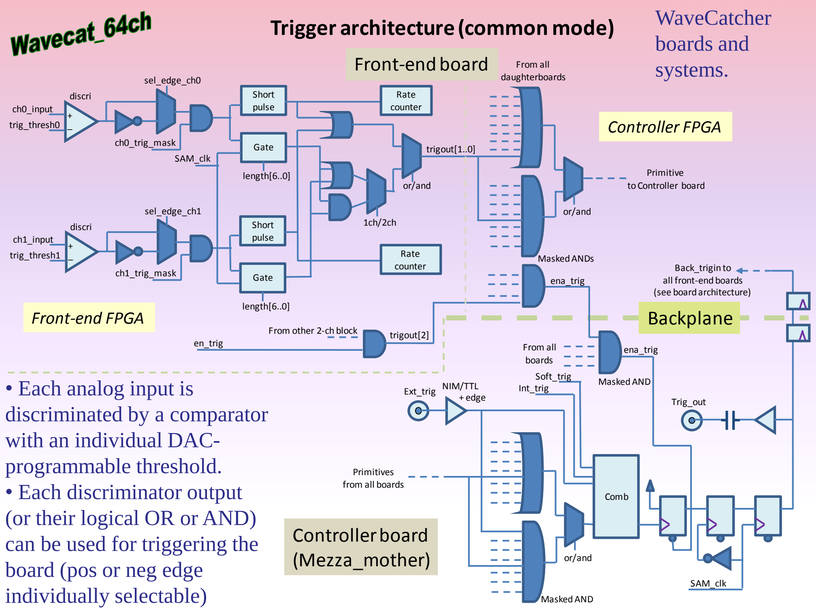
The SAMLONG ASIC



- AMS CMOS 0.35µm technology.
- 2 **differential** channels with 1024 cells.
- Configurable by a SPI-like serial link.
- Embedded DACs for internal tuning
- **"Built-in TDC"**
- 100,000 transistors, 11 mm2
- TQFP 100 14x14 package
- **New: lower power and noise version has been designed (SAMLONG_D) and will soon be mounted on new mezzanine boards**

Trigger & Readout

- Several modes of triggering are available in the WaveCatcher boards and systems.

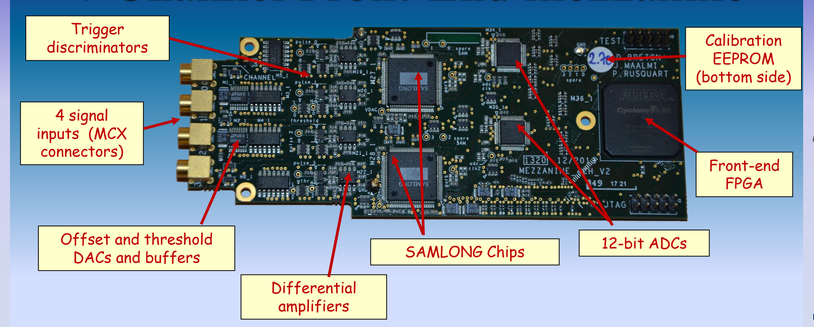


- Each analog input is discriminated by a comparator with an individual DAC-programmable threshold.
- Each discriminator output (or their logical OR or AND) can be used for triggering the board (pos or neg edge individually selectable)

System Features

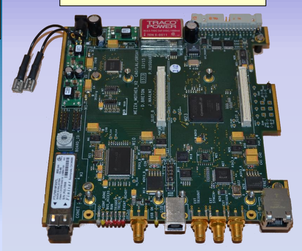
- Possibility to add an **individual DC offset** to each channel
- **Individual** trigger **discriminator** on each channel
- Integrated **raw trigger rate counter** on each channel
- **External** & internal trigger + different modes for **coïncidence** triggering
- 2 **extra** memory **channels** for « digital » signals on 16-channel board => can be used as additional analog inputs
- One **pulse generator** on each input
- External clock input for multi-board applications (8, 16 & 64-channel)
- Embedded USB, UDP and Gigabit optical interfaces (8, 16 & 64-channel)
- Possibility to upgrade the firmware via USB
- Embedded **charge** extraction
- Embedded signal **amplitude** and **baseline** extraction
- **Embedded digital CFD** for time measurement

4-Channel Front-End mezzanine



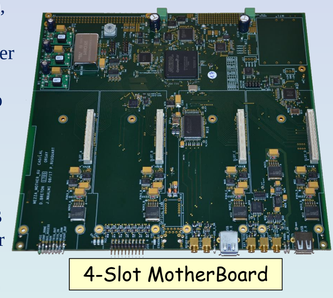
MotherBoards

2-Slot MotherBoard



Control and Readout motherboards have been developed for housing 2 or 4 mezzanines.
They permit separating the acquisition part from the specific front end part.

- The control and readout is possible through USB(2.0), UDP or Optical links (Ethernet over optical)
- The next step is to develop the 2.5 Gbits/s USB3 interface.
- Firmware can be uploaded via USB using the fwloader tool developed at LAL (C.Cheikali)

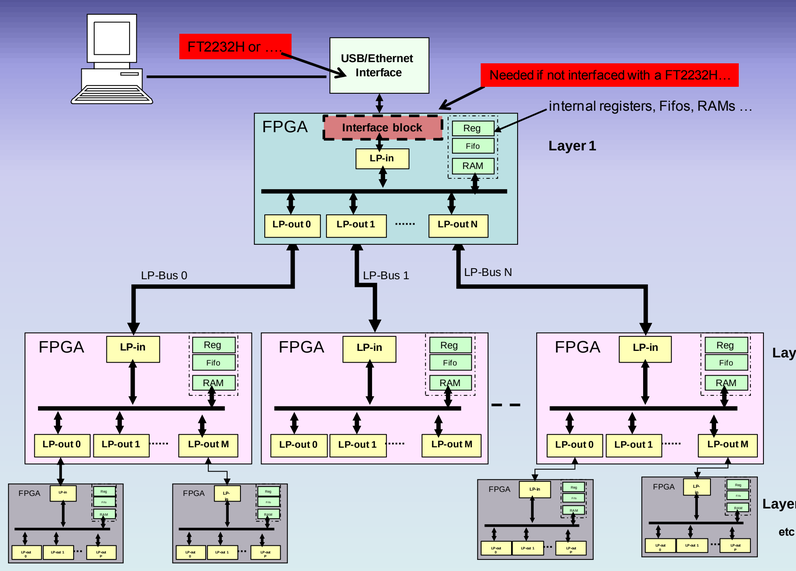


4-Slot MotherBoard

Application Examples

These acquisition systems are used in test benches or experiences in a multitude of labs, projects and fields:
- particle beam monitoring
- accelerators
- R&D on detectors
- study of new fast photo-detectors (SiPMs, MCP-PMTs, MeshAPDs)
- new generation of detectors (LGAD, pico-second Micromegas, diamonds) for high energy physics
- research on TOF-PETs for medical imaging
- particle physics detectors...

A Custom Control & Readout Architecture and Protocol

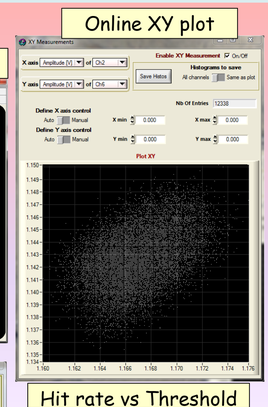


- The **Multi-Layer Parallel Interface** aims at simplifying the communication between FPGAs located at different levels in the system.
- **The same firmware** decoding blocks are implemented in the FPGAs **independently of their hierarchy level** in the system (same or different boards).
- **Software Libraries:** *LAL_USB_ML* and *LAL_UDP* libraries have been developed to handle the ML communication protocol. **UDP transfers are secured** with warranty of **no data loss** thanks to a continuous handshake between the firmware and the library .

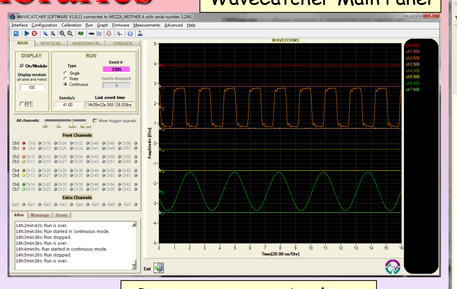
Dedicated software and C-libraries

- A dedicated **Software**, compatible with all WaveCatcher modules (from the 2-channel module to the 64-channel crate) has been developed under Labwindows CVI. It permits configuring all the available parameters on the modules, visualising and saving data (ASCII or Binary) but also making different online histogramming of: Differential Time Jitter, Amplitude, Charge, Baseline, XY plots… Unfortunatey, this Software runs only on Windows.
- A **dedicated C-library**, compatible with **Windows** and **Linux** allows the users to build their own DAQ software (via USB or UDP). It permits initializing, configuring and reading out the WaveCatcher Modules
- Documentation is available for Software, Library and Modules.
- A dedicated **website** houses all information and updates for Software, Firmware and Library.

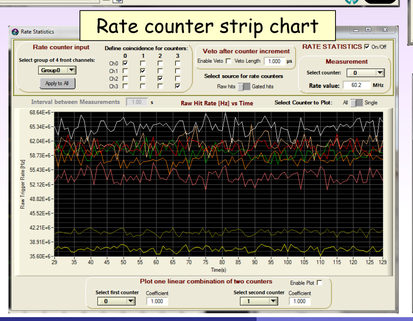
Online XY plot



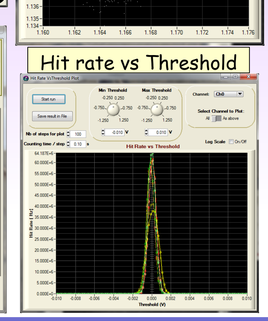
WaveCatcher Main Panel



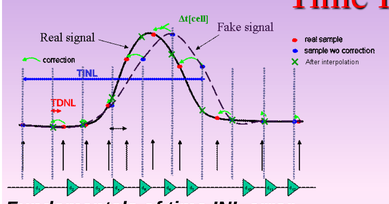
Rate counter strip chart



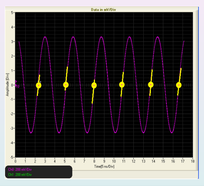
Hit rate vs Threshold



Time INL Calibration



Fundamentals of time INL error (same problem occurs with interleaved ADCs)

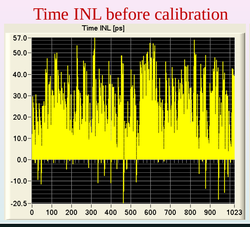


Zero-crossing segments of the sine-wave are considered as straight lines

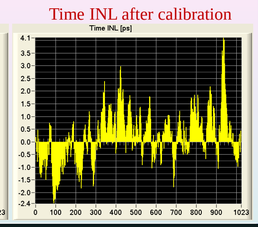
Calibration method:
We send a **sine-wave** signal to even then to pair channels, and we measure the length of the zero-crossing segments (*method we introduced in 2009*)
A dedicated 16-channel sine-wave generator box has been developped for this purpose: less than 2 minutes are needed to calibrate a 16 channel board at a few ps level!

Calibration signal generator

Time INL before calibration



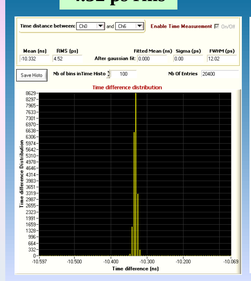
Time INL after calibration



Differential Time Jitter

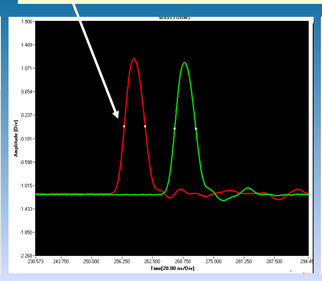
2 pulses, 2.5 ns risetime, 1.2V, Δt ~ 10 ns

4.52 ps rms



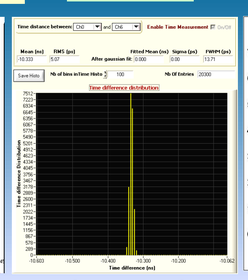
Δt measured by software

CFD points received from firmware



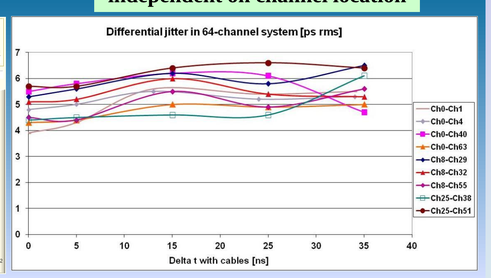
The 2 pulses recorded by the WaveCatcher board

5.07 ps rms



Δt measured by firmware

Differential jitter between channels: 4 to 7 ps rms, almost flat and independent on channel location



Jitter on Δt measurement in the 64-channel system, measured with cables

Summary

		Unit
SAMLONG ASIC technology	AMS CMOS 0.35µm	
System number of channels	2, 8, 16, 32, 48, 64	
Power consumption	2.5 (2-ch), 15 (8-ch), 23 (16-ch), 100 (64-ch)	W
Sampling depth	1024 / channel	Cells
Sampling speed	0.4 to 3.2	GS/s
Bandwidth	500	MHz
Range (unipolar)	± 1.25 (with full range individual channel offset)	V
ADC resolution	12	bits
Noise	0.75	mV rms
Dynamic range	11.5	bits rms
Readout time	11 to 66 (depends on number of cells read)	µs
Time precision before correction	< 20	ps rms
Time precision after time INL correction	< 5	ps rms

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