SAMPIC: a 16-channel Waveform-TDC for picosecond time measurement

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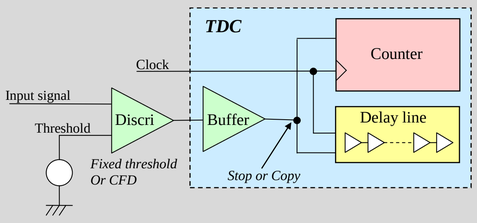
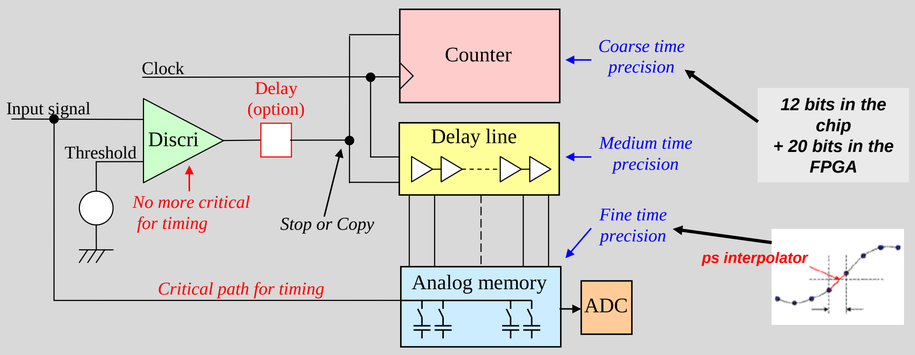
Waveform-TDC vs usual TDCs



Principle of usual DLL-based TDCs

A Time to Digital Converter is a circuit which works on a **digital** input signal:
⇒ **analog** signal from detector first has to be translated to digital with a **discriminator**
⇒ **additional jitter** and **residues of time walk** effect add up to the TDC own limits
⇒ overall timing resolution is given by the **quadratic sum of the discriminator and TDC timing resolutions** => **~ 20 ps rms for today's best solutions**



Principle of the Waveform TDC (patented)

An **analog memory** is added in parallel with the delay line. It samples the input signal which can now be analog and permits performing an interpolation of the samples recorded on the latter.
⇒ **the discriminator is no longer in the critical timing path**
⇒ **time resolution can reach a few ps rms, even on small analog signals !**

Project goals & Design principles

• We developed a **multi-channel scalable acquisition system** (ASIC, boards, software) for **picosecond** time measurement using the new **WTDC** (Waveform Time to Digital Converter) concept integrated in the new **SAMPIC** ASIC:
• The inputs directly receive the (amplified) **analog signal** coming from the detector.
• It is sent to both:
  • a **discriminator** with programmable threshold
  • an **analog memory** driven by a **Delay Line Loop** whose total delay is servo-controlled to the clock period of a **timestamp counter**.
• The discriminator output :
  • catches the state of the counter output: **coarse** timestamp (down to 6.4 ns steps)
  • catches the state of the DLL, giving a **medium** precision (down to 100 ps steps)
  • stops the waveform sampling which will give a **few ps** time precision after **interpolation** of the analog samples.

Applications

• All the new fast (photo)detectors: MCP-PMTs, diamonds, APDs, SiPMs , LGADs, …
• Test benches for fast detector characterization, TOF detectors, particle identification, pile-up rejection, TOF-PETs, muon detectors, …

Project schedule

• Project started in **January 2012**. **May 2013**: submission of **SAMPIC_0**, demonstrator ASIC for technology evaluation & validation of the WTDC principle..
• **November 2014**: submission of **SAMPIC_V1** with a few bug corrections and new design of the analog sampling cell => better linearity and dynamic range
• **November 2015**: submission of **SAMPIC_V2** with advanced features (input block, 16-bit timestamp, gated trigger coincidence, independent channel ADCs, TOT measurement & filter …)
• **November 2016**: submission of **SAMPIC_V3** with a few bug corrections and addition of other advanced features (self calib, ping-pong, channel chaining, trigger multiplicity, smart posttrig, …)
• **December 2017**: submission of **SAMPIC_V3D** with the last corrections. **1400 chips produced**.

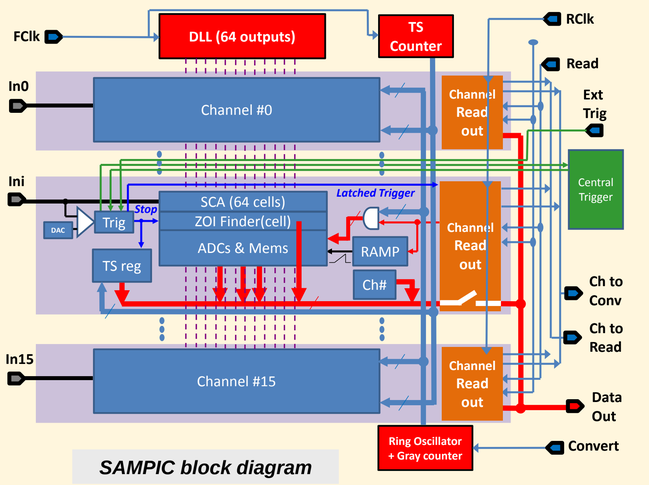
Main results

• **The chip is fully functional** (SPI interface, waveform sampling, triggering, time stamping, 1.3GHz Wilkinson ADCs, readout (up to 240 MHz => 3Gbits/s), self time calibration …)
• **~10 mW / channel**
• Sampling rate from **0.8 to 8.5 GS/s**
• **>> 1 GHz** analog bandwidth
• Input range **~ 1 V**
• Noise **~ 1mV rms => ~ 10-bit rms dynamic range**
• Conversion ranges from **7 bits (100ns) to 11 bits (1.6µs)**
• **TOT measurement and filter between 2.5 and 700 ns.**

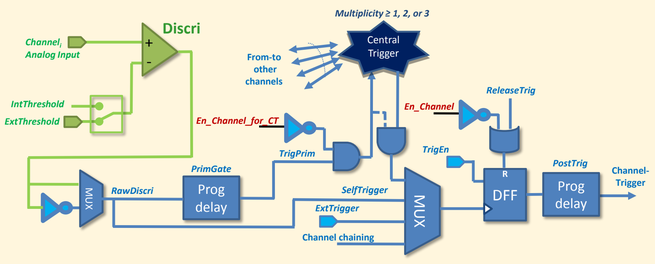
• **Single channel time resolution:**
~ 3.5 ps rms

The SAMPIC ASIC

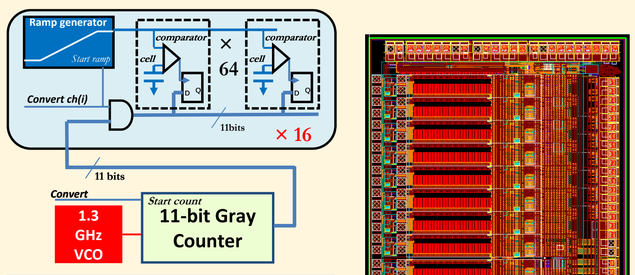
• **16 single-ended channels**:
  • Independent and self triggered (or Central Majority Trigger, or External Trigger)
  • 64 analog sampling cells/ch
  • One 11-bit ADC/ cell (total : 64 x 16 = 1024 on-chip ADCs)
• **One common 12-bit Gray counter** (@160MHz) for coarse time stamping
• **One common servo-controlled DLL**: (from 1,6 to 10 GS/s) for medium precision timing & analog sampling
• **One common 11-bit Gray counter** running @ **1.3GHz** and used for the massively parallel Wilkinson ADC conversion (**7 to 11 bits**)
• **Several trigger modes available, including majority trigger**
• **Integrated TOT measurement & Filter ***
• **Integrated smart readout**: 12-bit LVDS readout bus (running up to 240 MHz)
• **SPI Link** for register
• **Technology: AMS 0.18µm CMOS, now moving to TSI 0.18µm**
  • Mixed analog/digital design
  • Low cost, low leakage
  • High end technology
• Size: **8 mm²**
• Package: **128-pin QFP, pitch of 0.4mm**



SAMPIC block diagram

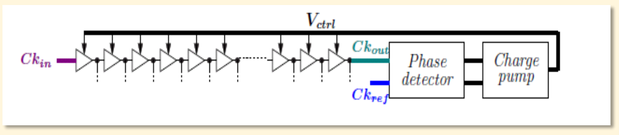


Channel trigger scheme



Principle of internal massively parallel Wilkinson ADC

Layout of SAMPIC _V3



Principle of the single 64-cell DLL driving the 16 channels. It ensures a constant width to the write pulse even after trigger.

SAMPIC on board

The SAMPIC module & DAQ Systems

• **Plug and play philosophy**
• Motherboards housing 1 to 4 mezzanines
  • **16-, 32-, 48- and 64-channel** systems
• New **64-channel board**
• **256-channel** mini-crate **soon** available
• Portable data readout
• **Acquisition software with GUI** for measurements, calibration & data display
• Includes timing extraction algorithms
• Special visualization for **WTDC mode (waveforms are located on the display at their real time location) USB and UDP DAQ** (Copper / Optical link)

New SAMPIC modules (desktops & VME boards) will soon be developed by CAEN

SAMPIC 16-channel mezzanine

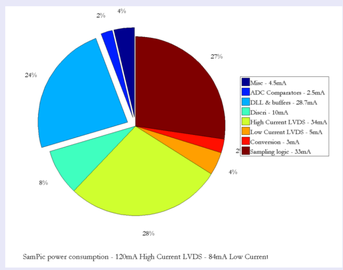
The new 64-channel SAMPIC board

Different SAMPIC readout modules

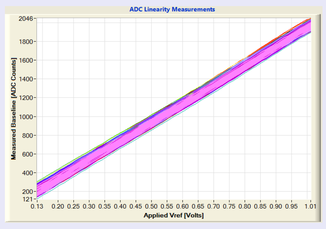
SAMPIC acquisition software GUI in WTDC mode

Performance Summary

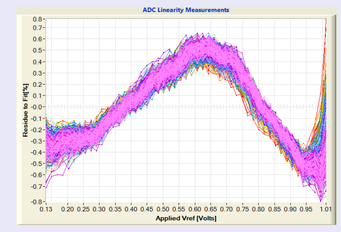
		Unit
Technology	AMS CMOS 0.18µm	
Number of channels	16	
Power consumption (max)	180 (1.8V supply)	mW
Discriminator noise	2	mV rms
SCA depth	64	Cells
Sampling speed	0.8 to 8.5 (10.2 for 8 channels only)	GSPS
Bandwidth	>> 1	GHz
Range (unipolar)	~ 1	V
ADC resolution	7 to 11 (trade-off time/resolution)	bits
SCA noise	< 1	mV rms
Dynamic range	> 10	bits rms
Conversion time	0.1 (7 bits) to 1.6 (11 bits)	µs
Readout time / ch @ 2 Gbit/s (full waveform)	< 450	ns
Single Pulse Time precision before correction (4.2 to 8.5 GS/s)	< 15	ps rms
Single Pulse Time precision after time INL correction (4.2 to 8.5 GS/s)	< 3.5	ps rms



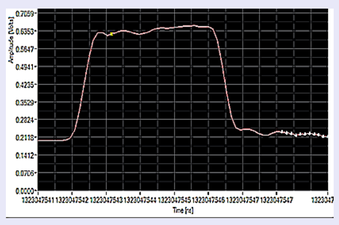
Consumption map : no more than 10-15 mW /ch



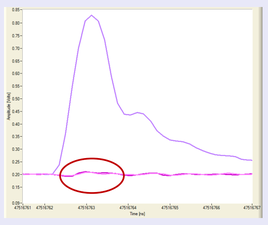
ADC linearity: all cells



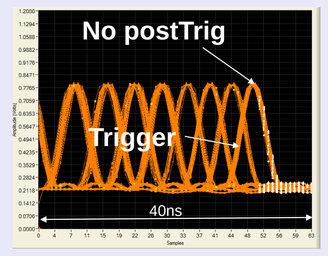
ADC linearity residue to linear fit (%): all cells



Signal with rise time of 400 ps is accurately recorded.



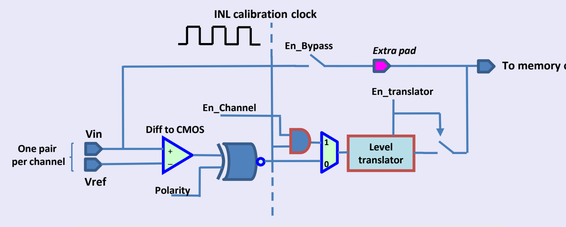
Crosstalk with neighbor channels is < ± 1,5%



Effect of PostTrig adjustment

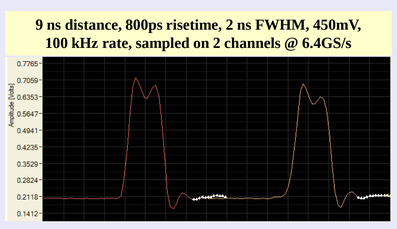
SAMPIC new input block

In order to permit performing a **standalone calibration** and dealing with **small differential digital signals**, the chip houses a dedicated input block on each channel. The latter includes a fast discriminator and edge selection. It can be switched off and **bypassed** in order to retrieve the usual analog waveform recording mode.

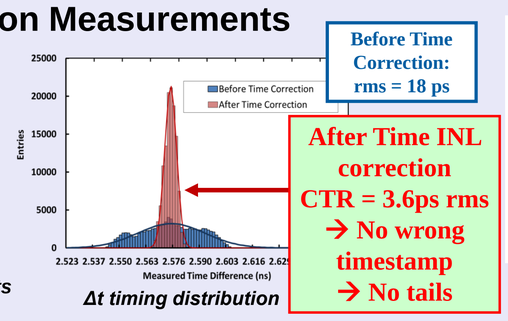


Simplified scheme of SAMPIC input block

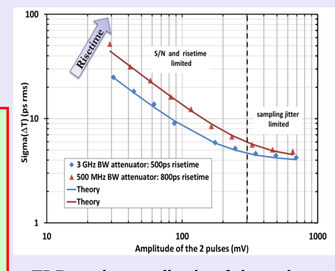
Time Difference Resolution Measurements



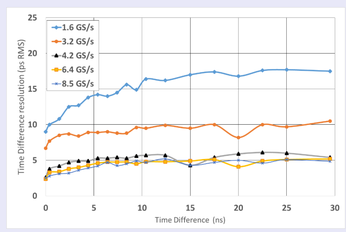
Examples of pulses used for Δt measurements



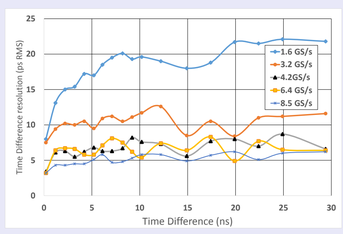
Δt timing distribution



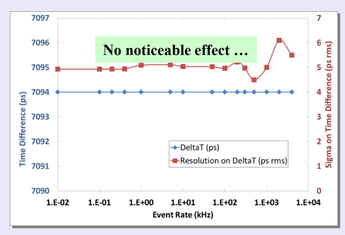
TDR vs the amplitude of the pulses for two different risetimes



Time difference resolution vs delay (made by cables).

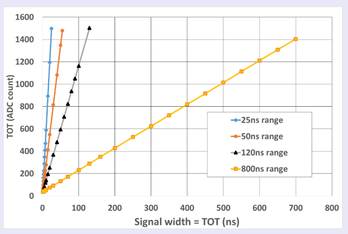


Time Difference Resolution vs delay: internal time calibration

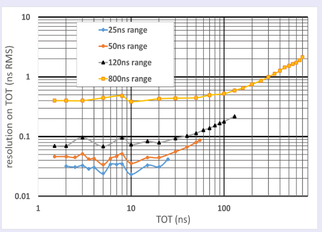


Time Difference Resolution vs input signal rate

Time Over Threshold Measurements

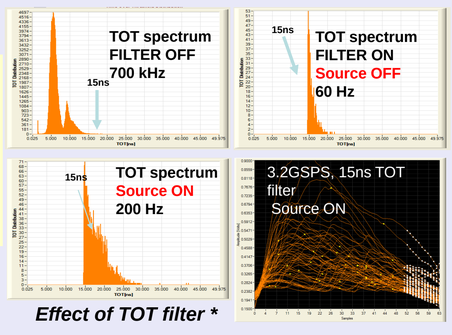


Examples of measured TOT ranges



Measured TOT resolution for different ranges

Use of TOT filter* and TOT measurement for 150Hz Na source signal extraction with PbWO4 crystal and KETEK 3x3 mm² SiPM @ 20° C



*Effect of TOT filter **

** The **TICAL** ERC project (grant number 338953 from EU; PI: Paul Lecoq) has also contributed to the developments of the TOT features integrated in the chip*

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