

AN 807: Configuring the Intel® Arria® 10 GX FPGA Development Kit for the Intel® FPGA SDK for OpenCL™



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AN-807 | 2018.05.04

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Configuring the Intel® Arria® 10 GX FPGA Development Kit for the Intel® FPGA SDK for OpenCL™

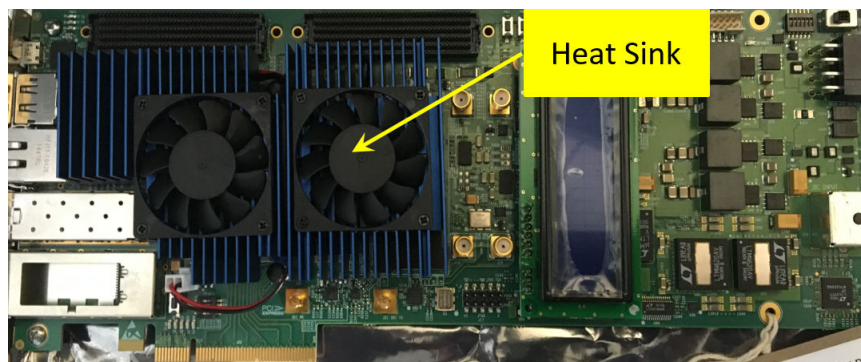
You must complete the instructions in this document before you can use your Intel® Arria® 10 GX FPGA Development Kit with the Intel FPGA SDK for OpenCL™. The instructions require you to be familiar with Intel Quartus® Prime software and hardware assembly to avoid damaging the Intel Arria 10 GX FPGA Development Kit PCIe card.

The instructions in this document are best carried out by or with the assistance of an Intel Programmable Systems Group Field Application Engineer.

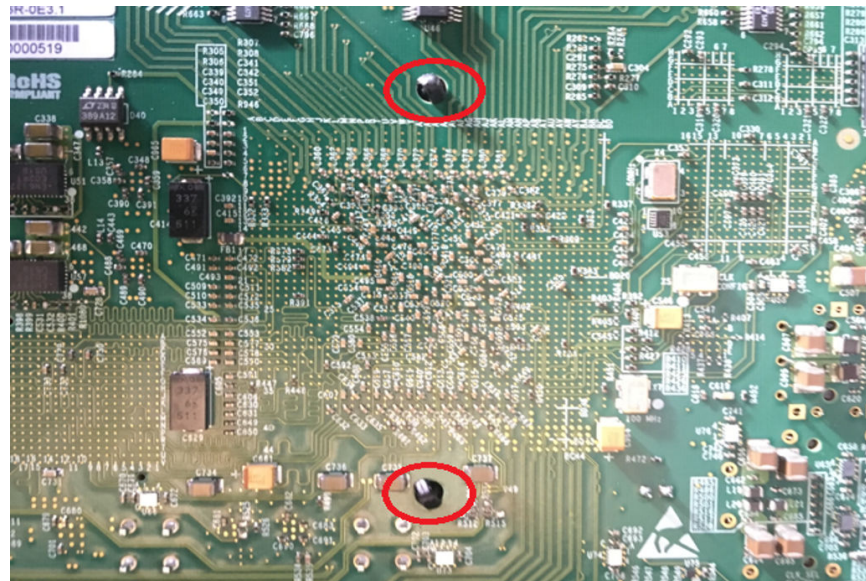
Configuring and installing the Intel Arria 10 GX FPGA Development Kit board

To use the Intel Arria 10 GX FPGA Development Kit with the Intel FPGA SDK for OpenCL, you must install the DDR4 memory module, configure certain DIP switches on the board, and add the board to your host system.

1. Install the DDR4 memory module as follows:
 - a. Locate the heat sink on the Intel Arria 10 GX FPGA Development Kit board:



- b. Remove the heat sink from the board by squeezing and pushing out the two pins from the back of the board.



- c. Locate the HiLo connector that was previously hidden by the heat sink



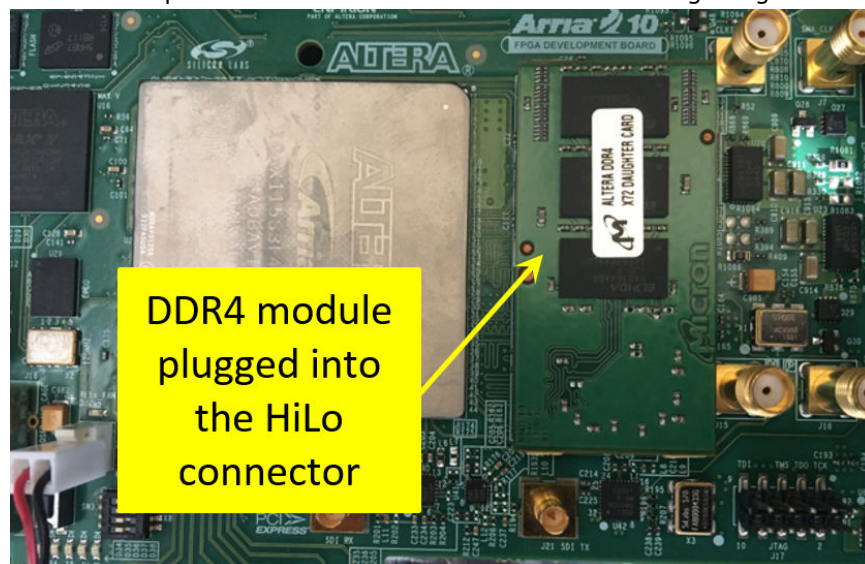
- d. Plug the DDR4 memory module into the HiLo connector.



The DDR4 memory module provided with the Intel Arria 10 GX FPGA Development Kit looks like the following image:



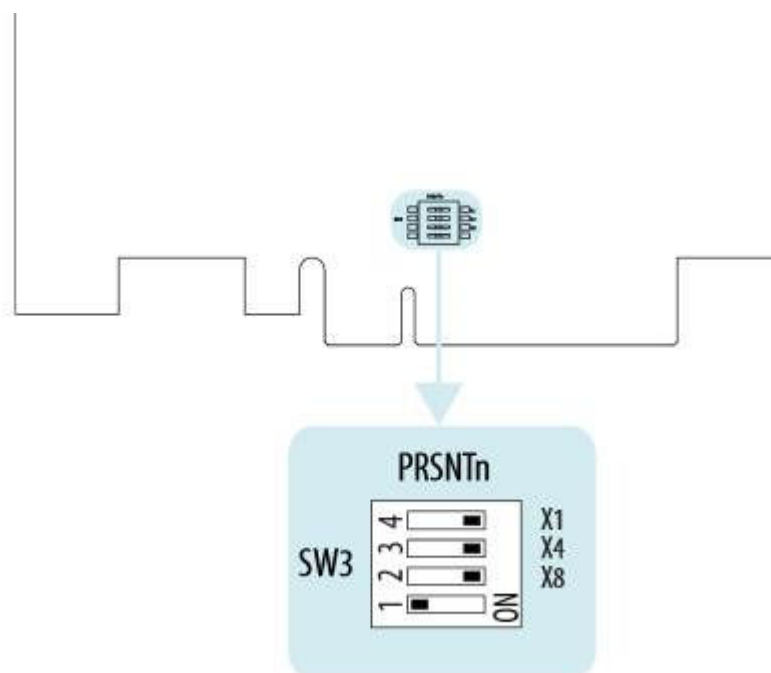
After you have plugged in the DDR4 memory module, your Intel Arria 10 GX FPGA Development Kit card should look like the following image:



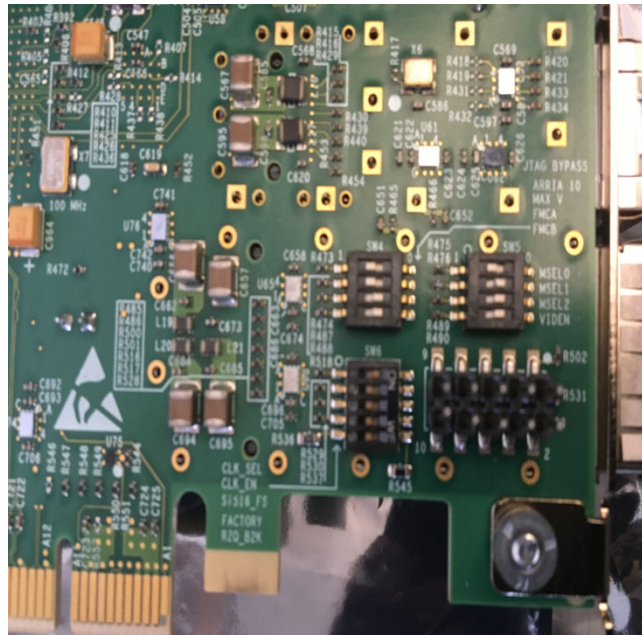
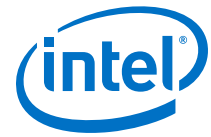
- e. Reinstall the heat sink on the board. Make sure that the two fans are visible.
2. Configure the following DIP switches: SW3, SW4, SW5, and SW6:
 - a. Locate the SW3 DIP switch on the front of the board:



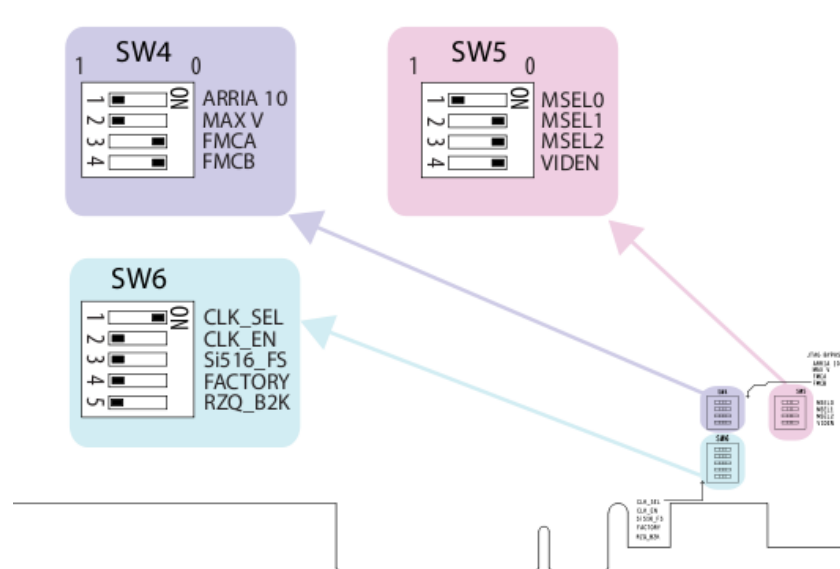
- b. Ensure that the SW3 DIP switch is configured as follows:



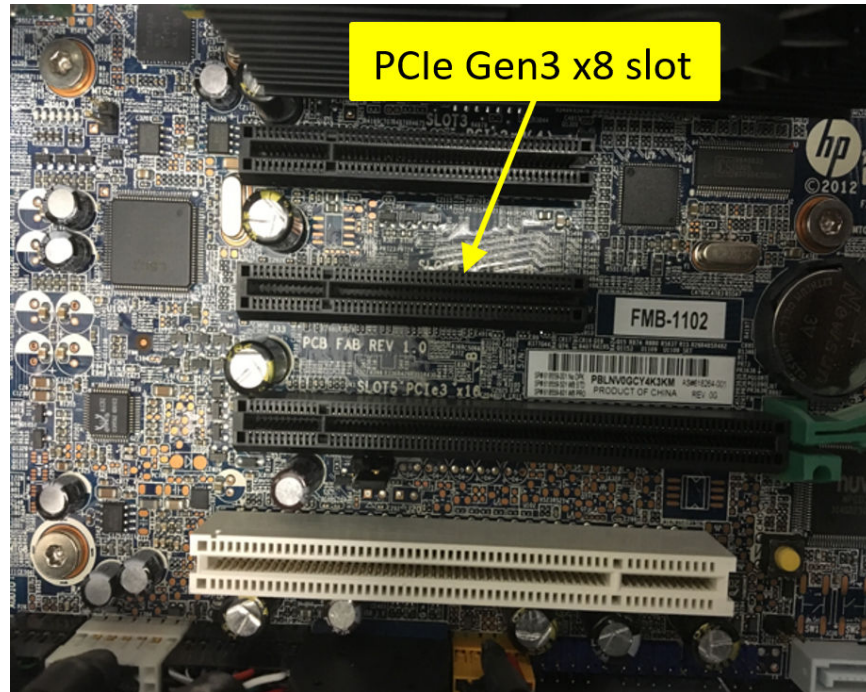
- c. Locate the SW4, SW5, and SW6 DIP switches on the back of the board:



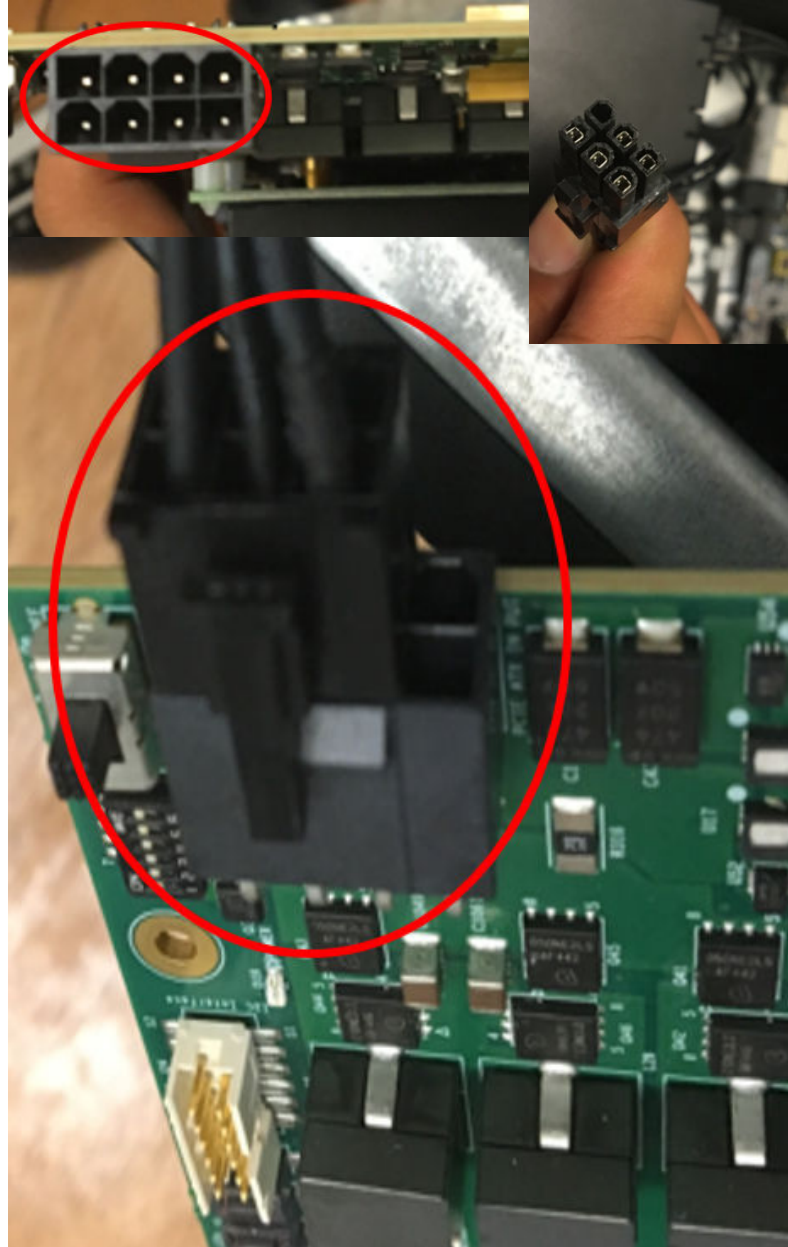
- d. Ensure that the SW4, SW5, and SW6 DIP switches are configured as follows:



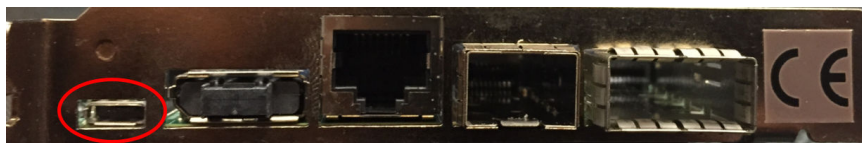
3. Add the Intel Arria 10 GX FPGA Development Kit card to your host system:
- Plug the card into a PCIe Gen3 x8 slot on your host system.



- b. Connect the 6-pin power cable to the card.



- c. Connect the card to your host USB subsystem using the micro USB cable.



After you have configured and installed the hardware, you must initialize the Intel Arria 10 GX FPGA Development Kit for use with OpenCL.

Initializing the Intel Arria 10 GX FPGA Development Kit for use with OpenCL

Before you can use the Intel Arria 10 GX FPGA Development Kit with OpenCL, you must initialize the board with an OpenCL image. Without this image, the board host operating system does not recognize the PCIe card and the Intel FPGA SDK for OpenCL Offline Compiler cannot find the device.

Before you initialize the Intel Arria 10 GX FPGA Development Kit for use with the Intel FPGA SDK for OpenCL, install the following software on the system where you installed the PCIe card:

Intel FPGA Download Cable driver

Download the Intel FPGA Download Cable driver from the Intel FPGA Cable and Adapter Drivers Information page at the following URL: <https://www.altera.com/support/support-resources/download/drivers/dri-index.html>.

Intel FPGA SDK for OpenCL

Download the Intel FPGA SDK for OpenCL at the following URL: <https://www.altera.com/products/design-software/embedded-software-developers/opencl/downloads.html>

To initialize the Intel Arria 10 GX FPGA Development Kit for use with OpenCL:

1. Lower the JTAG clock speed to 6 MHz using the following command:

```
jtagconfig --setparam 1 JtagClock 6M
```

You can confirm the clock speed with the following command:

```
jtagconfig --getparam 1 JtagClock
```

2. Uncompress the following file to a temporary location:

```
INTELFPGAOCSDKROOT/board/a10_ref/bringup/a10_ref_initialization.tgz
```

Where *INTELFPGAOCSDKROOT* in the installation path for the Intel FPGA SDK for OpenCL.

Ensure that you have the following files in your temporary location. You need these files to complete the steps that follow.



- max5_150.pof
- top.sof
- boardtest.aocx

3. Update the MAX V CPLD system controller with the max5_150.pof file as follows:
 - a. Ensure that cable number 1 is the cable connected to the Intel Arria 10 GX FPGA Development Kit with the following command:

```
quartus_pgm -l
```

The command output should resemble the following example output:

```
Info: Command: quartus_pgm -l
1) USB-BlasterII [2-1.3]
Info: Quartus Prime Programmer was successful. 0 errors, 0 warnings
```

- a. Run the jtagconfig command as follows to ensure that your Intel FPGA Download Cable driver is ready:

```
bash-4.1$ jtagconfig

1) USB-BlasterII [2-1.1]
   02E060DD 10AT115N(2E2|3E2|4E2)/..
   020A40DD 5M2210Z/EPM2210
```

- b. Run the following command to update the MAX V CPLD system controller:

```
quartus_pgm -c 1 -m JTAG -o "p:max5_150.pof@2"
```

4. Program the FPGA on your Intel Arria 10 GX FPGA Development Kit with the top.sof file by running the following command:

```
quartus_pgm -c 1 -m JTAG -o "p:top.sof"
```

5. Perform a soft reboot (sometimes called a warm reboot) of your host system. On Linux systems, use the /sbin/reboot command to perform a soft reboot.

After you program the FPGA and perform a soft reboot, the host system should recognize the Intel Arria 10 GX FPGA Development Kit PCIe card. Your system must recognize the card before you load the Intel FPGA SDK for OpenCL driver.

After preparing your Intel Arria 10 GX FPGA Development Kit for the compiler, install the OpenCL runtime driver, program the flash memory, and run a diagnostic test to confirm that board initialization was successful.



Installing the OpenCL Runtime Driver

After your Intel Arria 10 GX FPGA Development Kit board is initialized for use with the Intel FPGA SDK for OpenCL Offline Compiler, install the OpenCL runtime driver and run a diagnostic.

To install the OpenCL runtime driver and run a diagnostic test:

1. Ensure that the `AOCL_BOARD_PACKAGE_ROOT` environment variable points to where you have the `a10_ref` board support package (BSP).
2. On Linux host systems, set the `LD_LIBRARY_PATH` environment variable as follows:

```
export LD_LIBRARY_PATH=$LD_LIBRARY_PATH:$INTELFPGAOCCLSDKROOT/host/linux64/lib:$AOCL_BOARD_PACKAGE_ROOT/linux64/lib
```

3. Install the OpenCL runtime driver by running the following command with root or administrator privileges:

```
aocl install
```

The command should produce output like the following example output:

```
aocl install: Running install from /tools/aclboardpkg/altera_a10pciedk/16.0/linux64/libexec
Using kernel source files from /lib/modules/2.6.32-358.el6.x86_64/build
Building driver for BSP with name a10_ref
make: Entering directory `/usr/src/kernels/2.6.32-358.el6.x86_64'
CC [M] /tmp/openccl_driver_x6GjWS/aclpci_queue.o
CC [M] /tmp/openccl_driver_x6GjWS/aclpci.o
CC [M] /tmp/openccl_driver_x6GjWS/aclpci_fileio.o
CC [M] /tmp/openccl_driver_x6GjWS/aclpci_dma.o
CC [M] /tmp/openccl_driver_x6GjWS/aclpci_pr.o
CC [M] /tmp/openccl_driver_x6GjWS/aclpci_cmd.o
LD [M] /tmp/openccl_driver_x6GjWS/aclpci_a10_ref_drv.o
Building modules, stage 2.
MODPOST 1 modules
CC /tmp/openccl_driver_x6GjWS/aclpci_a10_ref_drv.mod.o
LD [M] /tmp/openccl_driver_x6GjWS/aclpci_a10_ref_drv.ko.unsigned
NO SIGN [M] /tmp/openccl_driver_x6GjWS/aclpci_a10_ref_drv.ko
make: Leaving directory `/usr/src/kernels/2.6.32-358.el6.x86_64'
```

Programming the Flash Memory on the Intel Arria 10 GX FPGA Development Kit

After you initialize the Intel Arria 10 GX FPGA Development Kit and install the OpenCL runtime driver, program the flash memory on the board and run a diagnostic test.

1. Program the flash memory on the board as follows:
 - a. Set the `AOCL_BOARD_PACKAGE_ROOT` environment variable to point the folder that contains your Intel Arria 10 reference BSP folder:

```
INTELFPGAOCCLSDKROOT/board/a10_ref
```

Where `INTELFPGAOCCLSDKROOT` is the installation path for the Intel FPGA SDK for OpenCL.



- b. Run the following command to program the flash memory. This command does not use PCIe. It requires only JTAG.

```
aocl flash ac10 boardtest.aocx
```

2. Perform a hard reboot (sometimes called a cold reboot) of your host system. That is, power your host system down, then turn the host system power back on.
3. Confirm that the initialization completed successfully by running the following command:

```
aocl diagnose
```

The command should produce output like the following example output:

```
aocl diagnose: Running diagnose from /tools/aclboardpkg/altera_a10pciedk/16.0/linux64/libexec

----- ac10 -----
Vendor: Intel Corporation

Phys Dev Name Status Information
acla10_ref0    Passed Arria 10 Reference Platform
                PCIe dev_id = 2494, bus:slot.func = 04:00.00, Gen3
x8
                FPGA temperature = 38.8 degrees C.

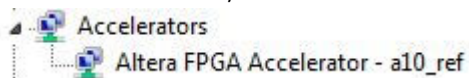
DIAGNOSTIC_PASSED
```

At this point, you can see the Intel Arria 10 GX FPGA Development Kit board as a PCIe device on your system.

On Linux host systems, the `/sbin/lspci | grep Altera` command should return output similar to the following example output:

```
-baseh-4.1$ lspci | grep Altera
03:00.0 Class 1200: Altera Corporation Device 2494 (rev 01)
```

On Windows host systems, the Windows device manager should show the device under **Accelerators**, similar to the following example:



Your Intel Arria 10 GX FPGA Development Kit is now ready to use with the Intel FPGA SDK for OpenCL Offline Compiler. If you had any errors when initializing your board, review the [Troubleshooting](#) on page 13 section.

Troubleshooting

If you encounter errors when you configure the Intel Arria 10 GX FPGA Development Kit for the Intel FPGA SDK for OpenCL, review the sections that follow for possible solutions.

The Quartus Programmer might display errors when your run `aocl flash` or `aocl program`

Your board might fail with the following error:

```
Info: Command: quartus_pgm -c 1 flash.cdf
Info (213045): Using programming cable "USB-BlasterII [2-1.1]"
Info (209060): Started Programmer operation at Wed Mar 22 13:56:27
```




```
2017      Error (209025): Can't recognize silicon ID for device 2
          Error (209025): Can't recognize silicon ID for device 2
          Error (209012): Operation failed
          Info (209061): Ended Programmer operation at Wed Mar 22 13:56:28
2017
```

This error indicates that the MAX V CPLD system controller not programmed with the correct image.

Solution

Use the Quartus Programmer to update the MAX V configuration with the `max5_150.pof` file for Intel Arria 10 GX FPGA Development Kit boards. If the error persists, program the FPGA with the `top.sof` file and program the flash memory with the `aocl flash` command again.

Quartus Programmer fails while programming either the FPGA or flash memory

If you receive one of the following errors while programming the FPGA or the flash memory, the JTAG clock frequency might be set higher than 6 MHz:

- Error (209014): CONF_DONE pin failed to go high in device 1
- Error (209012): Operation failed

Solution

Lower the JTAG clock frequency to 6 MHz with the following command:

```
jtagconfig --setparam 1 JtagClock 6M
```

You can confirm the JTAG clock frequency with the following command:

```
jtagconfig --getparam 1 JtagClock
```

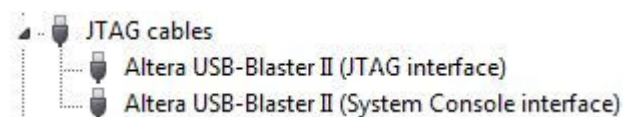
For Microsoft Windows users, Intel FPGA Download Cable driver might not be installed on your host

On Windows host systems, the Intel FPGA Download Cable (formerly USB-Blaster) needs a driver installed for the cable to function properly.

Solution

Download the Intel FPGA Download Cable driver from the Intel FPGA Cable and Adapter Drivers Information page at the following URL: <https://www.altera.com/support/support-resources/download/drivers/dri-index.html>.

After you install the drivers, you should see the cable listed in Windows device manager as follows:





PCIe read/write speed is slower than expected

If you find that your PCIe read/write speed is slower than you expect, then your board might not be plugged into the correct PCIe slot.

Solution

Verify that your Intel Arria 10 GX FPGA Development Kit is plugged into the PCIe Gen3 x8 slot on your host system. See ["Configuring and installing the Intel Arria 10 GX FPGA Development Kit board"](#) on page 3 "to see what the correct PCIe slot looks like.

Memory module is not plugged in or a loose connection on the board

If the memory module is not plugged in or if there is a loose connection on the board, you might see errors similar to the following example:

```
aocl diagnose: Running diagnose from
aocl diagnose: failed 32 times. First error below:
Vendor: Intel Corporation
MMD INFO: [acla10_ref0] uniphy(s) did not calibrate. Expected 0 but read 2
MMD INFO: If there are more failures than Uniphy controllers connected,
MMD INFO: ensure the uniphy_status core is correctly parameterized.
```

Solution

Confirm that you have connected the memory board, the power cable, and USB cable correctly as shown in ["Configuring and installing the Intel Arria 10 GX FPGA Development Kit board"](#) on page 3". If you have confirmed your connections and continue to get this error, the memory board might not be seated correctly in the HiLo connector.

Document Revision History

Table 1. Document Revision History of Configuring the Intel Arria 10 GX FPGA Development Kit for the Intel FPGA SDK for OpenCL

Date	Version	Changes
May 2018	2018.05.04	<ul style="list-style-type: none"> Added the topic Programming the Flash Memory on the Intel Arria 10 GX FPGA Development Kit on page 12 In Initializing the Intel Arria 10 GX FPGA Development Kit for use with OpenCL on page 10, moved steps 6 and 7 to Programming the Flash Memory on the Intel Arria 10 GX FPGA Development Kit on page 12. In Installing the OpenCL Runtime Driver on page 12, moved step 4 to Programming the Flash Memory on the Intel Arria 10 GX FPGA Development Kit on page 12.
November 2017	2017.11.16	<ul style="list-style-type: none"> In Initializing the Intel Arria 10 GX FPGA Development Kit for use with OpenCL on page 10, updated step 6. In Installing the OpenCL Runtime Driver on page 12, updated step 2 on page 12. In Initializing the Intel Arria 10 GX FPGA Development Kit for use with OpenCL on page 10, rebranded the environment variable <code>ALTERAOCLSDKROOT</code> to <code>INTELFPGAOCSDKROOT</code>.
May 2017	-	Initial release.