Mes actualités sur FPGA & OpenCL

09.04.2019

Bogdan Vulpescu
LPC

Séminaires, soutenances

The Fourth Paradigm in Astronomy: from ESA/Gaia and beyond

par Alberto KRONE-MARTINS (Universidade de Lisboa, CENTRA/SIM)

vendredi 5 avr. 2019 à 14:30 → 16:30 Europe/Paris

Description

"Astronomy (...) it was she who made us a soul capable of comprehending Nature".

Whether or not we agree with Henri Poincaré's central view of Astronomy, this Science has historically been deeply connected to, and in many cases motivated, the amplification of human sensitive and cognitive capabilities.

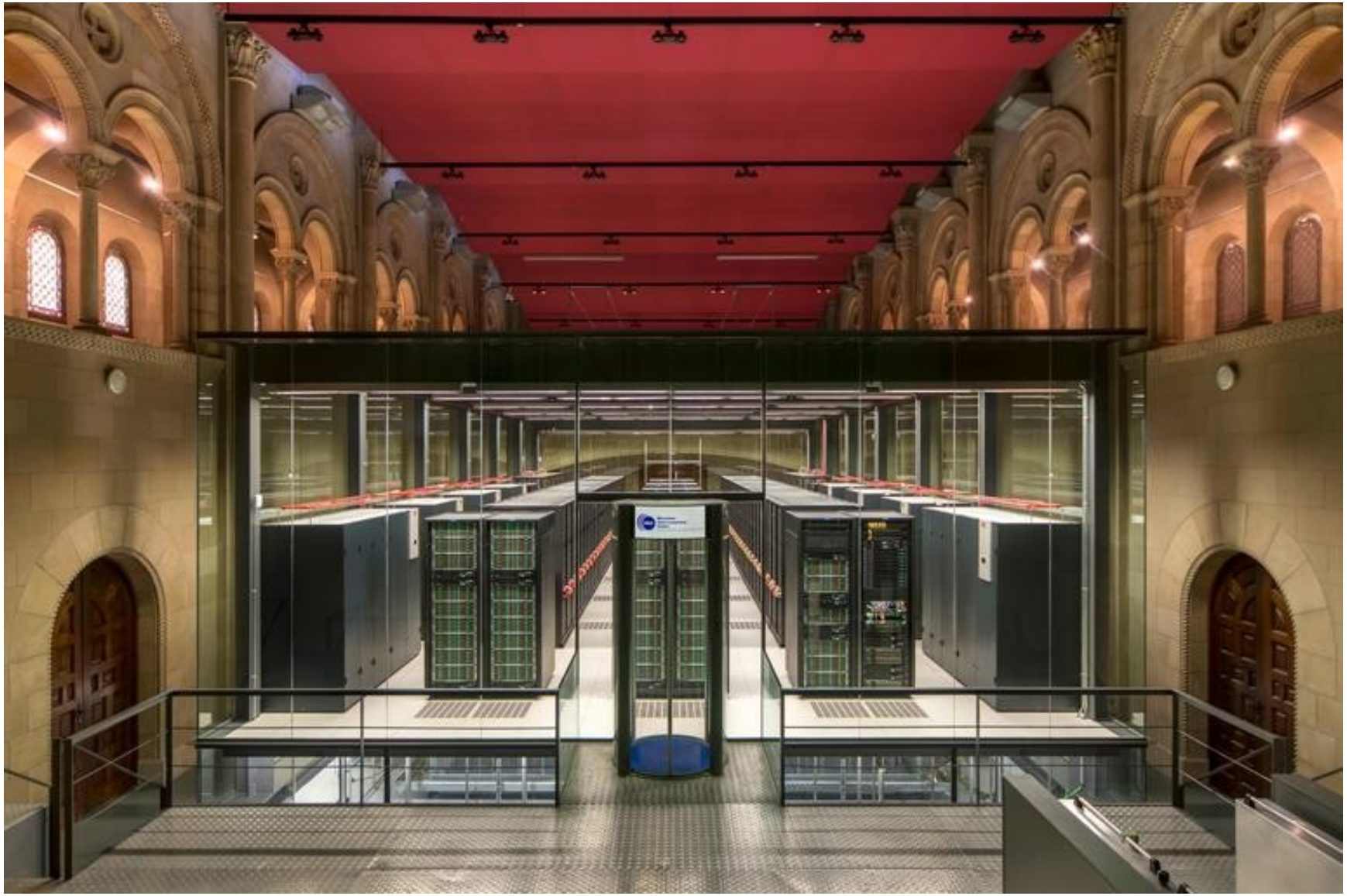
During this talk I would like to openly discuss the "fourth paradigm of Science" concept in Astronomy. This is a thought pattern that evolves the relation between Science and Informatics from the simple notion of "using a tool" towards a deeper degree of inter-dependency. To do so, I will briefly present some examples of my scientific research that are entrenched in this concept, as galaxy morphology inference from ESA/Gaia data, the supervised discovery of new strong gravitational lenses, the semi-supervised discovery of new stellar clusters and the unsupervised construction of galaxy catalogues.

Finally, I would like to profit from the talk to discuss if it will still be possible to do forefront discoveries in the era of large particle colliders, cosmic ray observatories and astronomical surveys as LSST, without some type of machine-assisted and continuously collaborative thinking.

The talk will be accessible to non-astronomers.

Alberto Krone-Martins is a researcher at the Universidade de Lisboa. He crossed the Universidade de São Paulo (Brazil), Université de Bordeaux (France) and Caltech (USA), mostly working at the interface of Astronomy, Space Astrometry, Informatics and Statistics. Besides industrial responsibilities related to satellite and spacecraft navigation, he is currently
responsible for a number of scientific work-packages in the ESA/Gaia DPAC (Data Processing Consortium) and also co-chairs the Cosmostatistics Initiative.

Mare Nostrum 4 - Barcelona Supercomputing Center



Home
Join Us
Fellowships
Scholarships
Job Opportunities
Excellence Career Opportunities
HR Initiatives & Badges
Gender and Diversity Equality Plan

FPGA Designer

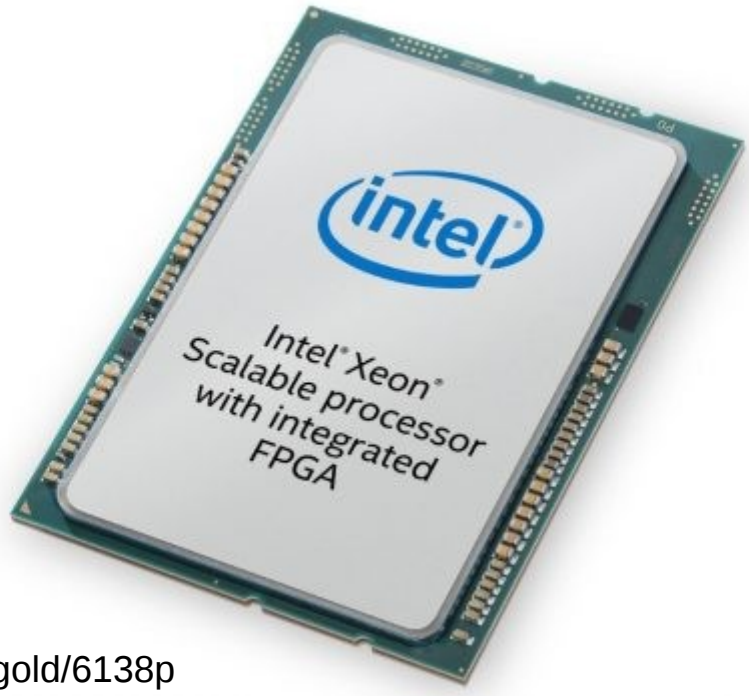
Job Reference	Position	Closing Date
22_CS_MEBHPC_R2	FPGA Designer	Monday, 08 April, 2019

Reference: 22_CS_MEBHPC_R2
Job title: FPGA Designer

About BSC

The Barcelona Supercomputing Center - Centro Nacional de Supercomputación (BSC-CNS) is the leading supercomputing center in Spain. It houses MareNostrum, one of the most powerful supercomputers in Europe, and is a hosting member of the PRACE European distributed supercomputing infrastructure. The mission of BSC is to research, develop and manage information technologies in order to facilitate scientific progress. BSC combines HPC service provision and R&D into both computer and computational science (life, earth and engineering sciences) under one roof, and currently has over 500 staff from 44 countries.

"May 2018: Available now for "select" customers, Intel's Xeon Scalable Gold 6138P processor with integrated Intel Arria 10 GX 1150 FPGAs marks the first production CPU with a coherently interfaced FPGA, according to industry observers."



https://en.wikichip.org/wiki/intel/xeon_gold/6138p

Intel Xeon Gold: Adding an FPGA		
AnandTech	Xeon Gold 6138	Xeon Gold 6138P with Arria 10 FPGA
Socket	Socket P LGA 3647	Socket P LGA 3647
Cores / Threads	20 / 40	20 / 40 ?
Base Frequency	2000 MHz	2000 MHz ?
Turbo Frequency	3700 MHz	3700 MHz ?
PCIe Lanes	48	32
DRAM	Six Channels DDR4-2666	Six Channels DDR4-2666
On-Package FPGA	-	Arria 10 GX 1150
Logic Elements	-	1150K (1.15m)
Embedded Memory	-	53 Mb
UPI Links	Three	Two
TDP	125 W	125 W CPU 60 - 70 W FPGA 195 W Total ?
Price	$2612	Arm, Leg

Rapid Discrete Fourier Transformation with OpenCL kernel

```
__attribute__((reqd_work_group_size(2048,1,1)))
__kernel void rdft(__global float* restrict x,
                   __global float* restrict lutrsin,
                   __global float* restrict lutrcos) {

  int N = (get_global_size(0)-1)*2;
  int num_vectors = N;

  float X_real = 0.0f;
  float X_imag = 0.0f;

  float lutcos, lutsin;

  int ilut, n = get_global_id(0);

  for(int i=0; i<num_vectors; i++) {

    if (i == 0) {
      ilut = 0;
    } else if (i < n) {
      ilut = n*(n-1)/2+n+i;
    } else {
      ilut = i*(i-1)/2+i+n;
    }

    lutcos = lutrcos[ilut];
    lutsin = lutrsin[ilut];

    X_real += x[i] * lutcos;
    X_imag -= x[i] * lutsin;
  }
```

(cont.)

```
  barrier(CLK_GLOBAL_MEM_FENCE);
  if(get_global_id(0) == 0) {
    x[0] = X_real;
  } else if(get_global_id(0) ==
            get_global_size(0)-1) {
    x[1] = X_real;
  } else {
    x[get_global_id(0) * 2] = X_real;
    x[get_global_id(0) * 2 + 1] = X_imag;
  }
}
```

FPGA resources occupancy report (Quartus Prime Standard 17.0)

`lut` = look-up-tables for sin and cos instead of built-in functions
`scal` = scalar (float) variables instead of vector (float4)

Kernel	ALUTs	FFs	RAMs	DSPs	
rdft_c5gt_blank_	52722	46925	366	0	
	23	10	30	0	[%]
Board interface + rdft	51152	45420	366	0	
	1570	1505	0	0	
	1	0	0	0	[%]

Kernel	ALUTs	FFs	RAMs	DSPs	
rdft_c5gt_					
	93301	109084	463	49	
	41	24	38	14	[%]
rdft_scal_c5gt_	72553	77945	454	16	
	32	17	37	5	[%]
rdft_lut_c5gt_	84171	97057	550	18	
	37	21	45	5	[%]
rdft_lut_scal_c5gt_	70690	73328	467	6	
	31	16	38	2	[%]
Board interface	51152	45420	366	0	
+					
Global interconnect	9588	10682	0	0	
+					
rdft	9950	17226	101	6	
	4	4	8	2	[%]