Development of CMOS Pixel Sensors
- Design & Characterisation -

Gilles Claus & Christine Hu Guo

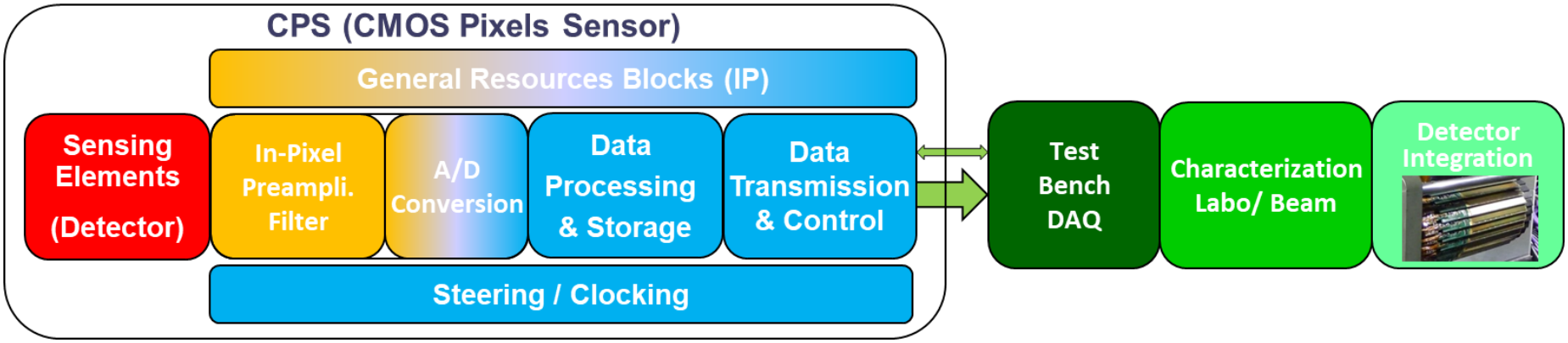
MicPHC

(The Microelectronics group at IPHC)

Outline

- Introduction, MicPHC technical organization
- CPS design & characterization
- R&D activities for the next 3-5 years
- Conclusions

CMOS Pixel Sensors Development



- CPS is an integrated measurement system (SoC)
  - Needs a **wide range of skills** in Si detector, microelectronics (analogue, digital), electronics (analogue, digital), data acquisition, mechanics, …
- The group MicPHC is organised by expertise in order to master the entire chain: **Definition-Design-Validation**-Integration of CPS
  - Physicists involved (PICSEL)
- Continuous R&D on sensor architectures and design techniques benefiting from the progress of semiconductor processes
- **Design to Reuse** (with adjustments) creates synergy among projects
  - Ability to handle multiple projects in parallel

Synergy Among Projects

Ultimate objective: ILC, with staged performances

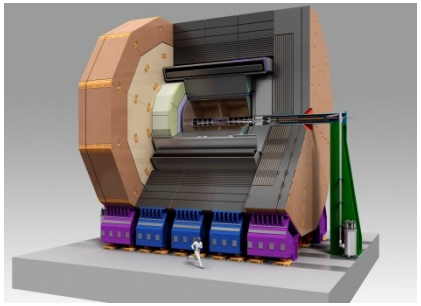
CPS applied to other experiments with intermediate requirements

EUDET 2006/2010

Beam Telescope

ILC ~2030

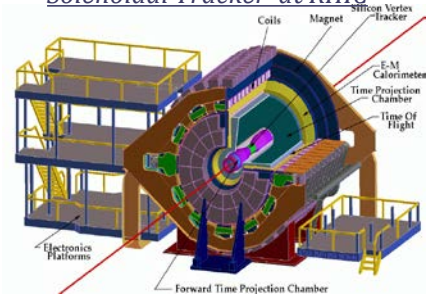
International Linear Collider



- **Tracking of Charged Particles**
  - Subatomic physics
  - Beam instrumentation
  - Hadron therapy
- **Imaging**
  - B-rays, low energy e^-
  - X-rays
  - Dosimetry
  - Hybrid photo-detector
  - Bio-inspired vision

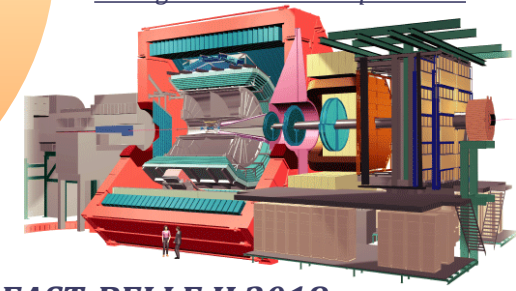
STAR 2013

Solenoidal Tracker at RHIC



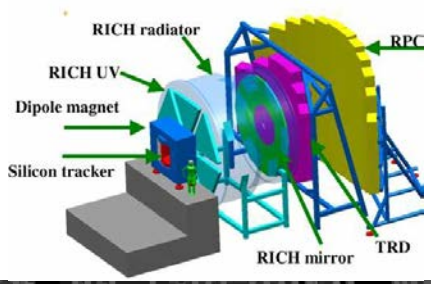
ALICE 2018

A Large Ion Collider Experiment



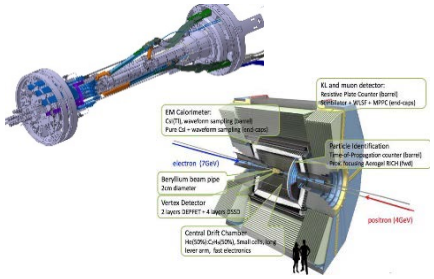
CBM >2020

Compressed Baryonic Matter

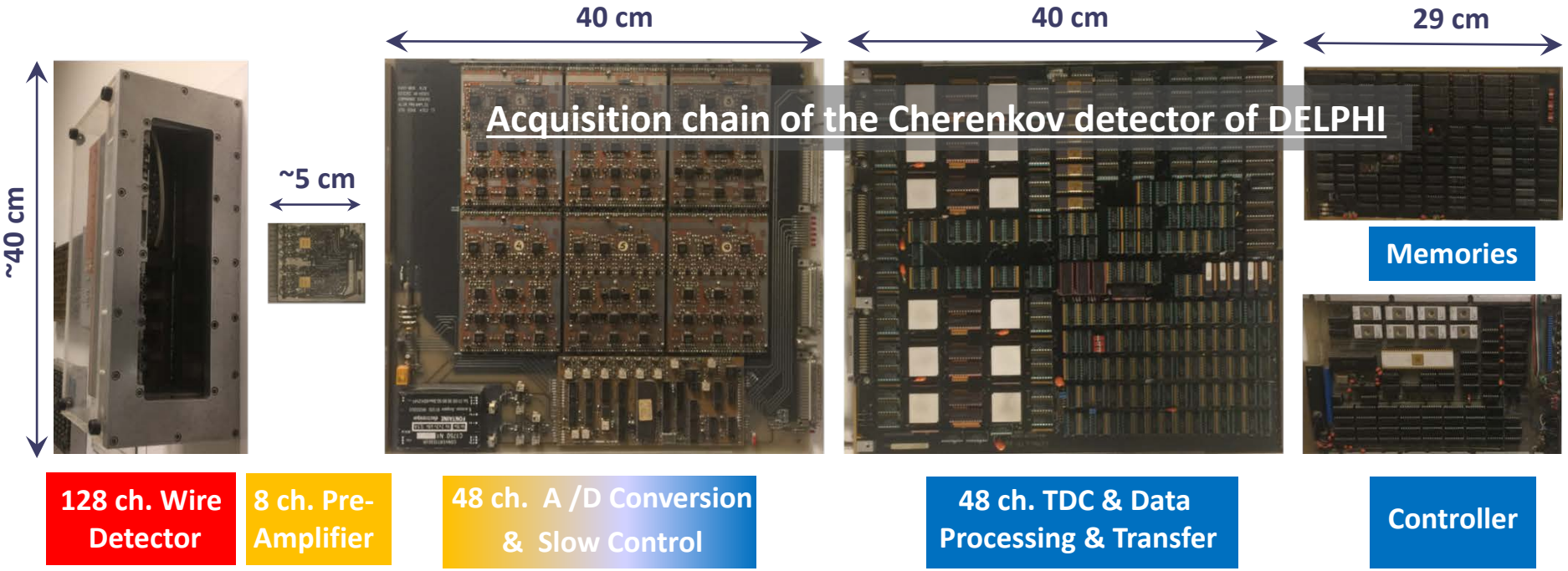


BEAST-BELLE II 2018

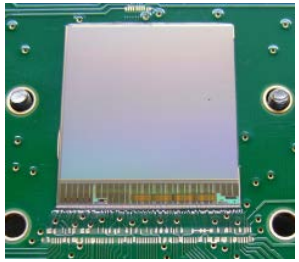
Beam Exorcism for A STable BELLE Experiment



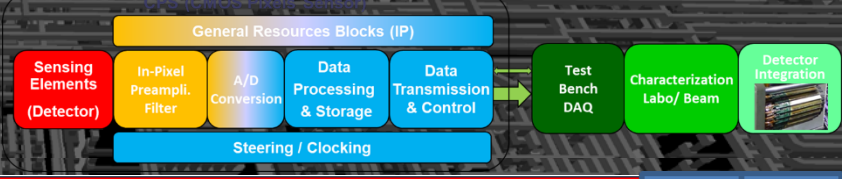
Earlier Measurement System (DELPHI 1981-1989)



- **1 detector group** + **2 technical groups** (A, D) were involved in the project
- Now, with CPS (MIMOSA28 ~1 M channels), the whole measurement system is integrated on the same substrate
  - Experts must interact strongly
  - Modeling/simulation prevail at each step of the development
    - Defective parts cannot be repaired



Work Breakdown & Team



Coordination technique

Définition & Etude des a s

Support des outils CAO et Systèmes

Eléments de détection → Modélisation Semiconducteur

ectronique du pixel — Simulation / Layout / Véri n

riques de base (IP) — ulation / Layout / Vér n

Ensembles numériques — délisation/Banc de test HDL

nsembles numériques — Synthèse/Routage/STA/CTS/

plantation /Intégration → Réalisation archi. / P&S coupl s

Vérification / Production → Règles de fabrication

Composants PCB → Y compris Capteurs CMOS

actérisation — Conception Bancs de test / DAQ

gration des bancs — Cartes, Monitoring

Caractérisation des IP — Les blocs de base

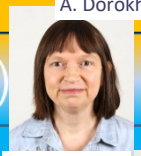
Caractérisation des capteurs — Labo-Faisceaux-Irradiation

Test de production → Construction du détecteur


C. Hu-Guo - IRHC


A. Dorokhov - IR1


M. Kachel - IR2


I. Valin - IR1


H. Pham - IR2


Y. Hu – Pr
µE Ph.D supervision


C. Colledani- IRHC


A. Himmi - IR1


G. Dozière- IR1


G. Bertolone - IE2


F. Morel - IR2


C. Illinger - IEHC


G. Claus - IR2


M. Specht - AI

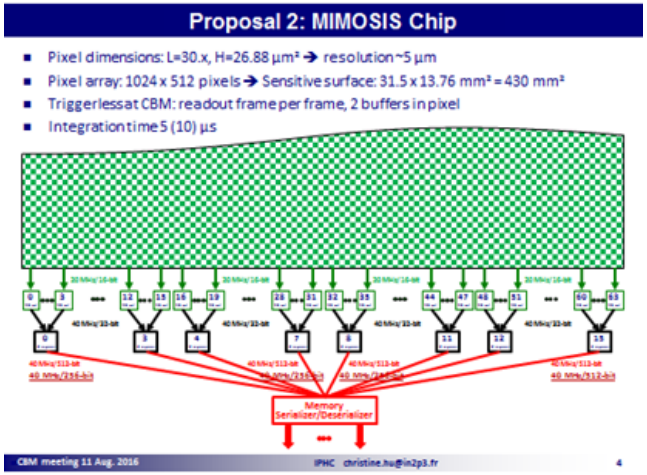

K. Jaaskelainen - IEHC


M. Goffe - IE2

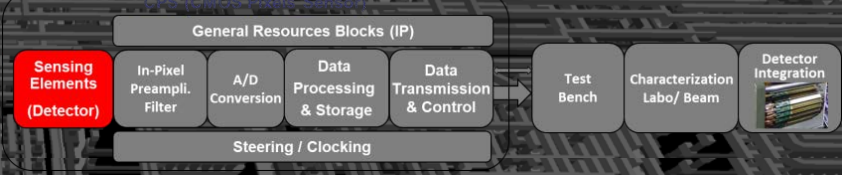

M. Szelezniak - IR2

Project Definition & Technical Coordination

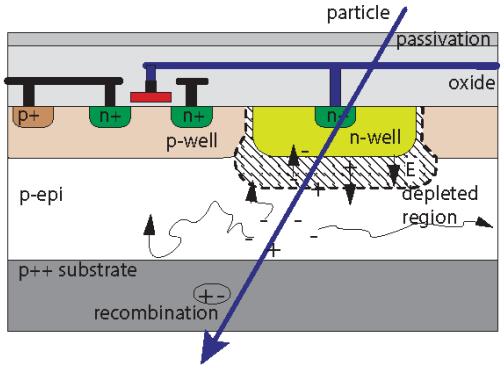
- Ensure connection between physics and CPS design
  - Transcription of physical constraints into electronic specifications
- Study / Propose of CPS architectures dedicated to the projects
  - Identifying the crucial points
  - Reusing, if feasible, the basic building blocks
  - Allocating of the necessary human resource
- Develop technical solutions in line with the technology progress
- Interact with foundries to maximize the process potential
- Interact within collaborations

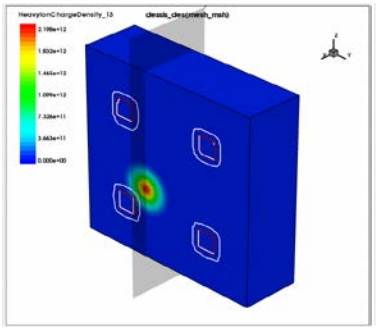


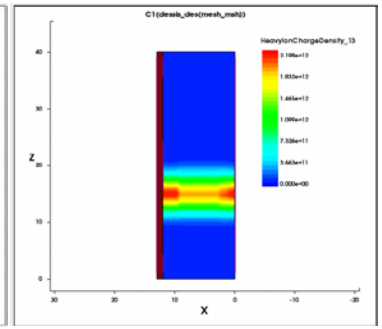
Sensing Elements

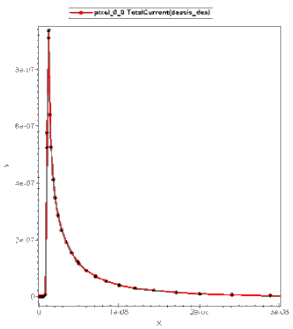


- **Objective**: according to PHY requirements: σ_{sp}, t, ☢, … dealing with µE specs: noise, P, …
- The key point is to choose the adequate process (doping, thickness, ρ, …)

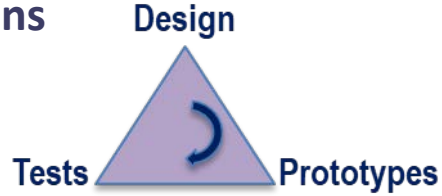




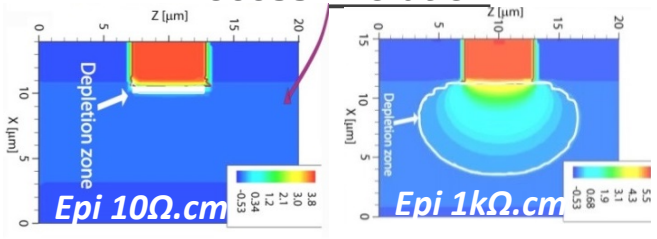




- **Design progresses by iterations**

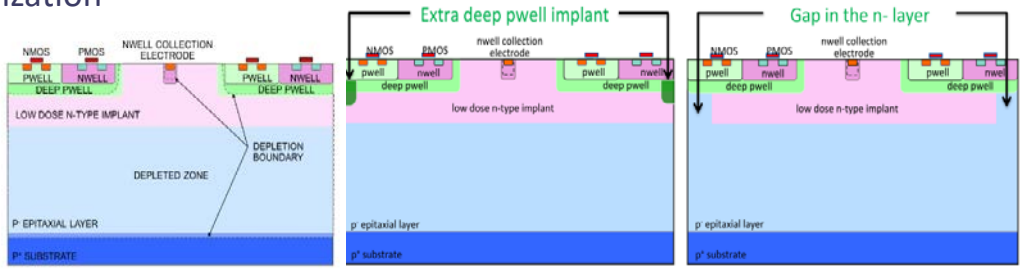


Process Evolution

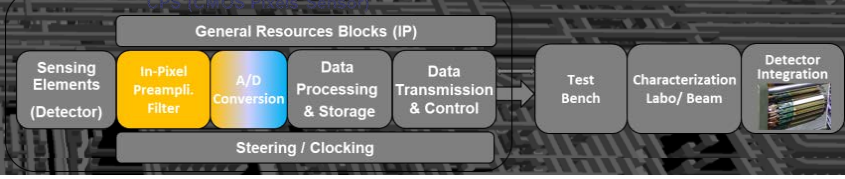


- TCAD simulation & optimization
  - **Depends on process parameters** (Access?)
    - Relation with foundry → process optimization
  - Radiation tolerance
    - Design validated by prototyping ($/€!)
    - → N diode topologies for a project

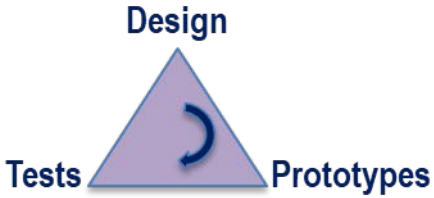
Process Optimisation (CERN-Foundry)

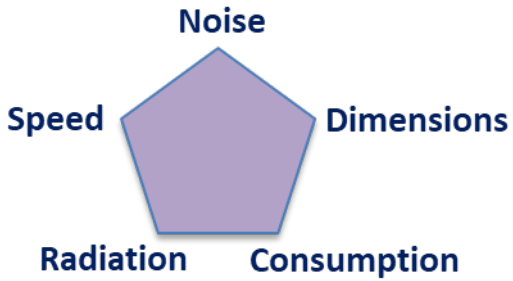


In-Pixel Front-End Electronics



- **Objective**: design a low noise & very low power FEE (Front-End Electronics)
  - Signal ~100 e^- due to the EPI layer thickness → ultra low noise
    - 1/f, thermal, shot, RTS (no modeling), …
  - High density, ~200 k ch/cm² requires → low power
    - Tradeoff Speed & Power consumption
    - Low power → MOS in weak inversion (model?)
  - Design robustness : pixel-to-pixel, chip-to-chip & wafer-to-wafer variations

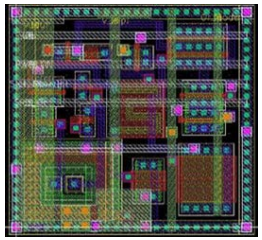




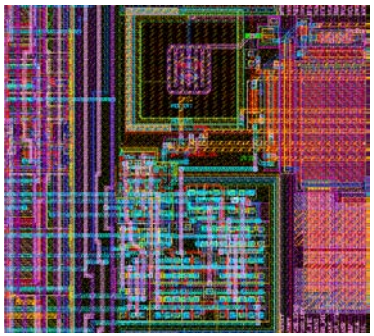
- **Access to foundry & specific process** can provoke a (r)evolution in the FEE design

  0.35 µm **Twin-wells** (NMOS) → 0.18 µm **Quadruple-wells** (CMOS) = more functionalities

Pre-amplifier/CDS



MIMOSA28

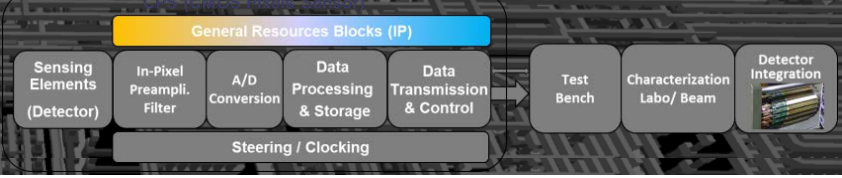


MIMOSIS

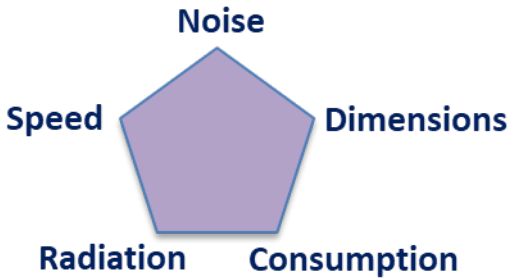
Integration of a FEE in typ. 20x20 µm²

- Pre-amplifier/Shaper
- A/D conversion
- In-pixel memories
- Data driven readout

Functional Blocks (IP)



- **Objective**: SoC, design functional blocks (IP), according to the spec, needed for a CPS. They have the **same constraints** as the in-pixel FEE



- These **IP blocks must** often be considered as **complete µE projects**
  - Ex. ADC: Collaboration LPSC, LPCC, IRFU, IPHC → 4 Ph.D theses

➔ **Reusable IP** for CPS → Synergy in projects and collaborations
  - DeSIs and DRHIM also benefited from these IPs for their circuits

Analog and mixed IP:

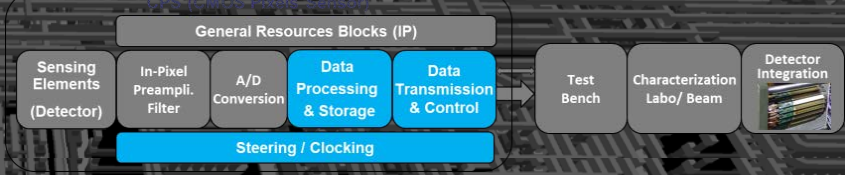
- ADC, TDC, bias DAC, LDO regulator, SRAM, PLL, DLL, LVDS Rx et Tx, Temp. sensor, Band Gap, …

➔ Analog IP modelization for Digital Design Flow compatibility → Another evolution in the knowhow

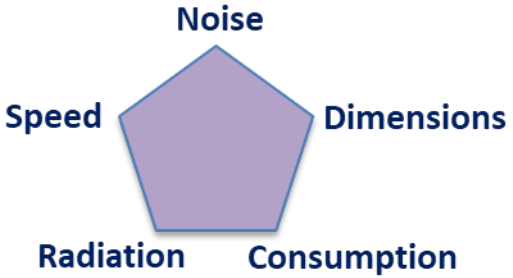
Digital IP:

- SPI, I2C, JTAG, Serialiser/deserialiser, 8B/10B, …

All Digital Circuits

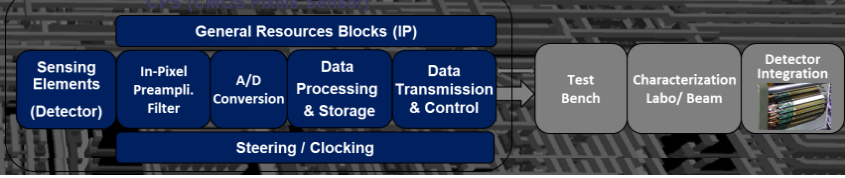


- **Objective**: readout strategy, embedded data processing & compressing, transmission
  - Steering & control logic, memories and digital IP blocks
  - Design technics + Constraints:
    - Consumption (clock & power gating, asynchronous RO)
    - cross-talk
    - surface (insensitive area)
    - radiation tolerance (SEE) & speed
    - **Signals / clocks distributions over long lengths** (3 cm)

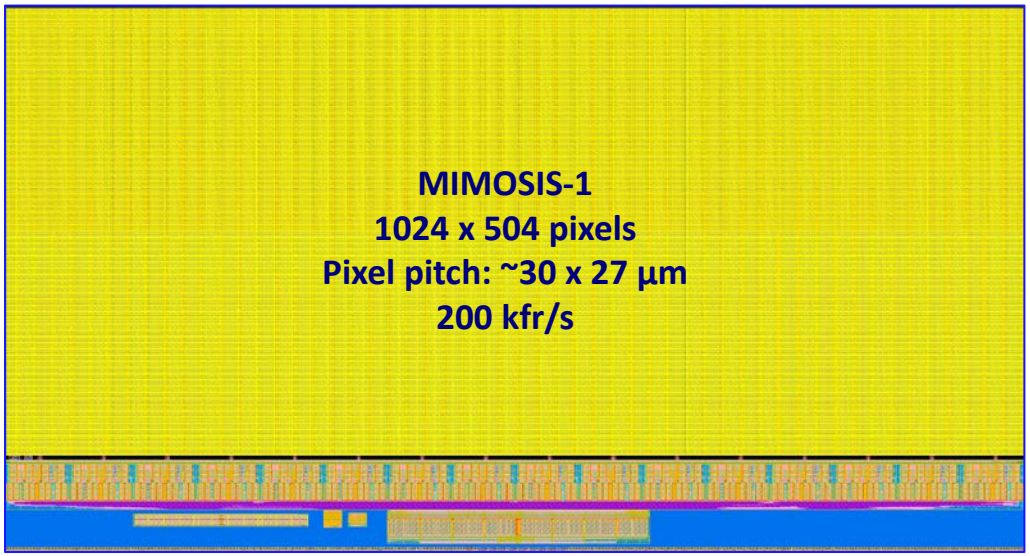


- **Pushed by the requirements of the experiments**
  - **Strong growth in complexity**
    - Steering and 'SUZE' logics→ data driven readout + high data flow management
    - For CBM (MIMOSIS) = 20 Gbps in internal data flow (~10xALPIDE)
      - New digital design on data compression, storage and transmission
      - **Collaborations: IKF**

CPS Integration



- **CPS == SoC** → need an engineer expert dedicated to the integration at the system level
- Design for Test (DfT) → the integrated testability is defined with the test team



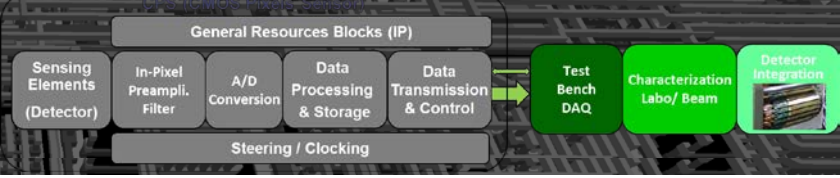
- **Facing the evolution** of mixed circuits: from (A/d) to (a/D)
  - ↳ Imposes an evolution of methodologies, from AoT to DoT → (new skill!)
    - **Always looking for additional digital designers!**
    - Few microelectronics designers at IN2P3 master it

Design Team Summary

Tasks	Definition & Study Coordination T	Sensing Elements	Front End Electronics	Functional Blocks (IP)	All Digital Circuits	CPS Integration	IT, PCB CAD Support	Activities off-project
FTE (total 11/year)	0.8/year	0.6/year	1.8/year	1.8/year	2.8/year	1/year	0.4/year	1.8/year

- Activities off-project:
  - IN2P3 expert site for Cadence tools, for sharing IP blocks — 0.1 FTE / year
  - Expertise & consulting (University - ICube, Mind, Collaborations, Juries) — 0.1 FTE / year
  - IN2P3 µE/CAD chargé de mission (C. Colledani) — 0.6 FTE / year
  - IN2P3 PCB library (0.3 FTE) and IPHC PCB support (0.4 FTE) (C. Illinger) — 0.7 FTE / year
  - Other: conferences, training courses, courses given — 0.2 FTE / year
- **Training place** for students in **µE** & physics instrumentation
  - PhD students work on **upstream R & D**
    - They are technically supervised by our Ph.D engineers
    - 22 since 2005 including 3 Imabio and 1 Ramses
      - 2 ongoing
  - 7 masters µE + 1 engineering student µE + 2 BAC pro PCB since 5 years

Tests Team Missions



- CPS, IP blocks Test & Characterization
  - Provide Test benches
  - Training / Test benches for CPS designers, Physicists, PhD students, Post Doc
  - Contribute to Test & Characterization activities


G. Claus - IR2


K. Jaaskelainen - IEHC


M. Specht - AI


M. Goffe - IE2


M. Szelezniak - IR2

- Contribute to CPS technology deployment
  - Demonstrators & Instruments for final applications
    - EUDET Telescope - 2010 DESY, CERN
    - FIRST - 2012 Heidelberg
    - CYRCé Hadron Therapy - 2016 IPHC

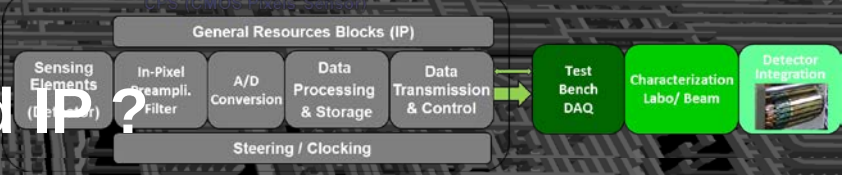

EUDET Beam Telescope

  - Construction of HEP detectors
    - STAR PXL detector - 2013 STAR USA
    - PLUME in BEAST - 2018 KEK Japon
    - CBM MVD detector - 2020 GSI Germany


STAR detector 2013


PLUME detectors in BEAST - 2018

Test & Characterization ➔ CPS and IP ?



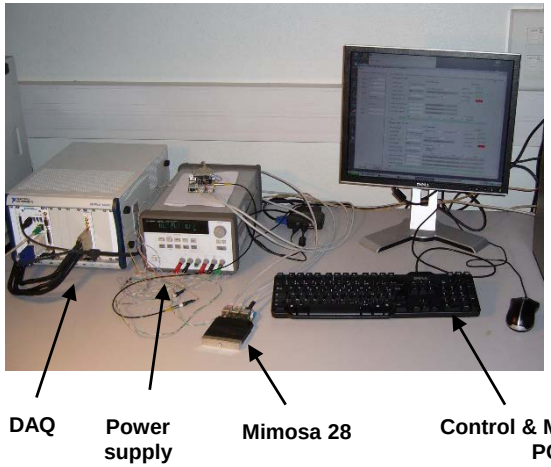
- Goal of the CPS in HEP ➔ Pixels matrix for particles position detection

  - CPS Input
    - It must be particles
    - Hardly emulated by electric signal

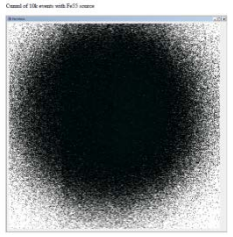
  - CPS characterization skills
    - Pixels ➔ Physics, Electronics
    - Signal processing ➔ Electronics

Mimosa 28
4 cm² - 10^6 pixels
5400 fr/s

Mimosa 28
mounted on a PCB



Mimosa 28 Test bench



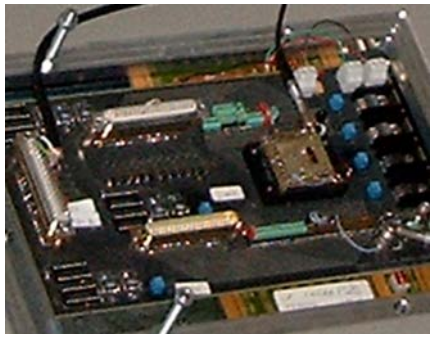
Fe55 X-Ray source picture taken with Mimosa 26

- What is an IP, IP block ➔ Electronic block (Amplifier, DAC, ADC, Processing logic)

  - IP Input & Output
    - Electric signals

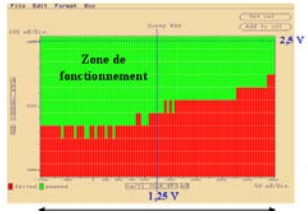
  - IP Characterization skill
    - Electronics

SLVS Bufer



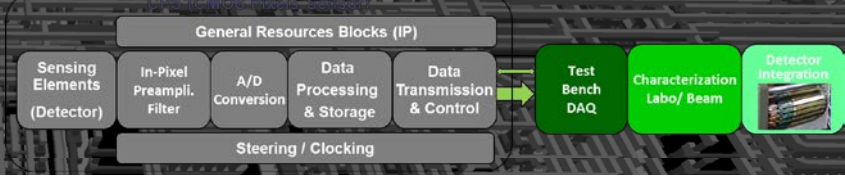
Test bench

Test results

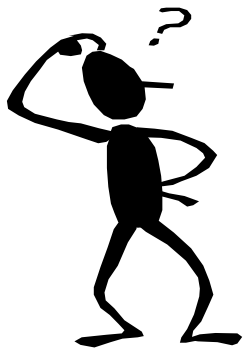


Buffer operation vs
-Power supply voltage
-Input signal level

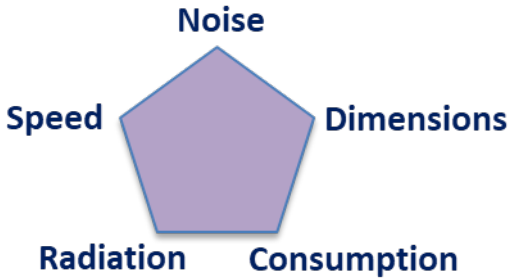
Test & Characterization → Why ?



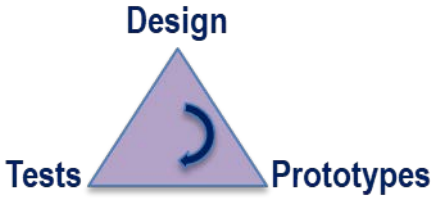
- Test & Characterization
  - Test = Functional test BEFORE performance measurement
    - Check for CPS design errors (Thanks to simulation risk is low but never null)
    - Check for CPS foundry process problems & Measure production yield
    - But … our test activities are not production test for final CPS
  - Characterization = Performance measurement



- Characterization is crucial
  - Characterization is more than performance assessment

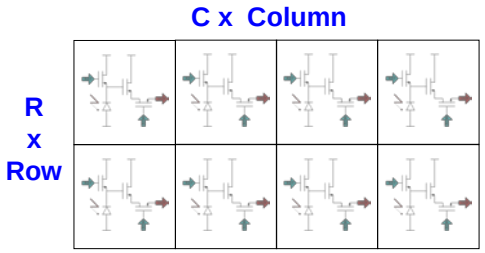


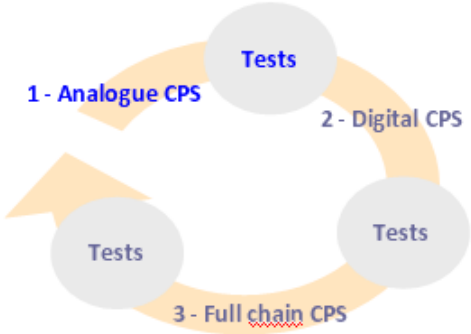
  - Characterization is integrated in the CPS R&D cycle
    - It is a feedback which guides the R&D program.
    - It starts with tests at laboratory and ends in Beam Tests
      CPS working conditions ~ final application



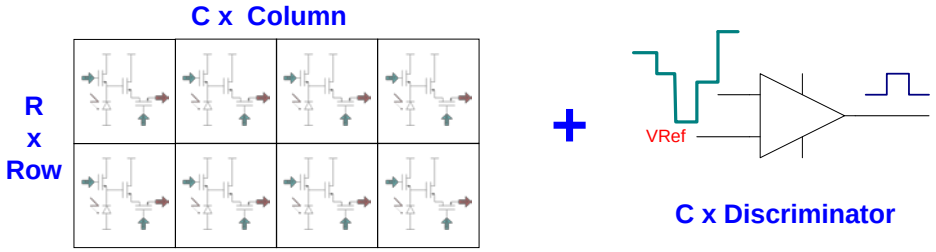
Test & Characterization ➔ CPS Design Steps

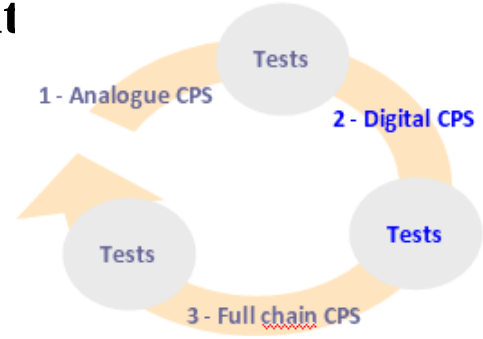
- **First Step ➔ Pixels matrix – CPS with Analogue output**



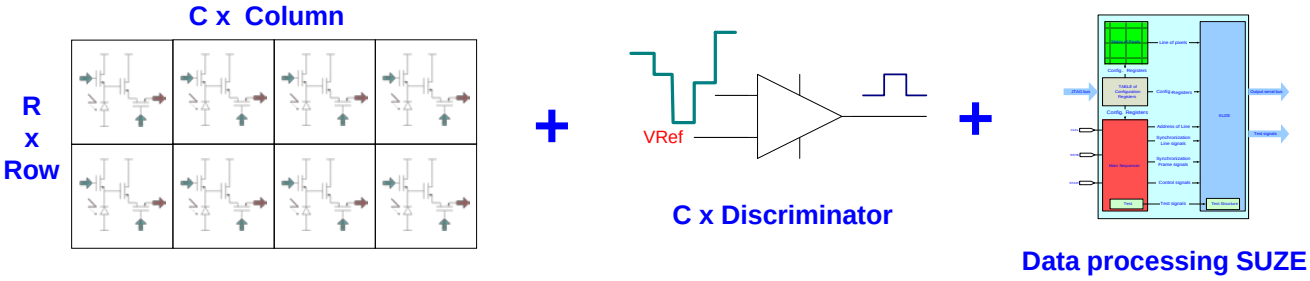


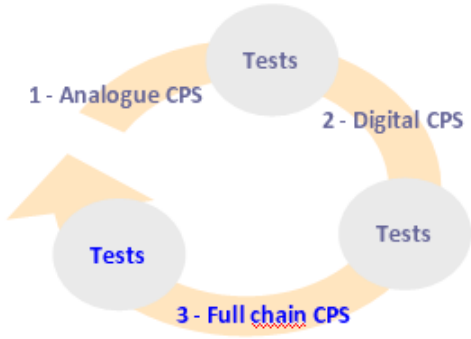
- **Second Step ➔ Signal digitization – CPS with Digital output**





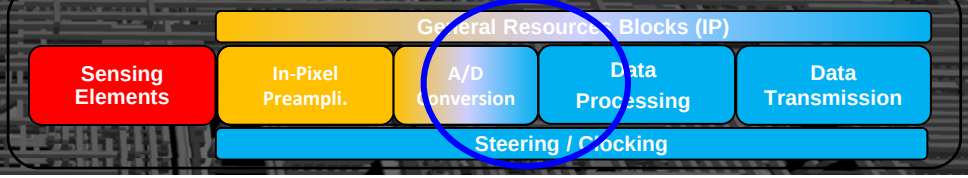
- **Third Step ➔ Data processing – Full chain CPS**





Conclusion : New CPS ➔ Three Prototypes - Analogue - Digital - Full chain
+ IP Electronics blocs

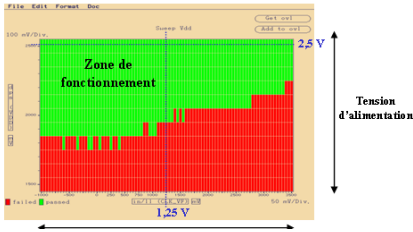
IP Blocs



- IP, Building blocks
  - Electronics blocks (Buffer, DAC, Discriminator, PLL, Data processing logic) needed to build CPS
  - Input & Output are electronic signals
    - Validation can be done at ~ 100 % by simulation at CPS design stage !
  - Why building and testing prototypes ?
    - Safety rule
      In case of new complex design
    - Evaluate robustness /
      - Voltage variations
      - Temperature variations
      - Radiations
      - etc …

Generators, Scop

IP on Test board



Test results

IP Blocs test bench

CPS Designer - Hung Pham

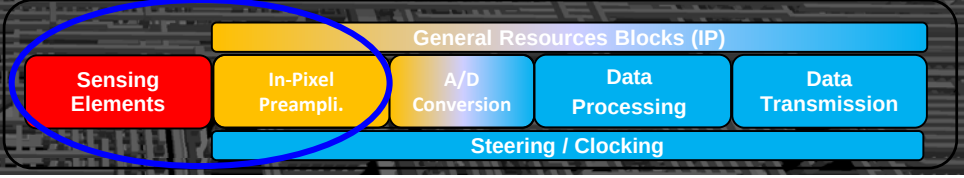
- Test and Characterization
  - Like ASIC
    (Application Specific Integrated Circuit)
  - Classic test benches
    - ASIC PCB
    - Analog / Digital waveform generators
    - Voltmeters, Oscilloscope, Logic analyser

} **Characterization done by CPS Designers & Test Engineers**

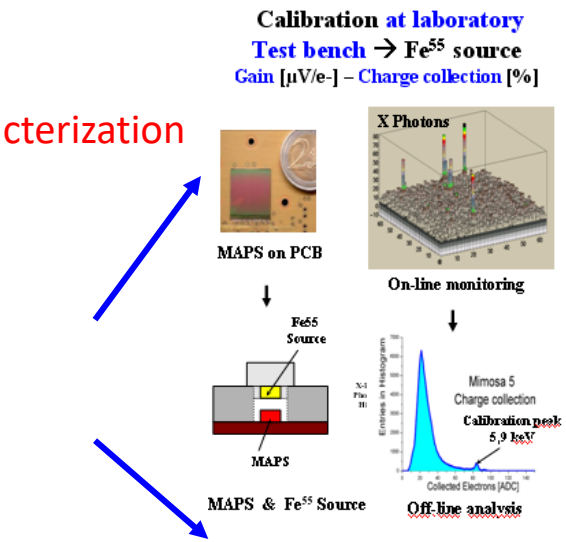
Test Engineer
K.Jaaskelainen

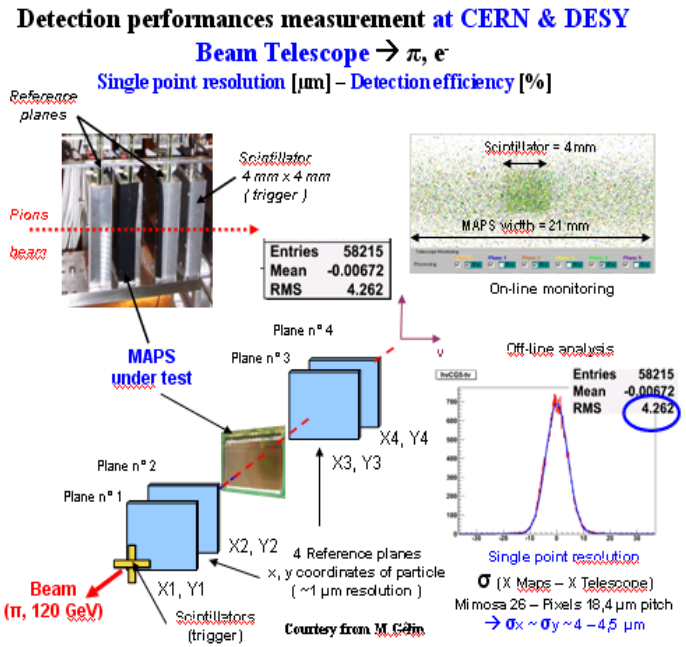
CPS Designer
G.Doziere

1 – Analogue CPS

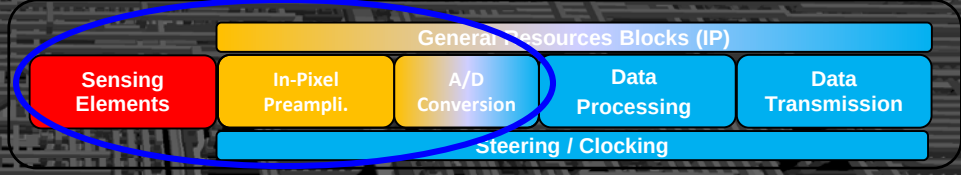


- Pixels characterization
  - Validation by simulation not possible ➔ Prototypes + Characterization
  - Characterization in two steps
  - At laboratory ➔ Estimate the S/N ratio
    - CPS excited by X Photons (Fe55) – Beta (Sr90)
      - Noise (e-)
      - CVF (Charge Voltage Factor) ⇔ Gain (uV/e-)
      - Charge collection (%)
  - In Beam Test (CERN, DESY) ➔ Particles position detection
    - CPS in a beam (Pions, e-) Telescope Particles
      - Spatial resolution [µm] ➔ 1-5 µm
      - Detection efficiency [%] ➔ > 99,5 %
- Characterization requires experts
  - Electronics Engineers ➔ Test bench construction
  - Physicists ➔ Pixel + Beam test data analysis
  - Microelectronics Engineers ➔ Test results analysis
  - Instrumentation Engineers ➔ System operation, Safety





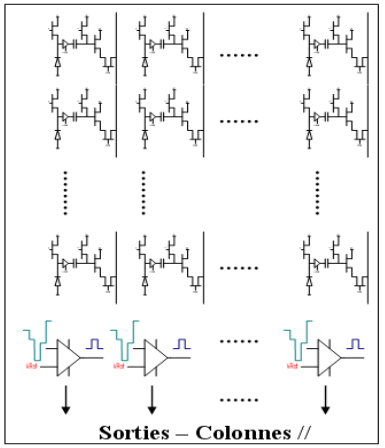
2 – Digital CPS



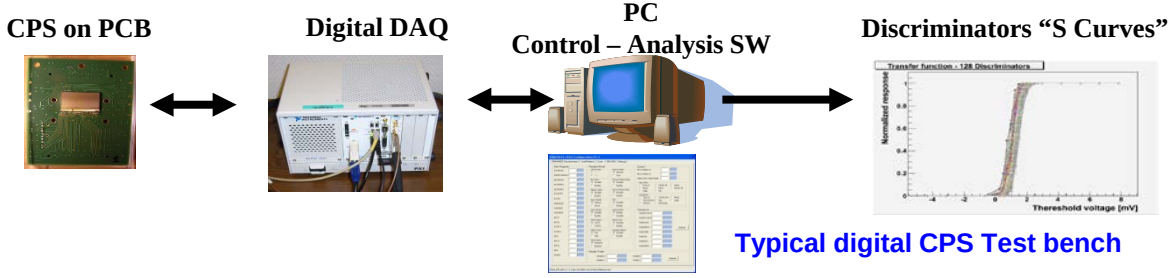
- Pixels + A/D chain
  - A/D = Discriminator (ADC one bit)
  - One discriminator / column or / Pixel
    - Example : Mimosa 26 (EUDET) 8680 fr/s = 1152 discriminators @ 10 MHz
- At laboratory ➔ Discriminators electric performance
  - 50 % Threshold distribution [mV] ➔ FPN ~ 0,5 mV
  - Noise distribution [mV] ➔ TN ~ 0,5 - 1 mV
- In Beam Test ➔ Detection performance (Resolution, Detection efficiency)
- Characterization requires experts
  - Electronics Engineers
  - Physicists
  - Microelectronics Engineers
  - Instrumentation Engineers

Digital CPS characterization is mainly an electronics job but physicists involvement is required for Beam Tests

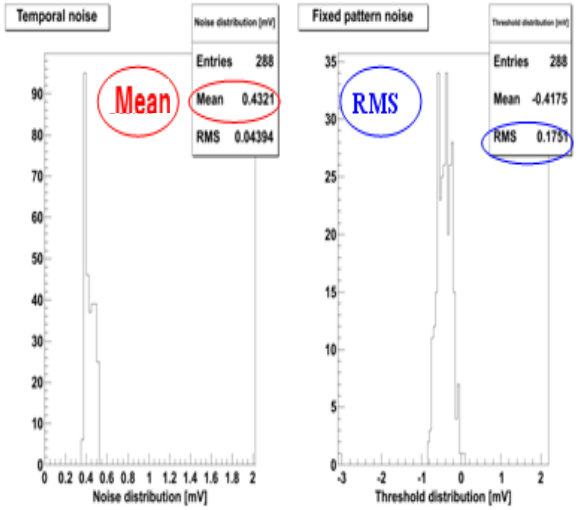
Digital CPS
One A/D (discri) / Column



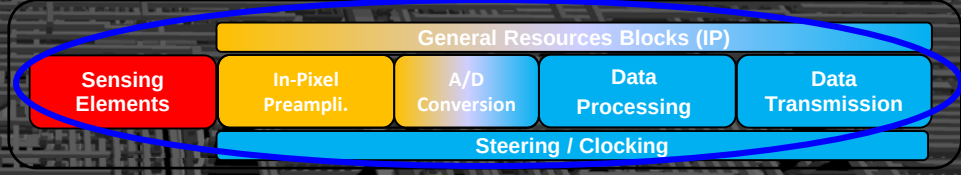
Discriminators TPN & FPN



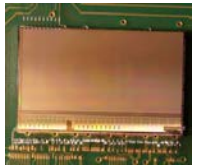
Typical digital CPS Test bench



3 – Full Chain CPS

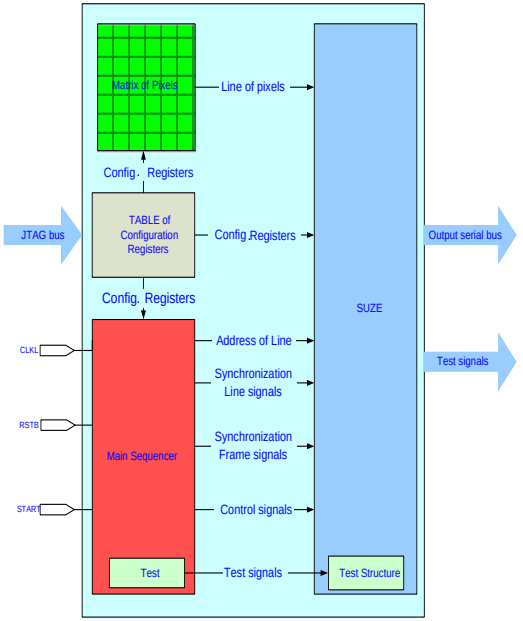


- Pixels + A/D chain + Data processing
  - Data processing = Data « compression » by Zero Supression logic
  - ZS = Read only fired pixels (removedzero = pixels not fired)



Mimosa 26
600 k pixels @ 8680 fr/s

- Testability integrated in CPS in order to check each block at laboratory
  - Pixel analogue
  - Pixels + Discriminators
  - Pixels + Discriminators + Data Processing

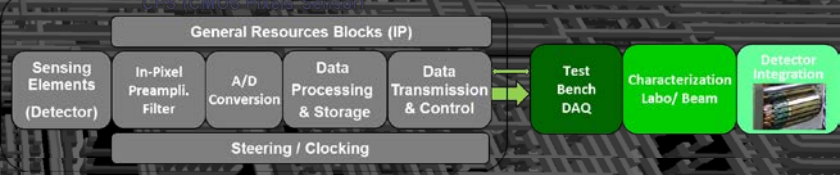


- Once blocks are checked ➔ Beam Test
  - Spatial resolution [µm] ➔ 1-5 µm
  - Detection efficiency [%] ➔ > 99,5 %

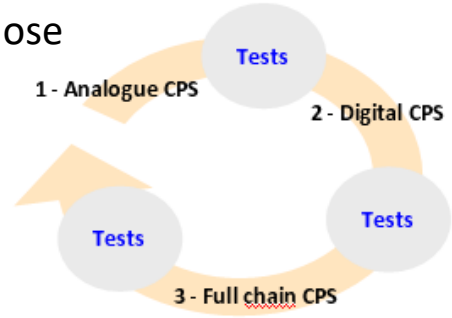
- Characterization requires skills & Experts in
  - Physics ➔ Beam test data analysis
  - Microelectronics ➔ Test results analysis
  - Electronics ➔ Test bench + Measure
  - Instrumentation ➔ System, Safety

Close and strong collaboration between Electronics engineers Microelectronics engineers Physicists

Irradiations



- Evaluate CPS, IP blocs radiation hardness
  - Characterize (at Laboratory or/and in beam test) non irradiated CPS, IP
  - Irradiate CPS at a given dose
  - Characterize again CPS
  - Etc …



M.Goffe
Characterization
Irradiation – Beam Tests

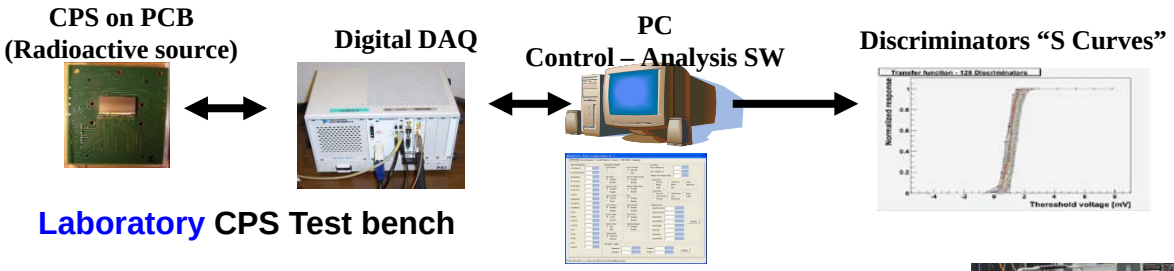
X rays Irradiation tests CERN

- Effects of radiations
  - Ionising radiations
    - Increase of Noise, Leakage current, Thresholds shift
  - Non ionising radiations
    - Done on bare chips
    - Reduction of Charge collection, Increase of Noise, leakage current
  - Transient effects : SEE (SEU, SEL, SET)
    - Generate errors, mainly on digital electronics (bit flip, etc)
    - Latchup

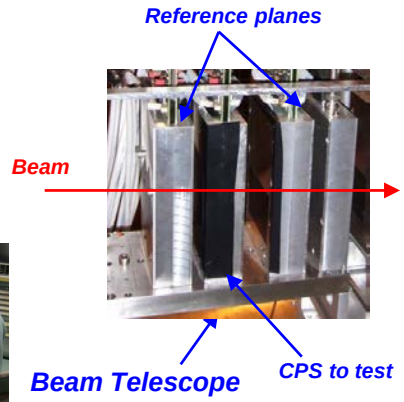
- Irradiation sites
  - Ionising ➔ CERN (CH), KIT (DE)
  - Non ionising ➔ Dubna (RU), Garching (DE), Ljubljna (SI)
  - SEU,SEE, SEL ➔ Louvain (BE), SIRAD (IT)

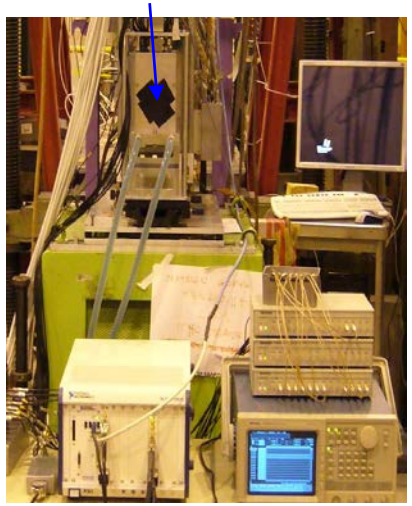
- CPS sensors radiation tolerance
  - Mimosa 28 (STAR) (tested until)
    - 150 krad (500 krad)
    - 3.10^{12} N_{eq} /cm² (3.10^{13})
  - Mimosis_0 (CBM)
    - > 3 Mrad (22 Mrad)
    - > 3.10^{13} N_{eq} /cm² (1.10^{14})

Test Benches Development & Validation



DAQ validation
G. Claus – M. Specht

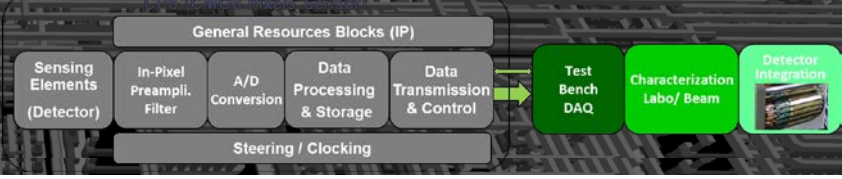




Beam Telescope & DAQ
At CERN

- Two types of test benches
  - Laboratory test benches
  - Beam Test Telescopes (+ DAQ)
- Test benches are developed by the Test Team
  - Digital & Analog electronics : CPS support, Buffers, …
    - Collaboration with MicroTechnics & Mechanics teams
  - DAQ systems : Mainly COTS (Commercial of The Shelf)
  - FW (VHDL, LabVIEW FPGA) & SW (C, C++, Python, LabVIEW, EPICS)
- Key aspects
  - They evolve in // as the CPS architectures ➔ **Anticipate** CPS evolution
  - They are ready when the CPS is back from foundry
- Test benches : HW, DAQ, Analysis SW Development & Validation > 50 % of Team activities

CPS Technology Deployment



- **From Laboratory prototypes to Demonstrators ➔ Instruments ➔ HEP Detectors**


M.Specht


K.Jaaskelainen


M. Szelezniak


M.Goffe

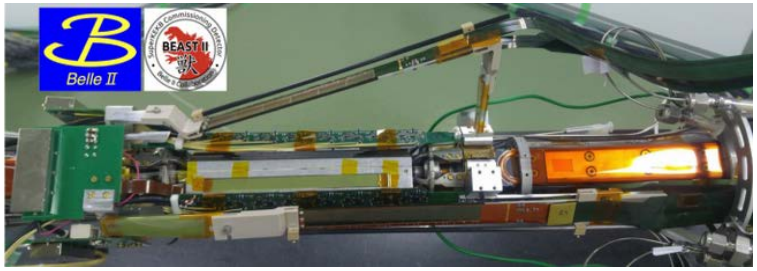

G. Claus

- Proof of readiness / maturity of the CPS Technology
  - Contribute to R&D on detection modules : PLUME, SALAT, …
  - Technical support to the CPS end-users
    - Instruments : EUDET (FP6) & AIDA (FP7) Telescopes
    - Detectors :
      - STAR Detector BNL USA
      - BEAST KEK Japan

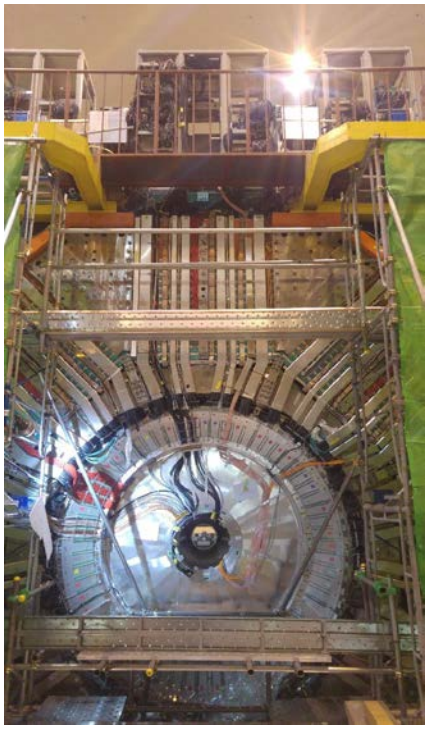

EUDET Beam Telescope

- Test team actions for CPS Technology deployment
  - Organize training on CPS, DAQ, Integration
  - CPS characterization (EUDET, STAR)
  - DAQ solution proposal (EUDET)
  - Detector development, installation & commissioning
    - Example ➔ BEAST for BELLE II
    - Strong contribution from MicroTechnics + Mechanics Teams


BEAST DAQ



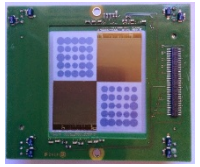
2 x PLUME ladders in BEAST detector


BEAST for BELLE II

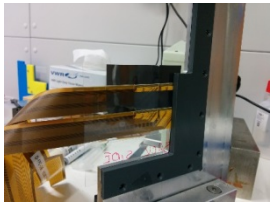
CPS Technology Deployment - Collaborations

- CPS Detection module / Integration projects

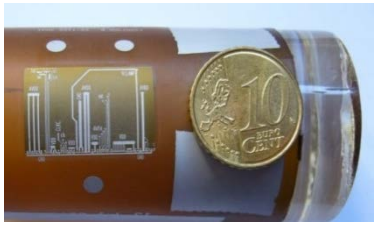
PLUME ladder
8 x 106 Pixels - 8680 fr/s



SALAT Plane (FP7)
4 x 10^6 Pixels 5400 fr/s



PRESTO (IKF)

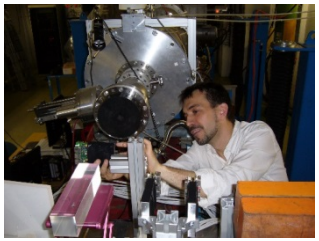


Sensor encapsulation (IPHC)

- Instruments for Hadrontherapy projects

FIRST (GSI) 2010-2012

CYRCé (IPHC) 2015

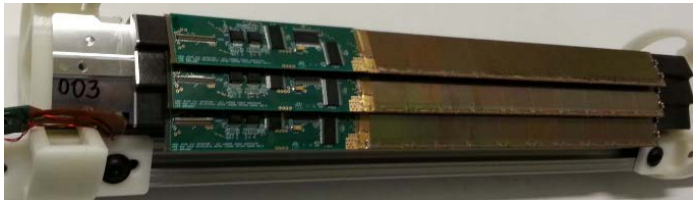


Biophysiks (GSI) 2012

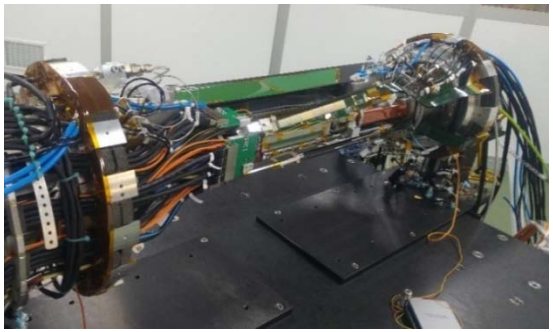
Padme (BNF) 2018

- HEP Detectors

STAR Detector 2013 - BNL
40 x Mimosa 28 ladders

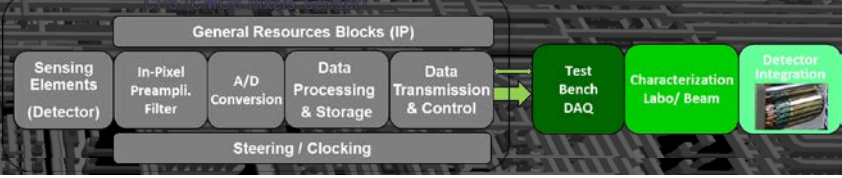


3 x STAR Ladder designed by BNL USA
1 Ladder = 10 x Mimosa 28 – 10 x 10^6 pixels @ 5400 fr/s



BEAST detector – 2018 – KEK Japan
2 x PLUME ladders – 2 x 8 x 10^6 pixels @ 8680 fr/s

Test Team: Conclusion & Future



Tasks	Systems developeme,t	Characterization Labo/Beam Test	Détectors integration	Others
FTE (Average 5/an)	3,1/an	1/an	0,5/an	0,4/an

- CPS Characterization ➔ Large field of activities
- We master all the CPS life cycle steps
  - Test benches development and validation
  - CPS characterization
  - CPS integration in detectors

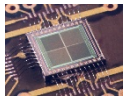
This is possible thanks to a close collaboration between
- Physicists
- CPS Designers
- Test Engineers

- We must concentrate efforts on CPS characterization
- Characterization & Test Benches development are running in //
  - Numerous test benches (TB) are required + Manpower
  - 6 Characterization TB – 3 Development TB - 4 Beam Telescopes - 5 Test Engineers
- Future challenges
  - Fast serial links >= 1 Gb/s & HEP standard DAQ, like IN2P3 DAQGEN project
  - Improve Simulation / Tests integration for digital blocks
  - New technics for wafer scale CPS

CPS R&D Milestone

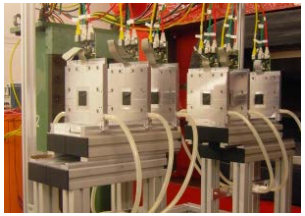
Proof of principle

1999



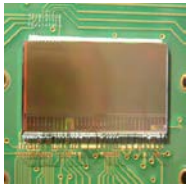
Mimosa-1
6,5 mm² - 16 k pixels
600 fr/s – Analogue output

2009



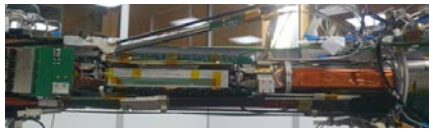
EUDET Beam Telescope

2008



Mimosa-26
2 cm² - 0.6 10⁶ pixels
8400 fr/s - Digital

2018

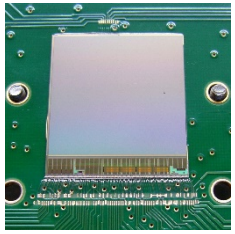


PLUME detectors in BEAST - 2018

2013

STAR detector

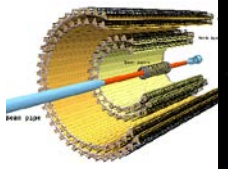
2011



Mimosa-28
4 cm² - 10⁶ pixels
5400 fr/s - Digital

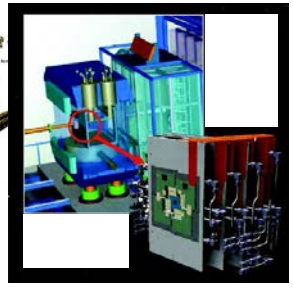
ILC
Pixel: ~ 22 x 22 µm²
>1 Mfr/s

2020



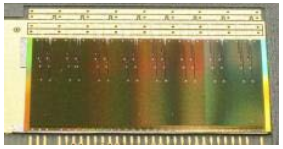
ALICE ITS

20XX



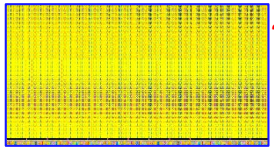
CBM MVD

2016



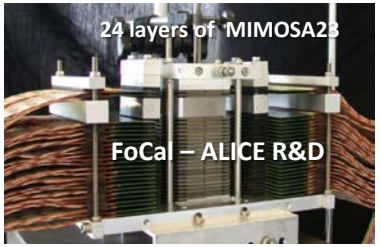
ALPIDE
4.5 cm² - 0.5x10⁶ pixels
~100 kfr/s - Digital

2019



Mimosis-1 2019
~ 5 cm² 0.5 10⁶ pixels
Pixel ~30 x 27 µm²
200 kfr/s - Digital
....
Mimosis-2 2020

Mimosa5: proto. SUCIMA project
Mimosa5: EBCMOS IPNL



Mimosa23: FoCal-ALICE R&D

Mimosa26: NA61, NA63
Mimosa26: other telescopes
Mimosa26: FIRST Project
Mimosa26: PLUME Project
Mimosa26: QAPIVI Project
Mimosa26: PRESTO demo IKF
Mimosa26: demo CERNWIET

Mimosa28: CYRCé
Mimosa28: FOOT project
Mimosa28: Hadrontherapy
Mimosa28: AIDA EU project
Mimosa28: demo BESIII

Mimosa22-SX: demo SOLEIL
PIPPER: demo X-rays

IMIC: intracerebral probe

Current & Future R&D Activities

Spatial resolution & Higher Functionalities (tradeoff)

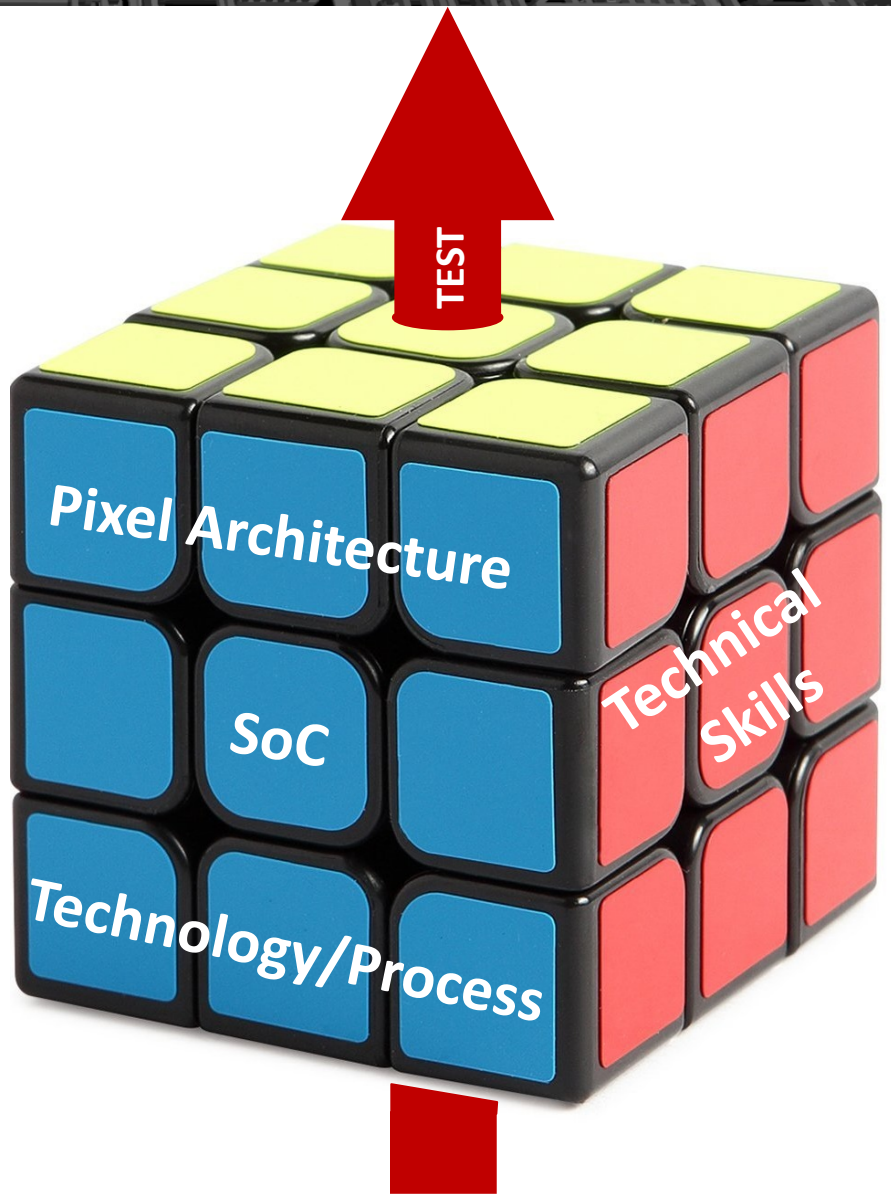
1. Smaller pixel for spatial resolution – new FEE
2. 4D, 5D pixels

Consumption & Complexity

1. Readout strategy (asynchronous)
2. Digital architecture

1. Charge collection improvement
2. Higher integration: 3DIT & wafer scale sensor

Strong international collaboration with foundries



Current & Future R&D Activities

- Very high spatial resolution (σ_s~3 µm)
- Low-voltage and low-power design
- Process stacking
- Radiation tolerance
- Charge collection speed
- …

Collaboration CPPM & Omega

Pixel Architecture: FEE, (σ_s) vs. t (4D) & E (5D) measurement, …

Technical skills

- Physics & SI materials
- Simu. & modeling Si devices: TCAD
- Design: Virtuoso
- Simulation: Spice, Spectre, Monte Carlo
- Verification: PVS, Calibre, QRC, …
- Circuits modeling to Digital flow: Liberate

+

- Ultra low power (<20 mW/cm²)
- Pulsed power operation (for LC)
- Programmable time resolution
- Wafer-scale ultra thin CMOS sensors
- …

Collaboration Frankfurt Univ.

Collaboration SMU, USA

SoC: Readout strategy, Digital architecture, High speed link, …

Technical skills

- …
- HDL modeling, functional verification
- Synthesis & simulation
- Floor-planning, P&R, DRC
- QRC, STA, IR-Drop, Power analysis, …
- System Verilog, UVM, …

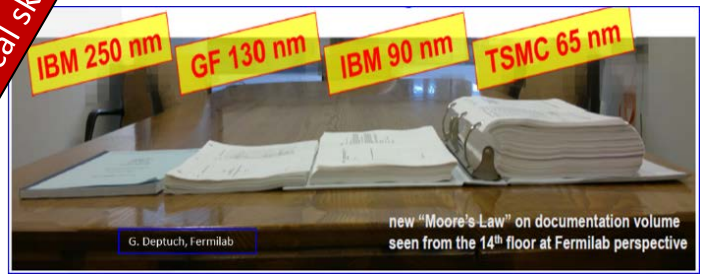
+

Collaboration KEK, Japon

Connected to CERN R&D 2020

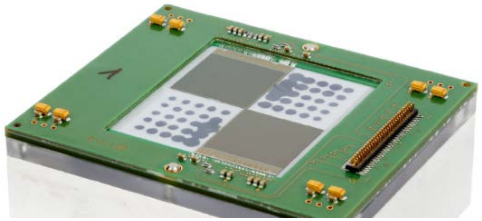
Technology: 3DIT, Process opt., large detector (stitching, 65 nm …)

Technical skills



MicroTechnics: Needs/Wishes for CPS

- MicroTechnics at IPHC is an important actor for our projects
  - Daily contribution: CPS bonding and PCB assembly
  - Low mass detectors modules construction (Flex–Rigid PCB)
    - PLUME ladder
    - Telescopes SALAT for AIDA (FP7)



- **For the future** projects following topics have to be evaluated carefully
  - **Maintaining** human expertise & technical resources
  - Studying **enabling technologies**
    - Different chip connections techniques
      - Die-to-die interconnections (e.g. direct bonds)
  - **R&D on assembly** of new ladders & wafer scale sensors
    - Data and power transmission
  - QC tools and procedures
    - Metrology
    - Infrastructure

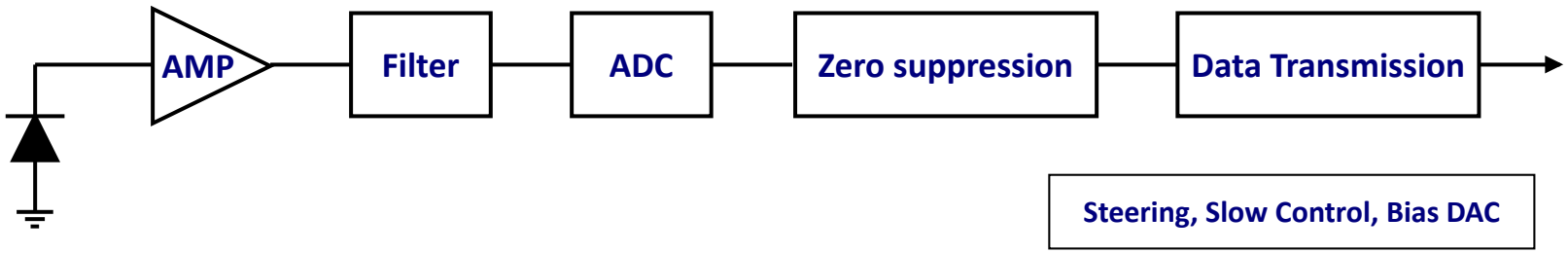
International collaborations

Conclusions

- We design(ed) **key sensors** for HEP and **continue** collaborating for this purpose
- We contribute to the **spread** of the CPS technology via many users of our sensors
- We **master the complete CPS development chain**: Definition, Design and Validation
- **Interaction with physicists** for:
  - Elaborating technical positioning strategies within collaborations
  - Defining the specifications, Finding the best trade-off for the process options, Evaluating CPS performance (lab test & beam)
  - Arguing on the results from the point of view of the physics experiment
  - Looking for synergistic CPS applications
- **Critical size** ➔ to have an **impact** in international scientific ***colla***boration/com***petition***
  - ⊕ **Upstream R&D** on sensor architectures and design techniques
- Importance to **collaborate** with Institutes like CERN, KEK, … allows to
  - Have an **access** to the foundry process information, Contribute to **process optimisation**
- **But how to maintain this capacity ?**

Back Up

Main Components of the Signal Processing Chain

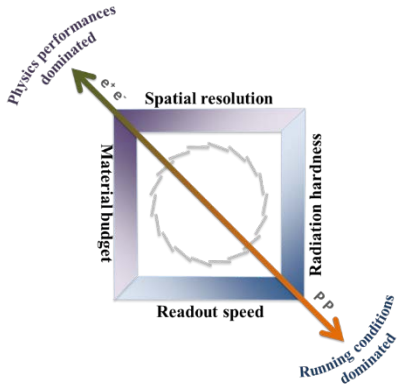


- Typical components of read-out chain
  - AMP: in-pixel low noise pre-amplifier
    - Low signal value: ~ 80 e-h+ pairs/µm ➔ signal O(1 Ke^-) collected by a cluster of ~3-5 pixels➔ low noise
  - Filter: in-pixel filter ➔ low noise
  - ADC: analog-to digital converter (1 bit = discriminator)
  - Zero suppression: only hit pixel information is retained and transferred
  - Data transmission: O(Gbits/s) link implemented on sensor periphery
- Read-out in general data-driven
  - Synchronous: clock distribution over pixel array ➔ power consumption
  - Asynchronous: no clock running over pixel array ➔ increased design complexity?

- Trade-off between conflicting parameters

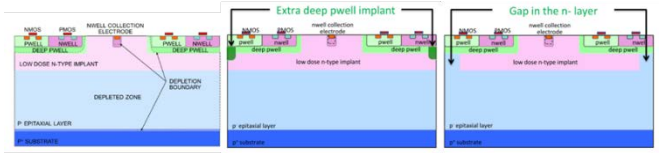
Pixel Architecture

MIMOSIS sensor = starting point + Project driven



- Very high spatial resolution (~ 3 µm)
  - Trade-off between spatial resolution and readout speed
  - High level integration benefit from very deep submicronic feature size processes and 3DIT
- Analogue power consumption
  - Small electrode (C ~ 5fF), analogue power ~ $(Q/C)^{-2}$
  - Improvement in S/N also good to improve timing jitter
- Radiation tolerance
  - AC vs DC coupling
  - Process optimisation: charge collection response + radiation tolerance
  - Simulation only (IPHC), contact to foundry via CERN ➔ it is necessary to be in the decision loop (CERN)

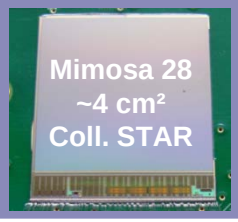
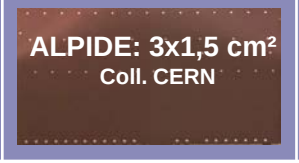
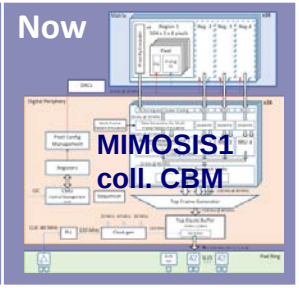
Process Optimisation (CERN-Foundry)



- Time resolution (sub-nanosecond)
  - Collaboration project with CPPM (QUARTET, IN2P3 upstream R&D)
  - ToA measurement, TDC for group of pixels? R&D on new architecture
  - Wider pixel pitch?
- Energy resolution
  - ToT measurement vs. ADC? particle identification? ➔ need investigation
- In-pixel memories
  - Keep data in pixel until level 1 (trigger) ➔ power trade-off

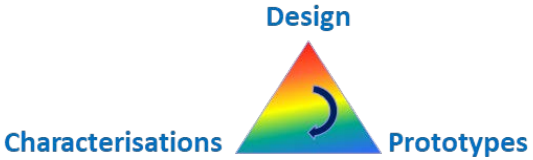
SoC

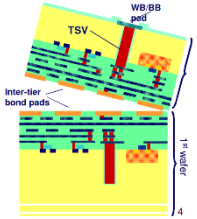
- Power consumption:
  - Trade-off between hit activity (average, fluctuation) and clock: Synchronous vs. asynchronous RO
  - On-chip power management
  - Reconsider circuit architecture design for wafer-scale sensor (stitching)
- Digital signal flow & state machines with & w/o SEE protection
  - From pixel outputs, zero suppression, data aggregation to transmission
- Digital design evolution:
  - More and more on-chip embedded signal processing➔ strong impact on design tools AoT→ DoT

Design Tools \ Chips	2005	2010-2012	2015	2016	Now
					
Verilog/ VHDL	✓	✓	✓	-	✓
STA		✓	✓	-	✓
IR-Drop			✓	-	✓
LIBERATE				✓	✓
SV-UVM					✓
LEC					

Process/Technology/Foundry

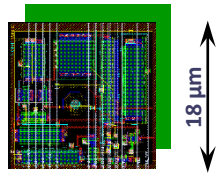
- Selection of the right process and foundry is a crucial step
  - Twin well (0.35 µm) $\xrightarrow{2011}$ Quadruple well (0.18 µm)
    - Increase digital circuit density, speed & power
    - Gain freedom in pixel design (NMOS vs. CMOS)→ readout speed x 10
- Process optimisation (CERN + foundry)
- 3DIT: stacked imagers
  - 3D integration (ASICs need to be designed to allow for this)
    - 2009 Fermilab Tezzaron multiproject Run
    - 2019: SOI stacking ➔ spatial resolution (~ 3 µm)
- Post processing (e.g. thinning <30 µm, dicing, redistribution layers-RDL)
- Wafer scale sensor (CERN)
  - Stitching + thinning ➔ Exploit flexible nature of Si?
  - Realise truly cylindrical detectors



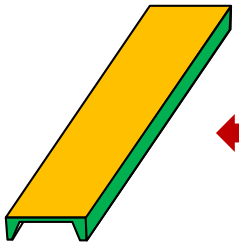


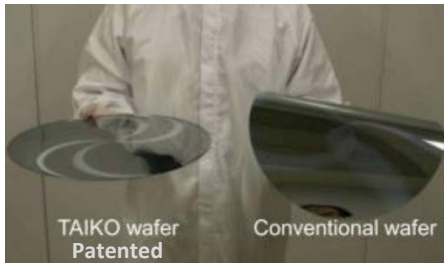
2009 Coll. FermiLab

2nd RO layer to realise

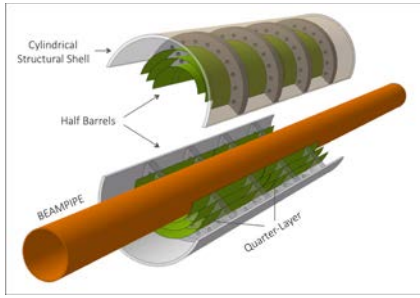


2019 Coll. KEK


Thin & rigid ladder

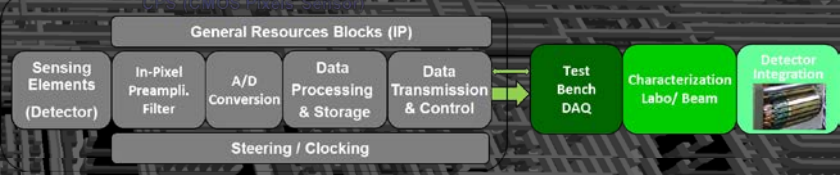


Wafer support by the outer rim



Thin cylindrical detectors

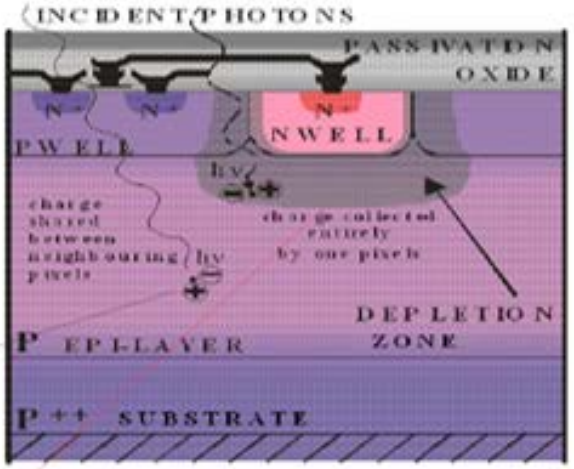
CPS characterization at lab



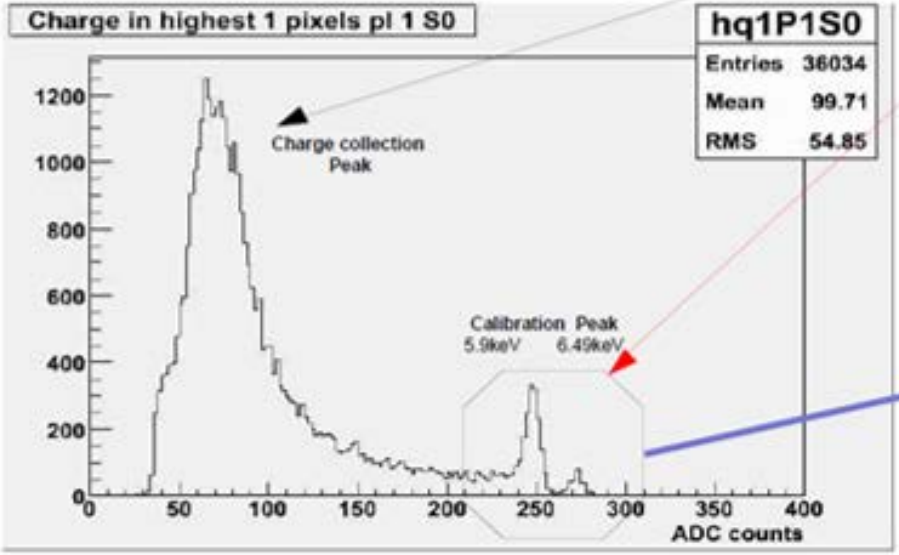
Calibration of the conversion gain - with soft X-rays

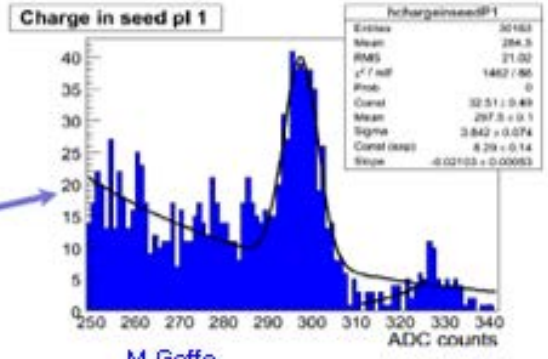
Emission spectra of a low energy X-ray source e.g. iron ^{55}Fe emitting 5.9 keV photons.

very high detection efficiency even for thin detection volumes, constant number of charge carriers about 1640 e/h pairs per one 5.9 keV photon



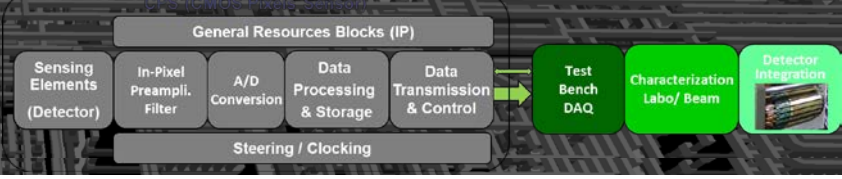
The ' warmest ' colour represents the lowest potential in the device





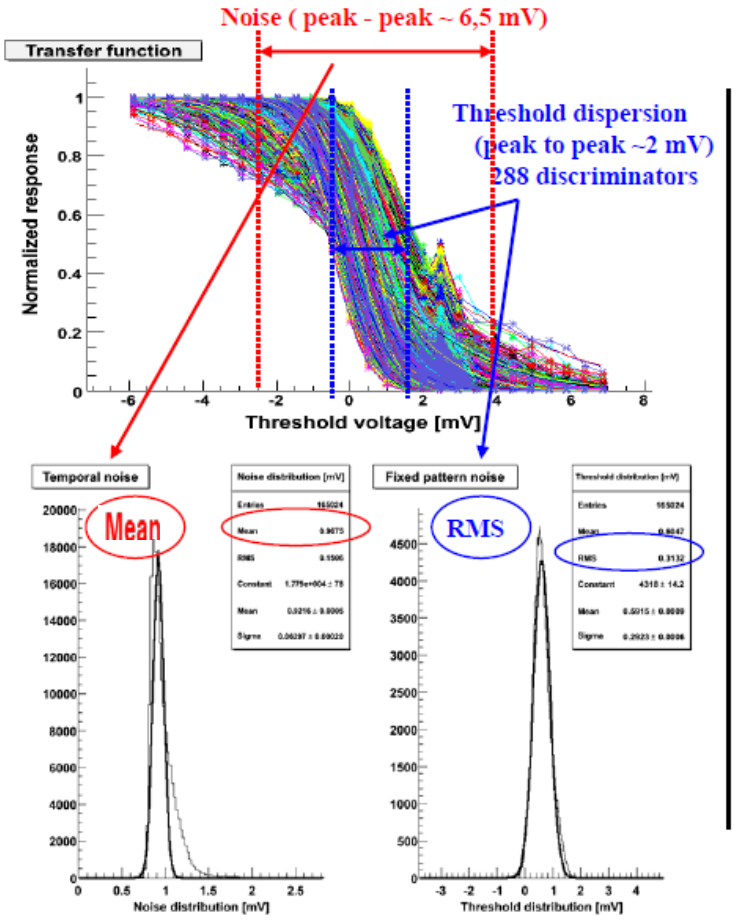
M.Goffe
2015_capteurscmos_details.pdf

Discriminators characterization



iPHC MAPS Standard characterization protocol → Example of Mimosa 26

Pixel + Discriminator characterization → The whole chain …

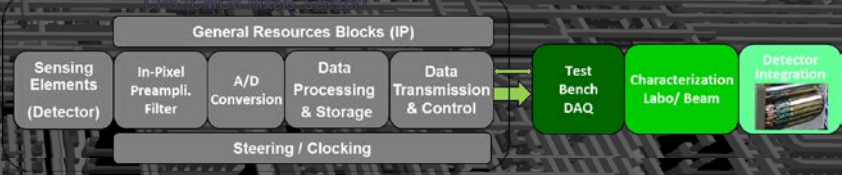


Marie.Gelin@ires.in2p3..fr

Characterization procedure

- Scan discriminators threshold to get " S curves "
- One curve / pixel → 663 552 curves (165888 / sub matrix)
  - One threshold → Run of 1000 events ~ 3 minutes
- Extract
  - Noise distribution → TPN ~ 1 mV
  - 50 % Threshold distribution → FPN ~ 0,3 – 0,4 mV
  - 30 Threshold steps → 1H30 DAQ + 1 H Analysis
  - Total 2H30
- Study influence of critical parameters
  - Temperature
  - Irradiation → Ionizing & Neutrons

CPS Beam Test

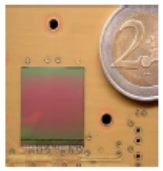


MAPS R&D cycle → MAPS Characterization at Laboratory & in Beam test

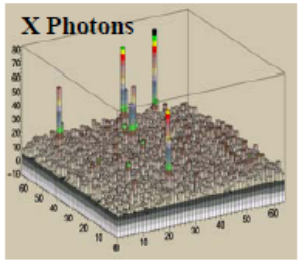
Calibration at laboratory

Test bench → Fe^{55} source

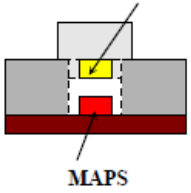
Gain [µV/e-] – Charge collection [%]

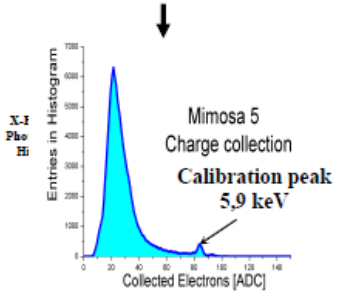


MAPS on PCB



On-line monitoring





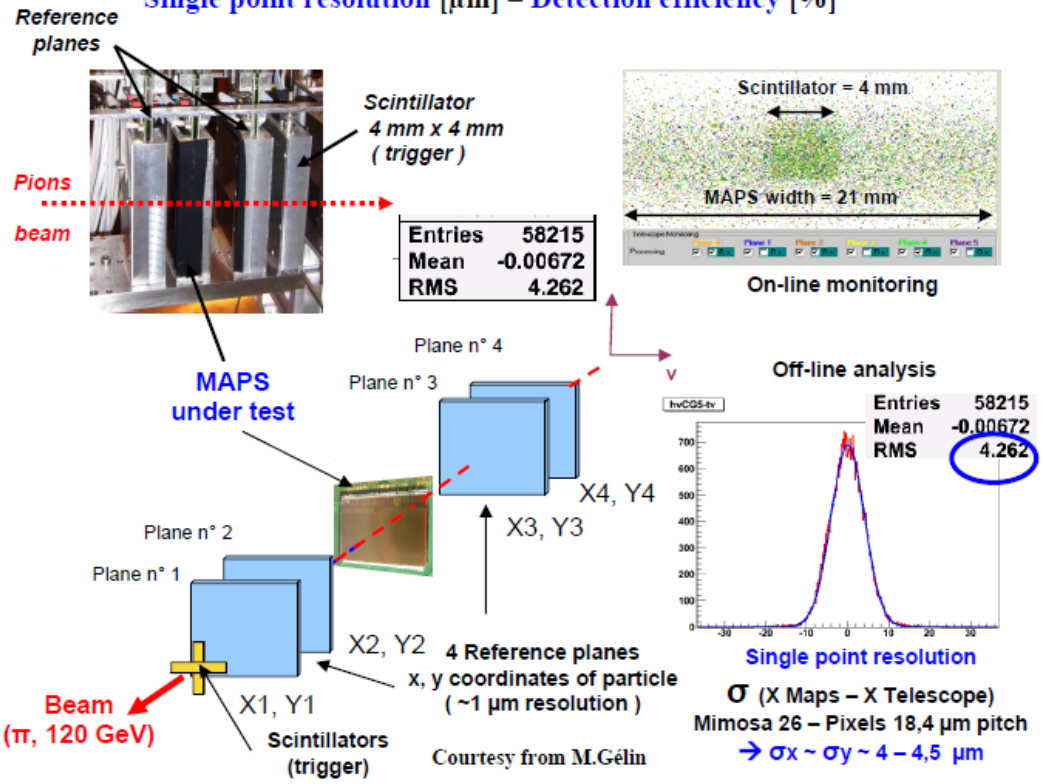
MAPS & Fe^{55} Source

Off-line analysis

Detection performances measurement at CERN & DESY

Beam Telescope → π, e^-

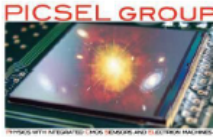
Single point resolution [µm] – Detection efficiency [%]



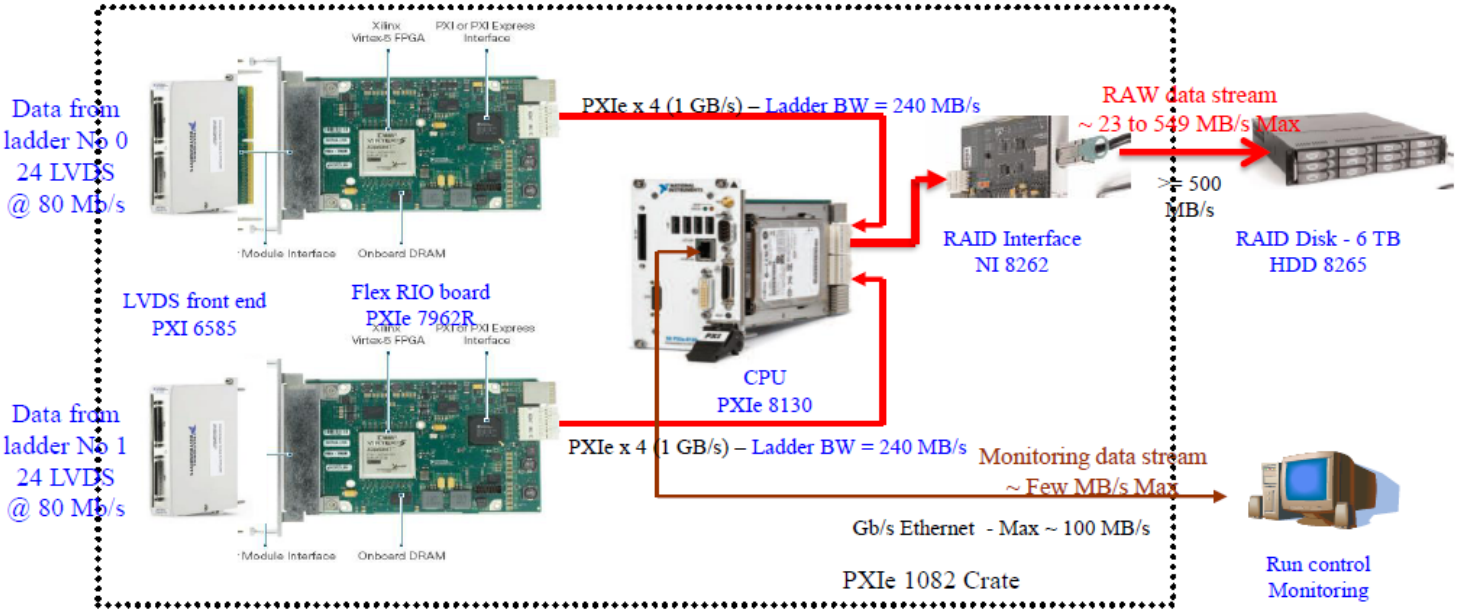
MAPS test bench → Needs DAQ → DAQ boards developed at lab until ~ 2007

CPS DAQ BEAST

3 - DAQ : Hardware NI PXIe



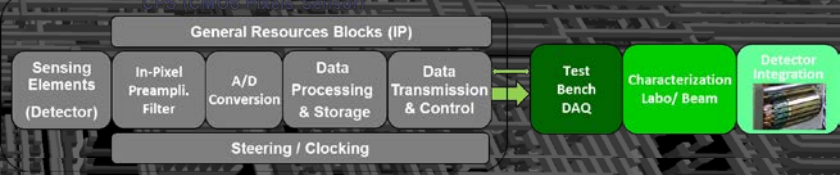
- Based on the IPHC PXIe NI FlexRIO board (EUDET & AIDA Telescopes)
  - **Input :**
    - Beam cycle signal : Time stamping with 0,2 us resolution
    - 2 Ladders data stream = 2 x 8 .10^6 pixels @ 8680 fr/s = 24 x Mimosa 26 = 48 links @ 80 Mb/s = 480 MB/s
  - **Output**
    - Ladders RAW data stream @ 8680 frames/s ➔ RAID system ~ 23 to 549 MB/s (see slides 11, 12)
    - Processed data Eg : Nb hits / Mi26 / Time unit ➔ Ethernet Few kB/s (see slide 13)



10

G.Claus BEAST II MiniWorkshop, KEK 31 January 2016

Discri in pixel – MIMOSIS (IPHC)



MVD: sensor requirement

	ALPIDE (demonstrated)	MIMOSIS (MVD design goal)	Factor
Ion. Rad. Tolerance	2.7 Mrad	> 3 Mrad	1
Non. Io. Tolerance	1.7 10^{13} neq/cm²	> 3x10^{13} neq/cm²	2
Heavy ion tolerance	N/A	1 kHz / cm²	--
Time resolution	5-10 µs	5 µs	2
Hit rate	> 12 kHz/mm²	700 kHz/mm² (peak)	56
Data rate	1 Gbps	2.5 Gbps	2.5
Data reduction	Trigger	Elastic buffer	--
Power consumption (depending on hit density)	20-35 mW/cm²	50-75 mW/cm²	0.4
GBTx compatible	No	Yes	--

- **ALPIDE is not sufficient to fulfil all the requirements of the MVD**
- **Need a new architecture based on ALPIDE**

Joachim Stroth | 56th Winter Meeting on Nuclear Physics | Bormio (Italy)

Mimosis TWEPP 2018
F.Morel & all (IPHC)

Equipe

Nom	Grade IT & Doctorant	Profil
Bertolone Grégory	IE2	Numérique/Support
Claus Gilles	IR2	Test/DAQ
Colledani Claude	IRHC	Numérique
Dorokhov Andrei	IR1	TCAD/Analog/Mixte/Test
Doziere Guy	IR1	Numérique
Goffe Mathieu	IE2	Test
Himmi Abdelkader	IR1	Numérique
Hu-Guo Christine	IRHC	Analog/Mixte
Hu Yann	Prof	Prof
Jaaskelainen Kimmo	IEHC	Test
Kachel Maciej	IR2	Analog/Mixte/Test
Illinger Christian	IEHC	CAD support/PCB
Molinet Sylviane	IE1	Infomaticienne (40%)
Morel Frédéric	IR2	Analog/Mixte/Numérique
Pham Hung	IR2	Analog/Mixte
Specht Mathieu	AI	Test
Szelezniak Michal	IR2	Test
Valin Isabelle	IR1	Analog/Mixte
Zhao Ruiguang	Doctorant	Analog/Mixte/Numérique
Zhao Yue	Doctorant	Analog/Mixte/Numérique

Ph.D Students in Microelectronics

	Prénom Nom	Soutenance de Thèse		Sujet	Note	Equipe
		Année	mois			
1	Michal Szelezniak	2008	Féb.	Développement des capteurs à pixels avec microcircuits intégrés pour le détecteur vertex de l'expérience STAR au collisionneur RHIC	Thèse: Université de Strasbourg	PICSEL
2	Sébastien Heini	2009	Mars	Conception et intégration d'un capteur à pixels actifs monolithiques et de son circuit de lecture en technologie CMOS submicronique pour les détecteurs de position du futur	Thèse: Université de Strasbourg	PICSEL
3	Ndeye Awa Mbow	2009	Juin	Conception et intégration en technologie CMOS d'un circuit de lecture et d'identification de coïncidences à résolution temporelle de l'ordre de la nanoseconde destiné à l'imagerie biomédicale	Thèse: Université de Strasbourg	IMABIO
4	Mokrane Dahoumane	2009	Nov.	Conception, réalisation et caractérisation de l'électronique intégrée de lecture et de codage des signaux des détecteurs de particules chargées à pixels actifs en technologie CMOS	Thèse: Université de Strasbourg	PICSEL
5	Nicolas Pillet	2010	Juin	Conception et intégration de convertisseurs analogique/numérique, compacts, à bas bruit, adaptés aux capteurs CMOS destinés à la détection de particules chargées	Thèse: Université de Strasbourg	PICSEL
6	Quan Sun	2010	Juin	Research on on-chip PLL clock generator for MAPS	Thèse: Beihang University	PICSEL
7	Olav Torheim	2010	Sept.	Design and implementation of fast and sparsified readout for Monolithic Active Pixel Sensors	Thèse: Bergen University	PICSEL
8	Wu Gao	2011	Jan.	Conception d'un circuit de lecture monolithique "Front-End" avec un CTN haute précision et un CAN basé sur le temps en technologie CMOS pour l'imagerie TEP	Thèse cotutelle UDS-NWPU	IMABIO
9	Xiaochao Fang	2011	Mars	Conception et intégration d'une chaîne de lecture faible bruit en technologie CMOS pour un système TEP à base d'APD dédié à l'imagerie du petit animal	Thèse: Université de Strasbourg	IMABIO
10	Ming Fu	2012	Juillet	3D TCAD based studies of high resistivity epitaxial layer pixel sensors	Thèse Dalian University of Technology	PICSEL
11	Yunan Fu	2012	Mai	Développement de capteurs à pixels CMOS pour un détecteur de vertex adapté au collisionneur ILC	Thèse: Université de Strasbourg	PICSEL
12	Ying Zhang	2012	Sept.	Development of CMOS sensors for a future neutron eleetronie personal dosemeter	Thèse: Université de Strasbourg	RAMSES
13	Jia Wang	2012	Sept.	Design of a low noise, limited area and full on-chip power management for CMOS pixel sensors in high energy physics experiments	Thèse cotutelle UDS-NWPU	PICSEL
14	Xiaomin Wei	2012	Dec.	Study and improvement of radiation hard monolithic active pixel sensors of charged particle tracking	Thèse cotutelle UDS-NWPU	PICSEL
15	Liang Zhang	2013	Sept.	Development of a CMOS pixel sensor for the outer layers of the ILC vertex detector	Thèse: Université de Strasbourg	PICSEL
17	Yang Zhou	2014	Sept.	Development of a CMOS pixel sensor for embedded space dosimeter with low weight and minimal power dissipation	Thèse: Université de Strasbourg	PICSEL
18	Wei Zhao	2015	Jan.	Development of CMOS sensor with digital pixels for ILD vertex detector	Thèse: Université de Strasbourg	PICSEL
19	Tianyang Wang	2015	Sept.	Development of CMOS pixel sensors for the inner tracking system upgrade of the ALICE experiment	Thèse: Université de Strasbourg	PICSEL
16	Zhan Shi	2017	Jan.	Microcircuits de transmission rapide intégré dans un capteur CMOS	Thèse Dalian University of Technology	PICSEL
20	Julian Heymes	2018	Juillet	Depletion of CMOS Pixel Sensors: Studies, Characterisations, and Applications	Thèse: Université de Strasbourg	PICSEL
21	RuiGuang Zhao			CMOS Pixel Sensors with on-chip Neural Network		PICSEL
22	Yue Zhao			Radiation Tolerance Design Of CMOS Pixel Sensor For The Compressed Baryonic Matter Experiment		PICSEL

Publications/Workshops (2012-2016)

1. Valin et al., “A reticle size CMOS pixel sensor dedicated to the STAR HFT”, JINST Volume: 7, January 2012
2. W. Dulinski, “New Fabrication and Packaging Technologies for CMOS Pixel Sensors : Closing Gap between Hybrid and Monolithic Slides”, PIXEL 2012, Sept. 2012, Inawashiro, Japan
3. L. Zhang et al., “A CMOS Pixel Sensor with 4-bit Column-Level ADCs for the ILD Vertex Detector”, TWEPP, Sept. 2012, London, UK
4. L. Zhang et al., “CMOS Pixel Sensor with 4-bit Column Parallel Self-triggered ADC for the ILC Vertex Detector”, IEEE International Conference on Electronics, Circuits, and Systems ICECS 2012, Dec. 2012 Seville, Spain
5. Y. Fu et al., “Design and characterization of high precision in-pixel discriminators for rolling shutter CMOS pixel sensors with full CMOS capability”, NIM-A, Vol. 717, July 2013
6. F. Morel et al., “MISTRAL & ASTRAL: Two CMOS Pixel Sensor Architectures Dedicated to the Inner Tracking System of the ALICE Experiment”, TWEPP, Sept. 2013, Perugia, Italy
7. T. Wang et al., “Development of CMOS Pixel Sensor with digital pixel dedicated to future particle physics experiments”, TWEPP, Sept. 2013, Perugia, Italy
8. M. Szelezniak ; A novel MAPS based vertex detector for the STAR experiment at RHIC Slides ; 13th Topical Seminar on Innovative Particle and Radiation Detectors IPRD13, Sienna, 7-10 October 2013
9. C. Hu-Guo et al. “Development of the MISTRAL & ASTRAL Sensors for the Upgrade of the Inner Tracking System of the ALICE Experiment at LHC”, IEEE-NSS, Nov. 2013, Seoul, Korea
10. W. Dulinski, “Post-Processing Step for Monolithic (CMOS) Sensors: Possible Added-on Value”, Mai 2014, Argonne National Laboratory, USA
11. F. Morel et al., “MAPS for ALICE Upgrade and Beyond”, Mai 2014, Argonne National Laboratory, USA
12. M. Kachel, “Development of MAPS Based Telescope for Neutron Spectroscopy”, Mai 2014, Argonne National Laboratory, USA
13. T. Wang et al. “Development of CMOS Pixel Sensor Featuring Pixel-Level Discrimination for the ALICE-ITS Upgrade” TIPP, June 2014, Beurs Van Berlage, Netherlands
14. Y. ZHOU et al. “COMETH: a CMOS pixel sensor for a highly miniaturized high-flux radiation monitor”, TIPP, June 2014, Beurs Van Berlage, Netherlands
15. C. Hu-Guo et al., “Design of CMOS Pixels Sensor for the STAR Experiment”, CPIX, Sept. 2014, Bonn, Germany
16. M. Kachel et al., “Fully Depleted MAPS: Peagasus and Mimosa33”, CPIX, Sept. 2014, Bonn, Germany
17. M. Szelezniak, “Upgrade of the STAR Silicon Detectors”, VERTEX, Sept. 2014, Macha Lake, Czech
18. F. Morel et al., “FSBB-M and FSBB-A: Two Large Scale CMOS Pixel Sensors Building Blocks Developed for the Upgrade of the Inner Tracking System of the ALICE Experiment”, TWEPP, Sept. 2014, Aix en Provence, France
19. L. Zhang et al., “A CMOS Pixel Sensor Prototype for the Outer Layers of Linear Collider Vertex Detector”, TWEPP, Sept. 2014, Aix en Provence, France
20. C. Colledani, “HEP Electronics in France”, TWEPP, Sept. 2014, Aix en Provence, France
21. J. Heymes et al., “IMIC – Needle-shaped Low-Power Monolithic Active Pixel Sensors for Molecular Neuroimaging on Awake and Freely Moving rats”, IEEE-MIC, Nov. 2016, Strasbourg, France
22. M. Kachel et al., “MIMOSA-22SX – A Monolithic Active Pixel Sensor for Low Energy X-Ray Counting Applications”, IEEE-NSS, Nov. 2016, Strasbourg, France

Conclusions - Weakness / Solutions -

- Mid term
  - Improve the reactivity
    - Need microelectronic digital designer, …
    - Widen collaborations (both for design and test)
  - ~~**Avoid saturation** by CPS deployment projects → Slow down the R&D~~
    - ~~Concentrate efforts on CPS validation, test bench & Data Acquisition developments for the test team~~
  - Recurrent budget
    - Trainings, technical collaboration missions, workshops, …

- Long term
  - Human resource strategy to maintain technical expertise and task force
    - Call for regular turnover of Ph.D students for upstream R&D
    - Post Doc for dedicated projects
    - 4 people (out of 12) in the design team will be retired in 4 - 7 years