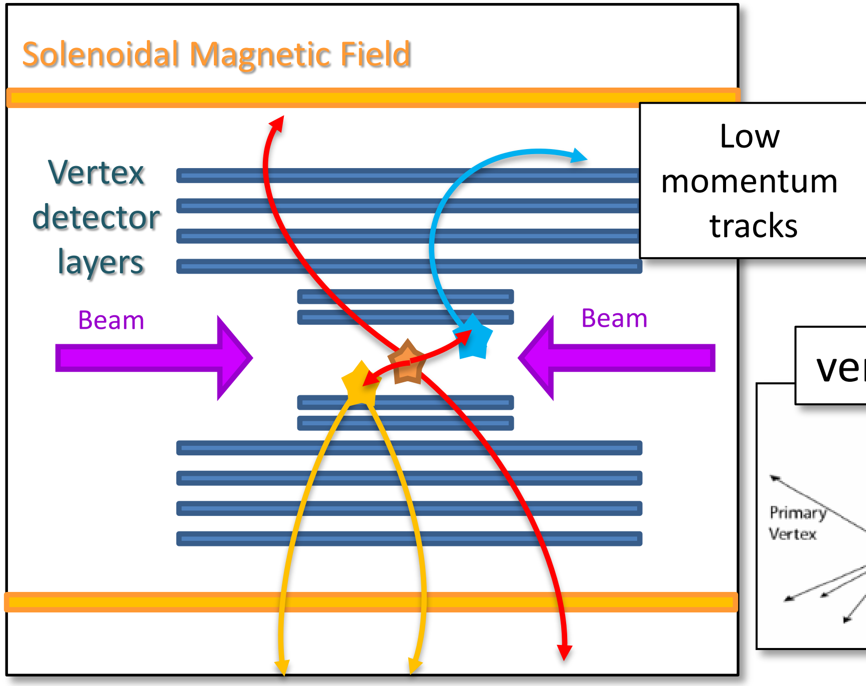
PICSEL

CMOS Pixel Sensors for subatomic physics

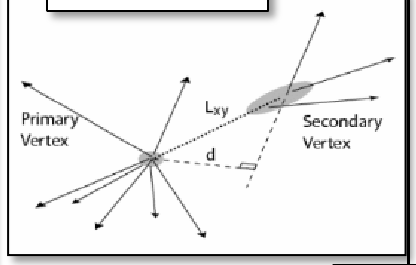
Colliders, fixed target experiments and telescopes

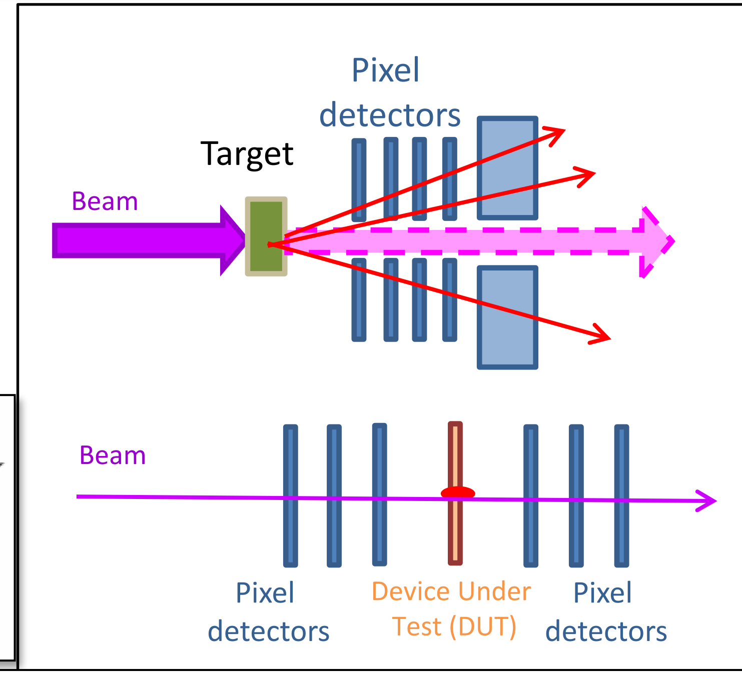
- Introduction
- Past
- Present
- Future & perspectives in other groups

Vertexing and charged particle tracking



vertexing

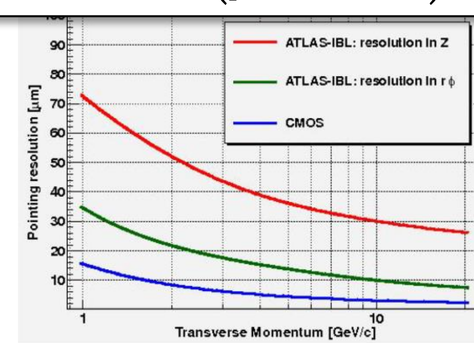




Tracks compared to a Device Under Test

- Why do we need vertexing and tracking ?
  - ✓ Reconstruct Primary and secondary vertex
    - Heavy flavor tagging (b, c, τ)
    - Order of magnitude: O(1µm)- O(10µm)
  - ✓ Low momentum tracking
    - pT ~< 100 MeV/c – 1 GeV/c
  - ✓ Vertex/Jet charge determination

$$\sigma_{d0}{}^2 = a^2 + \left(\frac{b}{p.\sin^{3/2}\theta}\right)^2$$



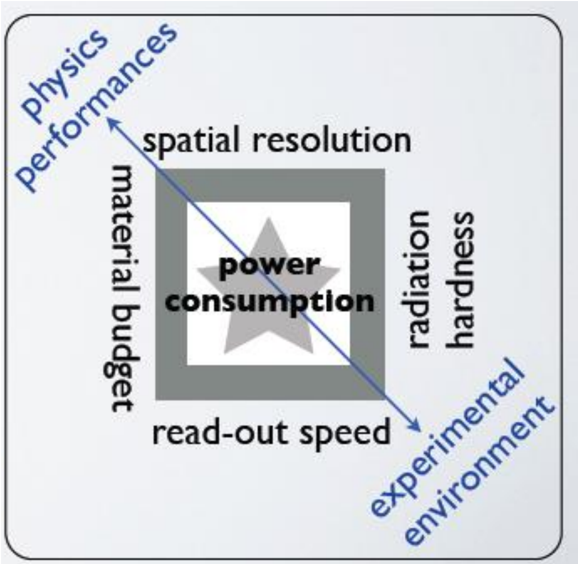
Vertexing: squaring the circle

$$\sigma_{d0}{}^2 = a^2 + \left(\frac{b}{p.sin^{3/2}\theta}\right)^2$$

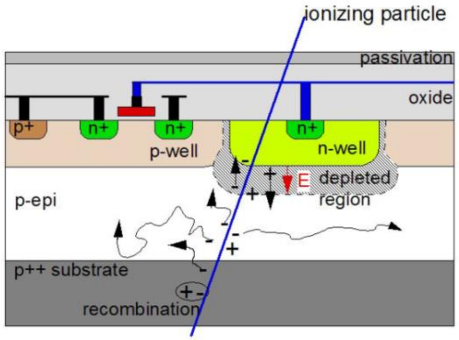
- General trend in particle physics
  - ✓ More statistics & More precision
- R & D : since ~ 1999-2000
  - ✓ Motivated by a Linear e^+e^- collider
- Leptons colliders and heavy ions exp.
  - ✓ Different approach compared to hybrid pixels & LHC
  - ✓ Experimental environment much less demanding

⇨ favors technologies which allow to focus on resolution and material budget

⇨ CMOS pixel sensors (CPS) offer the best compromise

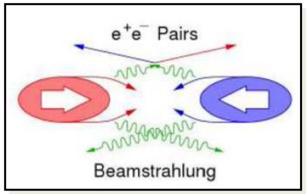


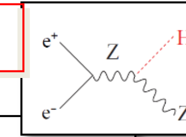
- ✓ Granularity
- ✓ Material budget
- ✓ Signal processing integrated in the sensor
- ✓ Flexible running conditions
  - (Temperature, Power, Rad. Tol.)
- ✓ Industrial mass production



ILD requirements @ ILC

$$\sigma_b < 5 \oplus 10/p\beta \sin^{3/2}\theta \ \mu m.$$

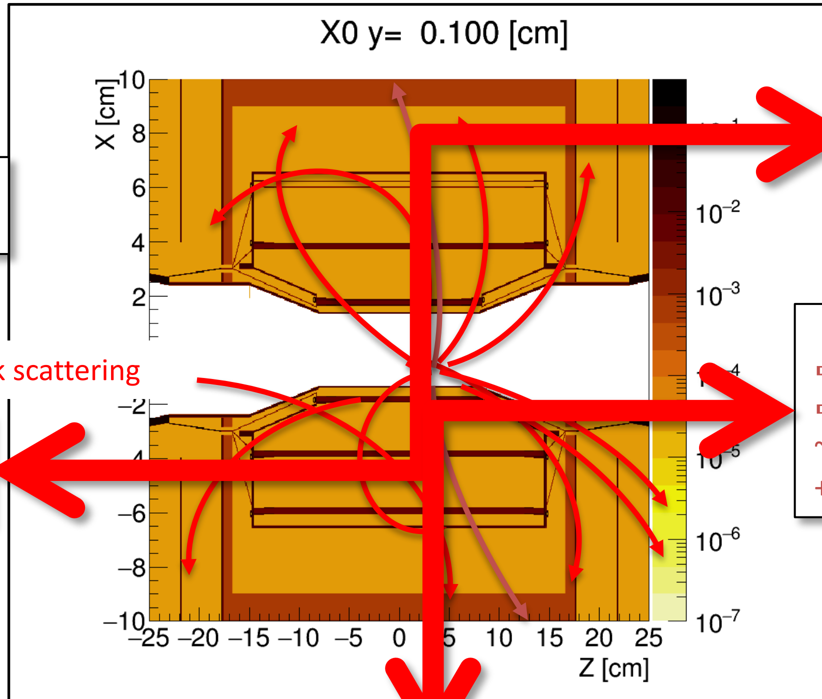




Physics
- ⇨ Flavour tagging
- ⇨ Low pT tracks

Beam background

Beam background (~ 5 hits/BX/cm² on layer 0)



Radiation hardness
O(100kRad/an) & O(10^{11})neq/an

Rad.Tol. devices

Vertex reconstruction
- ⇨ granularity
- ⇨ Pitch ~17 um
- ⇨ (σ_{sp} ~3 um)

Material Budget
- ⇨ ~ 0.15% X_0 / layer
- ⇨ < 1% X_0 for the whole VTX

~ 900 µm Si
+ ~0.14% X_0 for the beam pipe

Read-out speed
O(1-10 µs)

Power consumption
~< 50mW/cm²

Fast read-out & low Power architectures

Cooling
Stiffness / Alignment

Low material detectors & supports structures

Challenge : meet the requirements all together

Challenges and goals of CPS R&D in subatomic physics

- How to improve read-out speed/time resolution ?
  - ✓ while keeping
    - a spatial resolution in the 3-5 µm range
    - a material budget per layer in O(0.1-0.2)% X_0 range
    - a controlled power consumption (50-100 mW/cm^2)
    - a controlled data flow (~10^7 – 10^8 particles/cm^2/s)

⇨ Progress of the technology

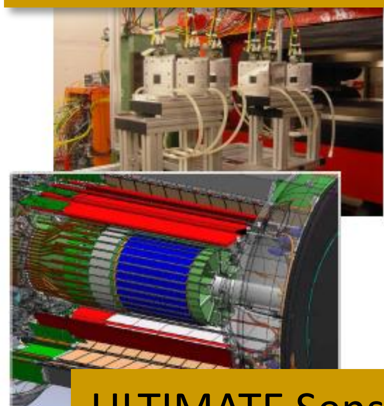
⇨ Step by step

CPS roadmap

- 1999: 1st prototype
- 2005: Full scale (M5)
- 2006: Digital output

EUDET telescope

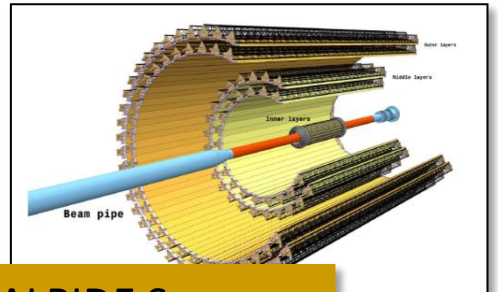
MIMOSA-26 Sensor



ULTIMATE Sensor

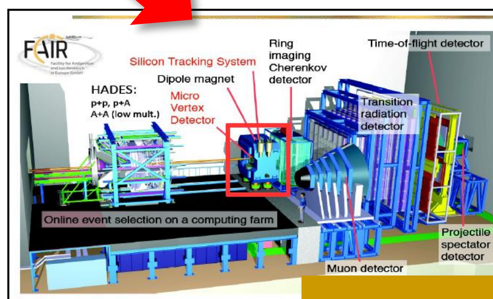
STAR-PXL

ALICE ITS upgrade



ALPIDE Sensor

CBM-MVD



MIMOSIS Sensor

ILC-VXD & SIT

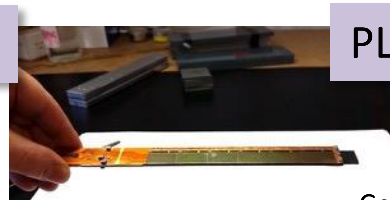
PSIRA proposal

O(100 μs) — 2010-2014

O(10 μs) — 2015-2019

O(1 μs) — > 2020-2030

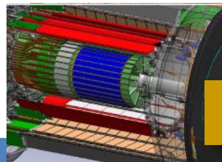
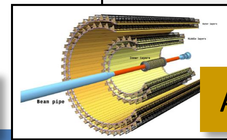
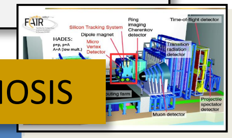
PLUME 1



PLUME 2

BEAST-2

Evolving CPS

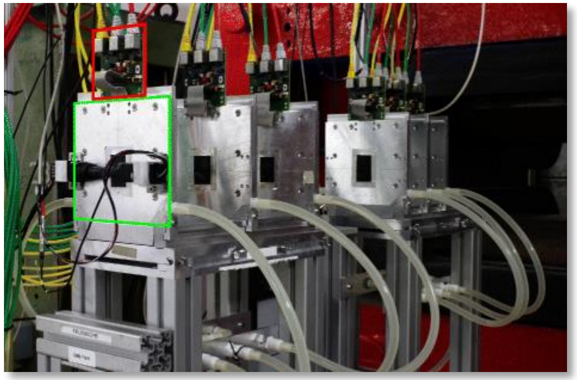

	ULTIMATE STAR-PXL	ALPIDE ALICE-ITS	MIMOSIS CBM-MVD	PSIRA proposal ILD-VXD
Data taking	2014-2016	>2021-2022	>2021	>2030
Technology	AMS-opto 0.35 μm	**TJ 0.18 μm**	TJ 0.18 μm	0.18 μm (conservative) < 0.18 μm ?
	4M	HR, V_{bias} ~-6V Deep P-well	HR, Deep P-well	?
Architecture	Rolling shutter + sparsification + binary output	**Data driven** **In pixel discri.**	data driven r.o. In pixel discri.	Data driven r.o. (conservative)
Pitch (μm^2) / Sp. Res.	20.7 x 20.7 / 3.7	27 x 29 / 5	22 x 33 / <5	~ 22 / ~ 4
Time resolution (μs)	~185	**5-10**	5	**1 – 4**
Data Flow		~10^6 part/cm^2/s Peak data rate ~ 0.9 Gbits/s	peak hit rate @ 7 x 10^5 /mm^2/s **>2 Gbits/s output (20 inside chip)**	~300 Gbits/s (instantaneous) **~1-3 Gbits / s (average)**
Radiation	O(50 kRad)/year	$2x10^{12}$ n_{eq}/cm^2 300 kRad	**$3x10^{13}$ $n_{eq}/cm^2/yr$** **& 3 MRad/yr**	O(100 kRad)/year & O($1x10^{11}$ n_{eq}(1MeV)) /yr
Power (mW/cm^2)	< 150 mW/cm^2	**< 35 mW/cm^2**	< 200 mW/cm^2	~ 50-100 mW/cm^2 **+ Power Pulsing**
Surface	2 layers, 400 sensors, $360x10^6$ pixels 0.15 m^2	7 layers, $25x10^3$ sensors **> 10 m^2**	4 stations Fixed target	3 double layers 10^3 sensors ($4cm^2$) 10^9 pixels ~0.33 m^2
Mat. Budget	~ 0.39 % X_0 (1st layer)	~ 0.3% X_0 / layer		**~ 0.15-0.2 % X_0 / layer**
Remarks	1st CPS in colliding exp.	(with CERN)	Vacuum operation Elastic buffer	Evolving requirements

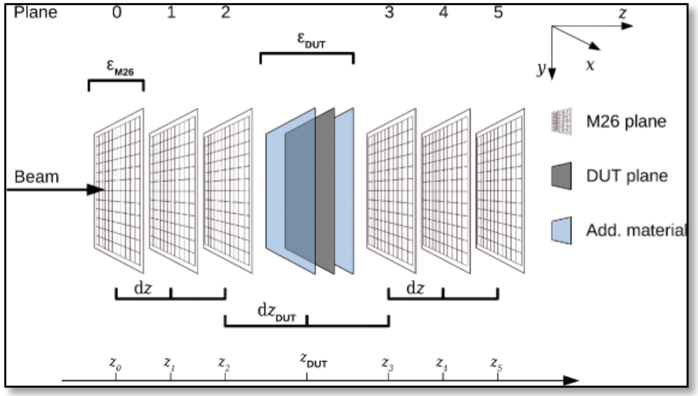
Achievements

Beam Telescopes

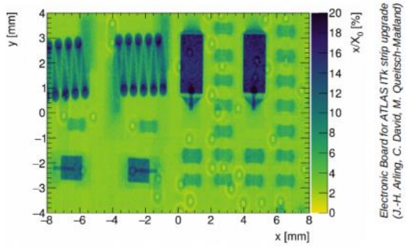
- EUDET/AIDA Telescopes (since 2010)
  - ✓ EU-FP6
  - ✓ 6 x Mimosa-26
    - 1152 x 512 pixels (10x21 mm^2)
    - Pitch = 18.4 x 18.4 μm^2
  - ✓ ~ 10 copies around the world
  - ✓ Typical Performances
    - Read-out ~115 μs
    - Pointing: ~ 1.5 μm

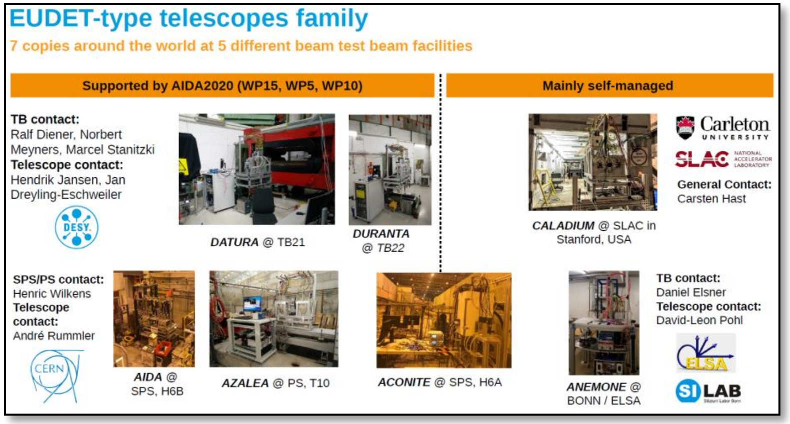
      σ_{sp} ~< 2.5 μm with 6 GeV e^-
    - tomography





H. Jansen et al https://doi.org/10.1140/epjti/s40485-016-0033-2



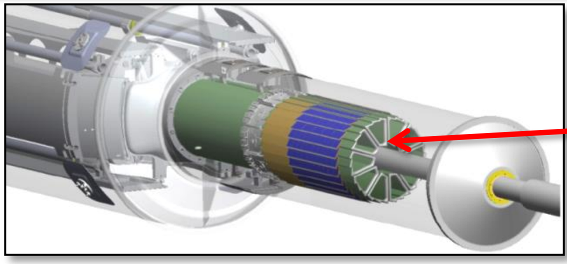


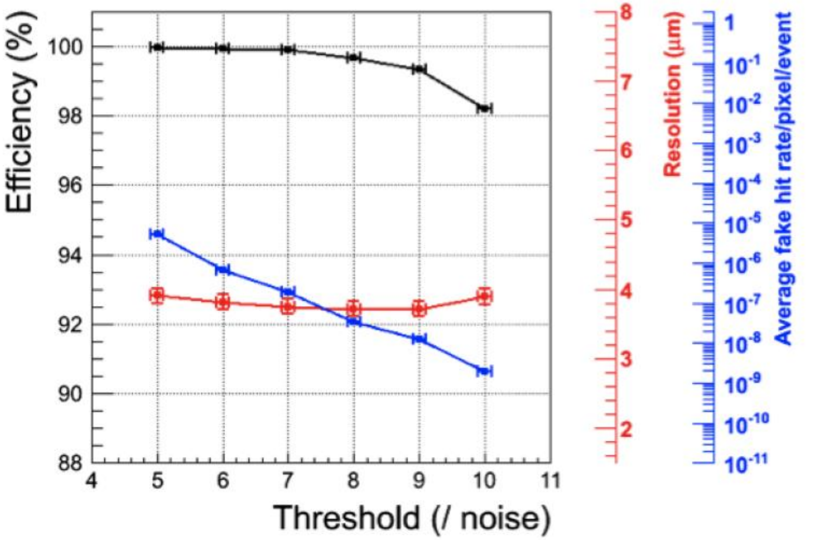
Jan Dreyling-Eschweiler,
Status of the EUDET-type beam telescope infrastructure

- CREMLIN+ program (EU+Russia)
  - ✓ DESY, CERN, JINR, FAIR, BINP, KINR, Frankfurt, IPHC
  - ✓ Telescope with MIMOSIS 1 or 2
    - Double sided ladders
    - faster read-out time 100 μs -> 5 μs.

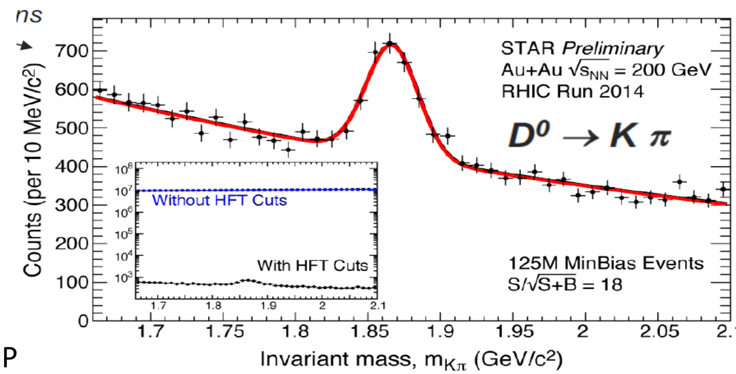
Past: STAR Heavy Flavor Tracker

- STAR-HFT @ RHIC
  - ✓ Ultimate sensor (Mimosa-28)
    - AMS CMOS 0.35 µm
    - 20.7 µm pitch
    - ~185 µs r.-o. speed,
    - 0.37 % X_0/layer
    - 2 layers, 400 sensors,
    - 360×10^6 pixels
    - 0.15 m^2
  - ✓ Architecture
    - Rolling shutter read-out
    - sparsification
    - binary output



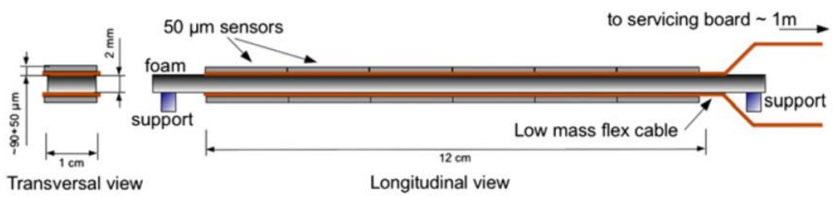


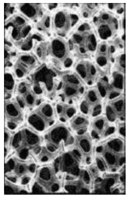
➪ 3 years of successful data taking for physics (2014-2016)
➪ PXL meets the requirements (σ_{IP}, eff., etc.)
➪ STAR: most sensitive HI experiment to charm tagging

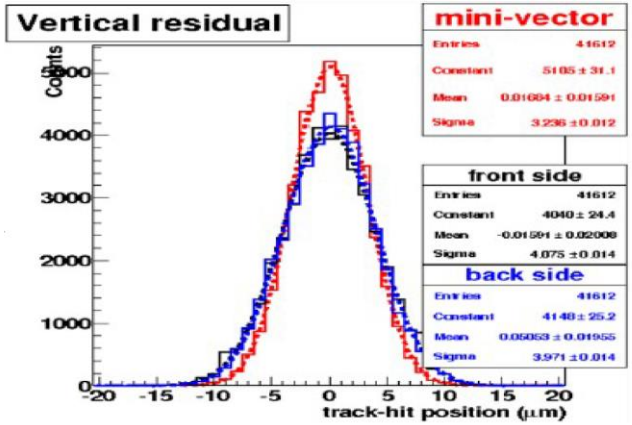


Recent Past: Integration with PLUME

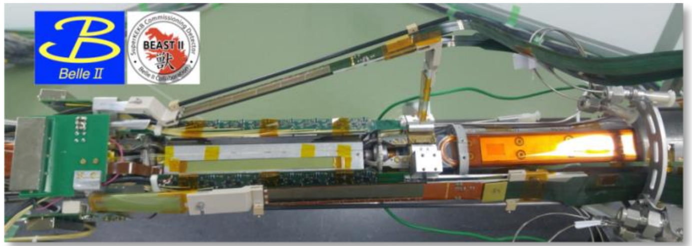
- PLUME collaboration (Bristol, DESY, IPHC)
  - ✓ Double sided ladders (12xMi26) with minimized material budget







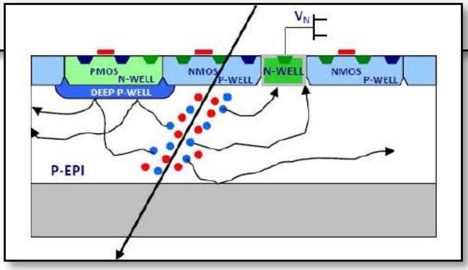
  - ✓ Mat. Budget
    - Cu(0.42%)/Al(0.35%) X_0 flex cable
- Output
  - ✓ No major issue
  - ✓ 0.3 % X_0 reachable
- Application in BEAST for Belle-2 (2018)
  - ✓ Machine commissionning & beam parameters opt.
    - Identify different background sources
  - ✓ Check rad. safety for VXD before BelleII
  - ✓ Ran continuously March-July 2018



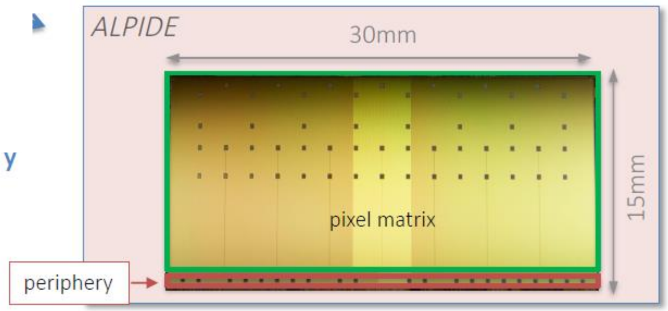
Know-how acquired ⇨ Ladders close to ILC mat.budget specifications

Present and short term

Present: ALICE ITS Upgrade

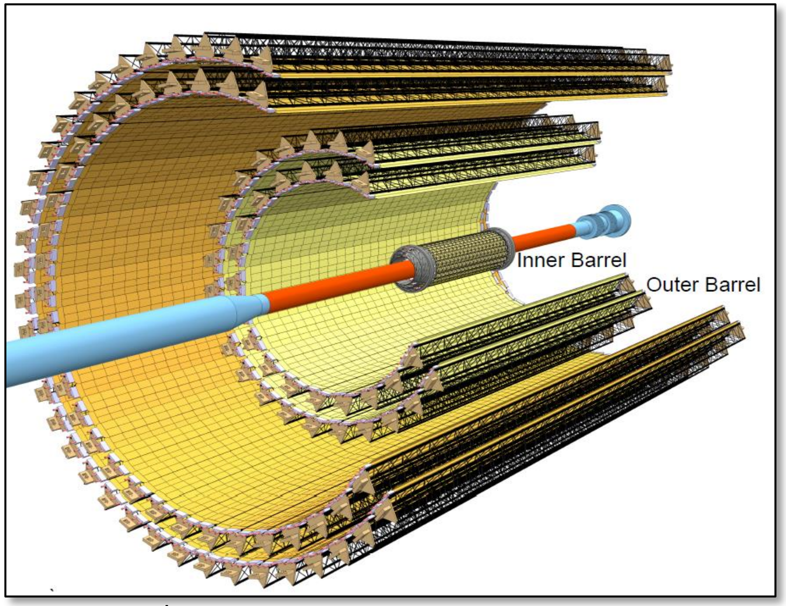


- Technology
  - ✓ 0.18 µm deep P-well (⇨PMOS transist)
    - Allows more functionnalities
- Alpide (CERN & IPHC)
  - ✓ Data driven read-out
  - ✓ Substrate reverse bias (depletion)



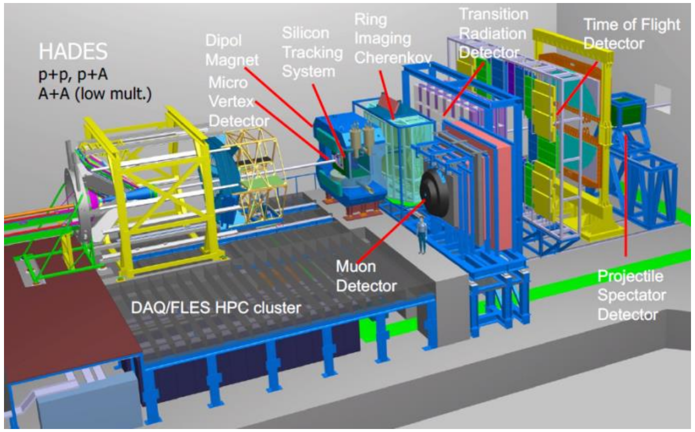
- Requirements & Design
  - ✓ Pitch = 27x29 µm^2 ⇨ σ_{sp} ~< 5 µm ;
  - ✓ Time resolution ~ 5 µs
  - ✓ Mat.budget ~ 0.3% X_0 / layer
  - ✓ 7 layers, > 10 m^2, 25x10^3 chips
  - ✓ Power < 50 mW/cm^2
  - ✓ Peak data rate ~ 0.9 Gbits/s
  - ✓ σ_{sp} ~< 5 µm ; ~ 0.3% X_0 / layer
  - ✓ 7 layers, > 10 m^2, 25x10^3 chips

⇨ 10 m^2 detector in 0.18 µm technology

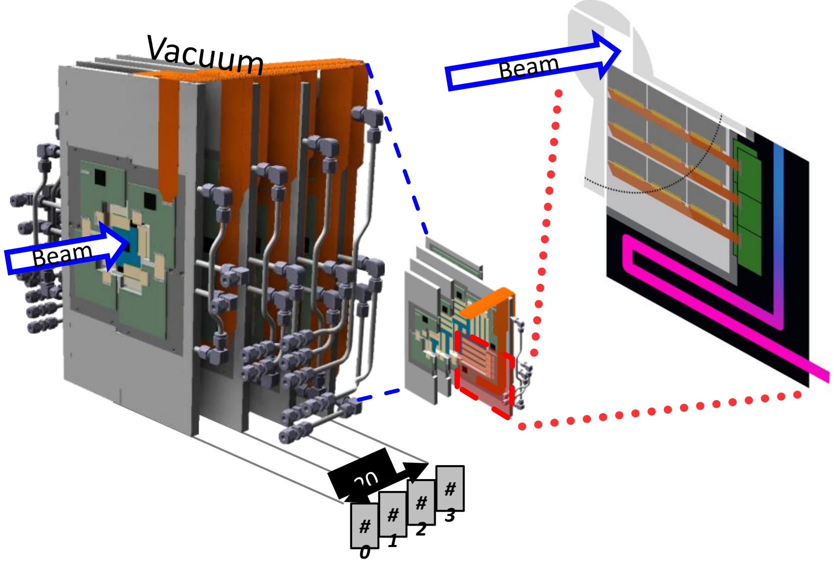


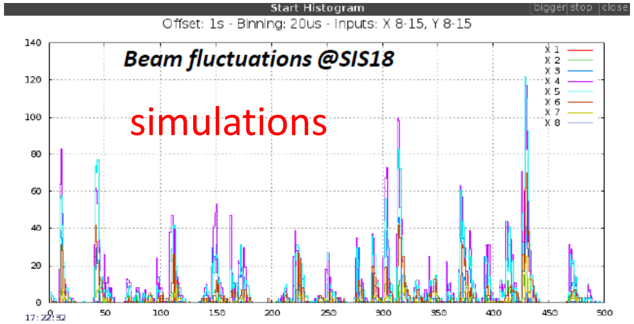
CBM-MVD @ FAIR

(IPHC and IKF)



Joachim Stroth | 56th Winter Meeting on Nuclear Physics | Bormio (Italy)

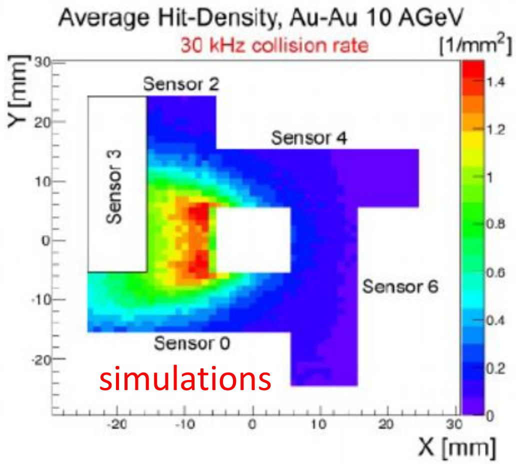




Michal Koziel| deutsche physikalische gesellschaft 2017| Münster (Germany)

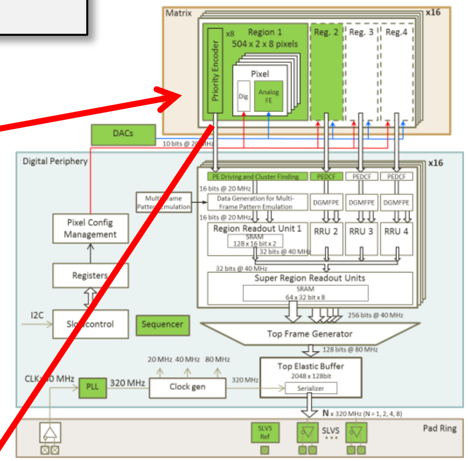
Au/Au 10 AGeV 100kHz

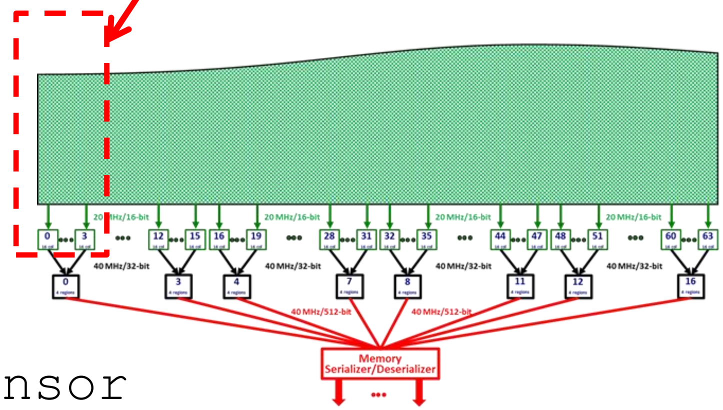
Non uniform hit density in time and space

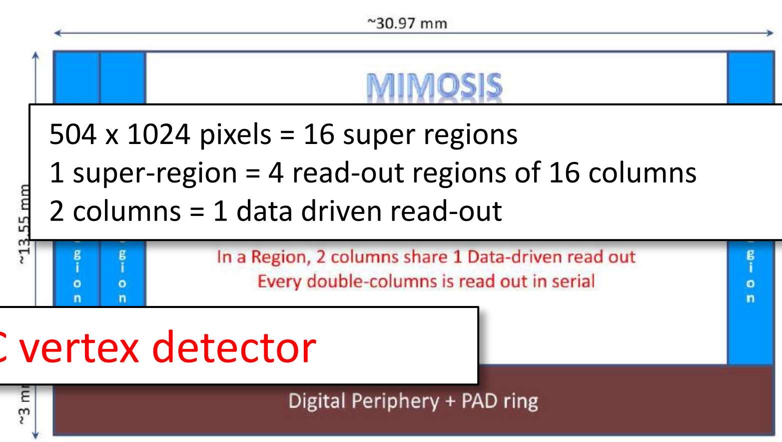


MIMOSIS roadmap

- 4 prototypes:
- MIMOSIS-0: = 2 regions
  - ✓ Test in progress
    - Priority encoder
    - Radiation hardness design (SEU)
    - Testability
- MIMOSIS-1:
  - ✓ 1st prototype of complete sensor
  - ✓ (2019)
- MIMOSIS-2:
  - ✓ (2020)
- MIMOSIS-3: final pre-production sensor
  - ✓ (≥~2020)







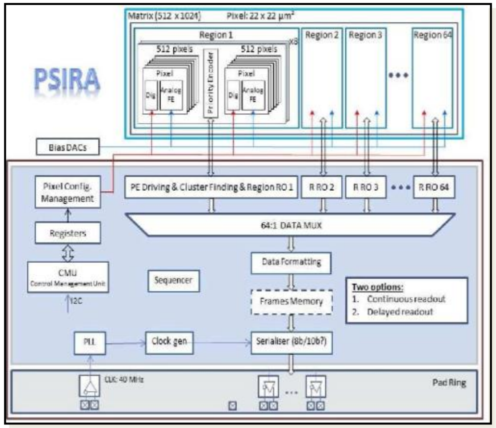
⇨ architecture adaptable to a fast sensor for an ILC vertex detector

Future & Perspectives

Extension of MIMOSIS to ILC vertexing and tracking

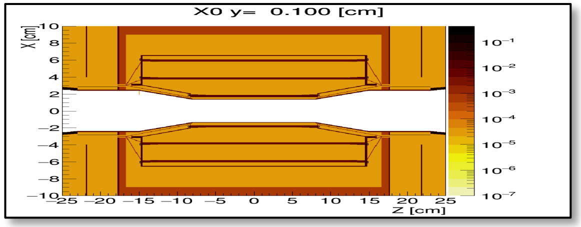
- Conservative approach
  - ✓ Minimize changes w.r.t. MIMOSIS
    - ▪ Keep TJ 0.18 µm technology & a similar architecture
  - ✓ 2 sub-systems targeted
    - ▪ Vertex detector & Silicon inner trackers (SIT @ ILD)

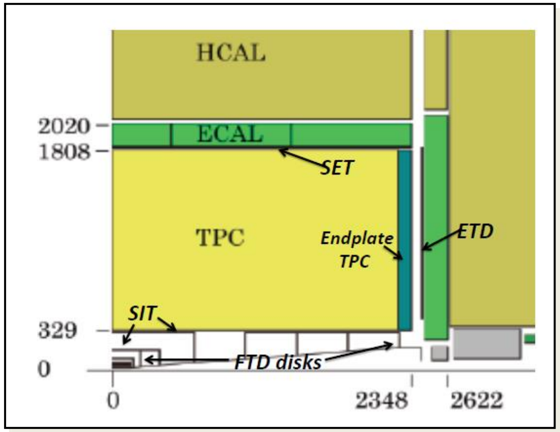
⇨ PSIRA



⇨ Finalize CPS ~2025

- Expected Performances
  - ✓ σ_{sp} ~4 µm ⇨Use double sided ⇨ σ_{sp} ~2.8 µm
    - ▪ 22x22 µm^2 ~ 20% better spatial resolution w.r.t. ALPIDE (vertexing)
    - ▪ Faster = higher Power consumption
  - ✓ Read-out time: 2-4 µs (ILD-VXD) and 1 µs (ILD-SIT)
  - ✓ Sustainable occupancy
    - ~ 100 hits/cm^2/µs



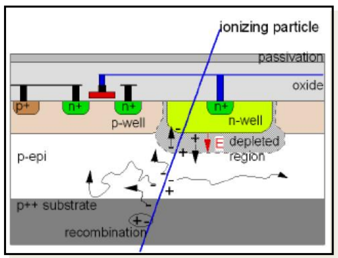


⇨ PSIRA architecture already reaching 4-8 BX read-out time
⇨ Power vs read-out speed compromise
⇨ Avoiding power pulsing possible ?

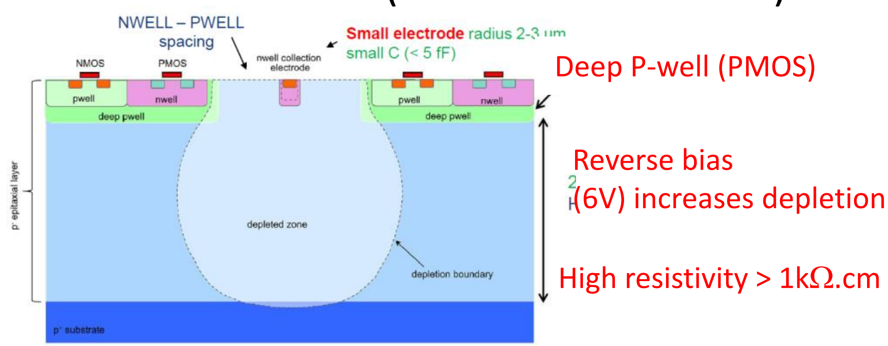
CPS: an evolving technology

- TJ 0.18um process
  - ✓ Smaller feature size, adapted epitaxial layer

Classical CMOS



State of the art (ALPIDE & MIMOSIS)

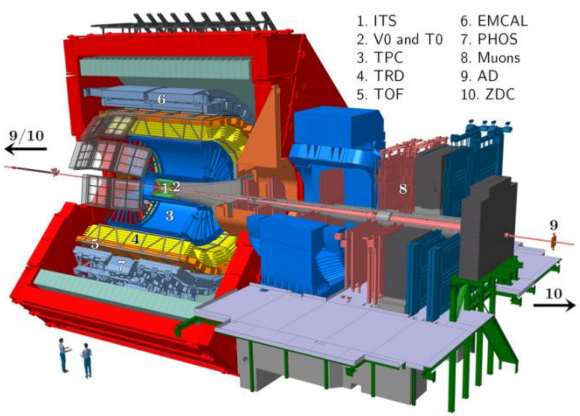


- Explore smaller feature sizes 180 nm ⇨110 nm or even 65 nm.
  - ✓ Motivations
    - Smaller pixel dimensions & faster read-out
    - Reduced power consumption
- Long term R&D (with CERN)
  - ✓ Stitching -> reduce ladder overlap / reduce space between sensors
    - ~150 µm to ~<50 µm
  - ✓ Synergy with ALICE plans
  - ✓ 65 nm technology exploration
    - Mixed CMOS processes

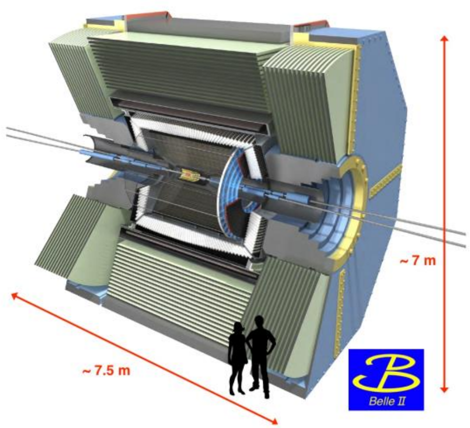
⇨ Smaller feature size offers opportunities to get closer to 1 µs r.o. time

Perspectives from other groups @ IPHC

ALICE

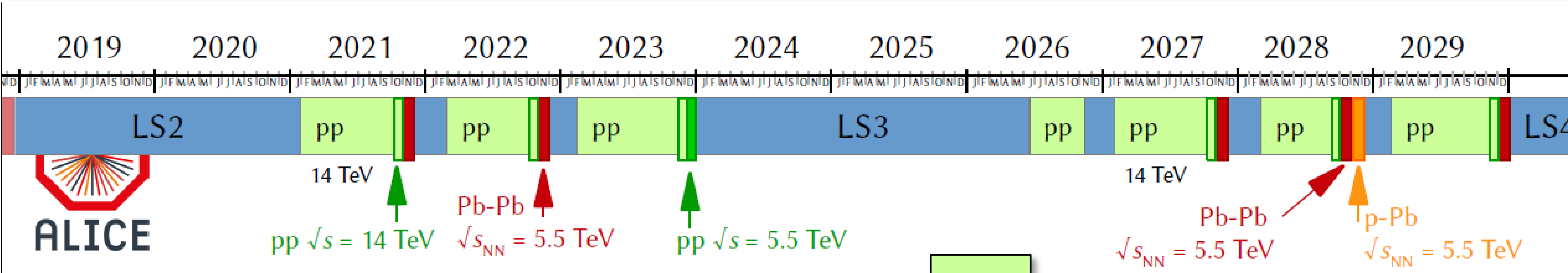


Belle-2

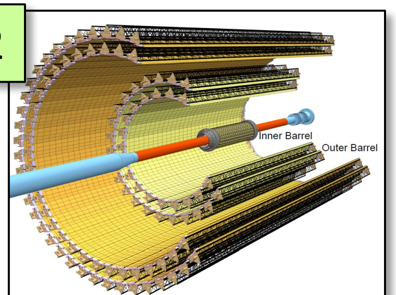


⇨ More materials in backup slides

Alice perspectives

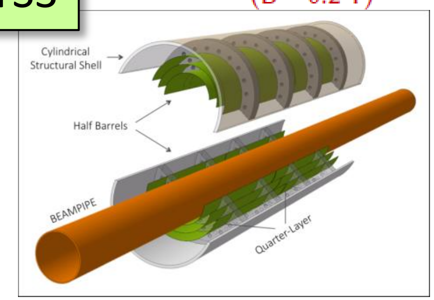


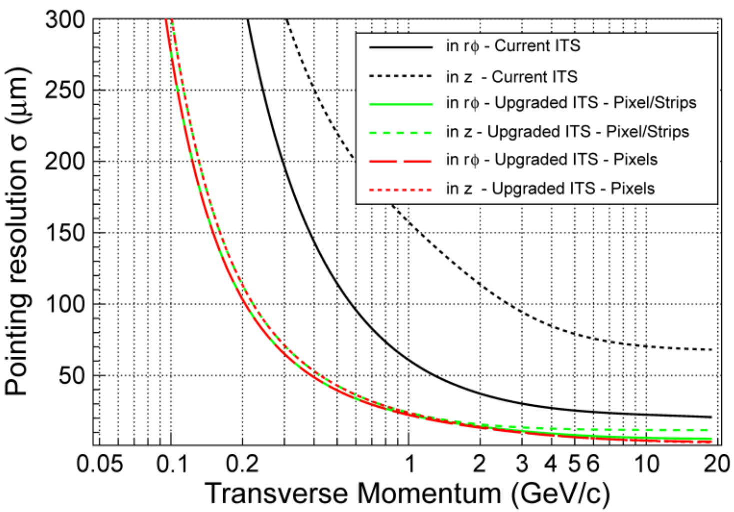
ITS1 LS2 ITS2



LS3

ITS3



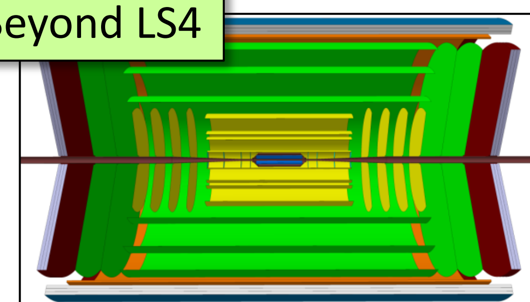


Pointing resolution significantly improved

- Factor 3 in rϕ-plane
- Factor 5 along z axis

LS4

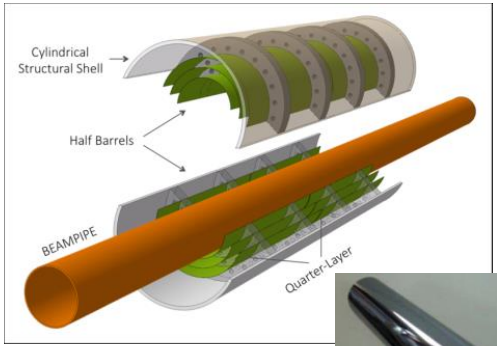
Beyond LS4

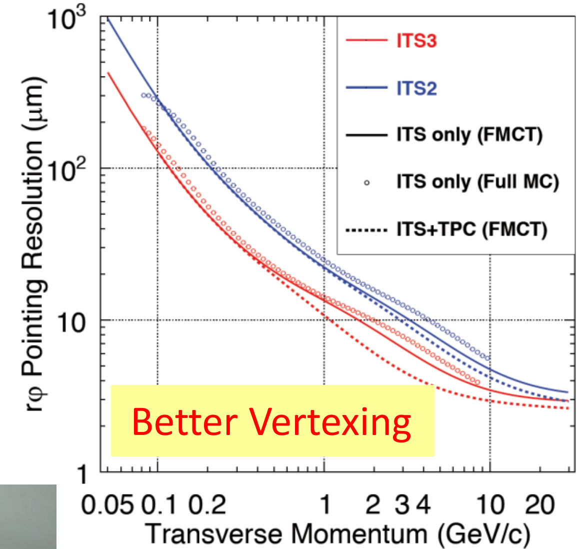


HI Experiment at LHC "All-Silicon"

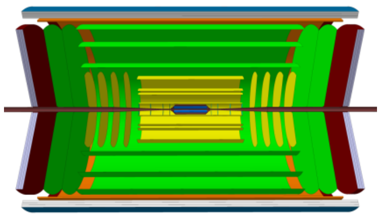
ITS3 & beyond LS4

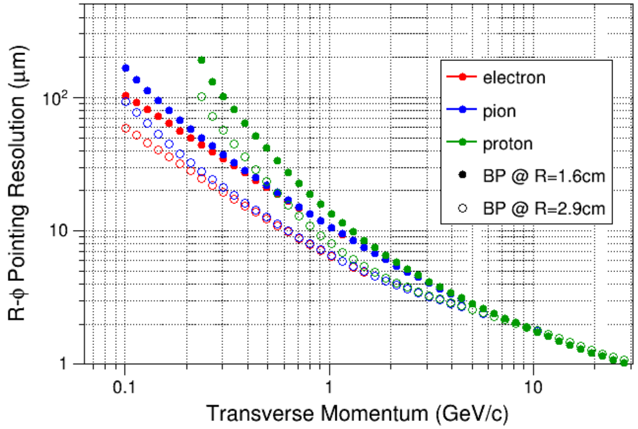
- ITS3 — Expression of Interest ALICE-UG-2018-01
  - ✓ Replacement of ITS 2 inner barrel by 3 layers of very thin CMOS sensors
    - Extension to lower pT's
    - R=18/24/30 mm
  - ✓ Expected performances
    - Factor 2 in pT
    - Factor 4 in significance





- Beyond LS4 — [arXiv:1902.01211]
  - ✓ Tracker: ~ 10 layers based on CPS
    - Spatial resolution
      - innermost layers ~1-3 um
      - outer layers ~5 um
    - High precision time Measurement (<30 ps)





Sensor thickness: 20 – 40μm (0.03 - 0.05% X0)

Belle-2 perspectives

March-July 2018

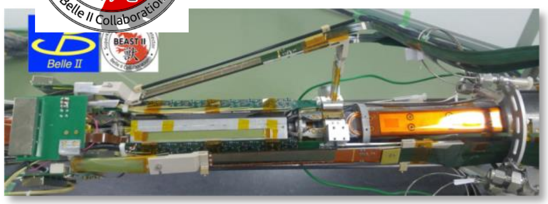
2019-2027

Phase-2

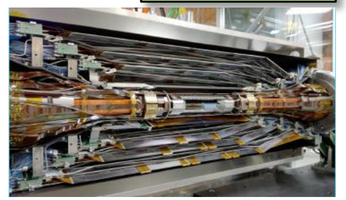
Phase-3

Upgrade

2027: L ~50 ab^{-1}

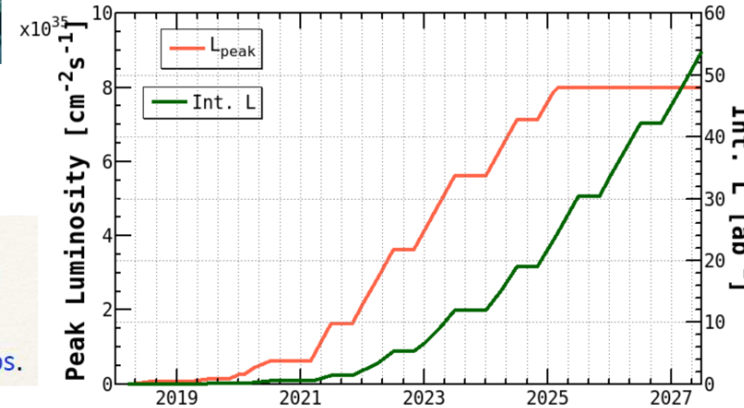


Beam background commissionning



VXD installed

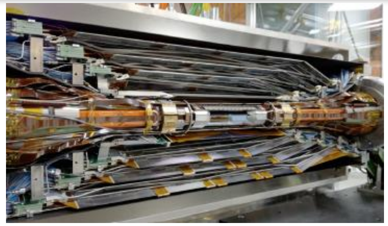
- As installed end of 2018:
  - PXD = 2 innermost layers of DEPFET pixels (only 50 % finally installed).
  - SVD = 4 layers of double-sided silicon strips.



- **Search for new physics in Belle II:**
  - Measurements with unprecedented precision with B, D and τ:
    CP violation, V-A coupling, charged lepton flavour violation, lepton universality (see current observation of flavour anomalies), ...
    Current observation of flavour anomalies: lepton universality?
  - Currently based on **50 ab^{-1}** delivered thanks to **8×10^{35} cm^{-2} s^{-1}**.
  - SuperKEKB e^+e^- collisions at the intensity frontier: only collider until at least 2030 with complementary program to LHC.

Belle-2 Possible upgrade vertex detector

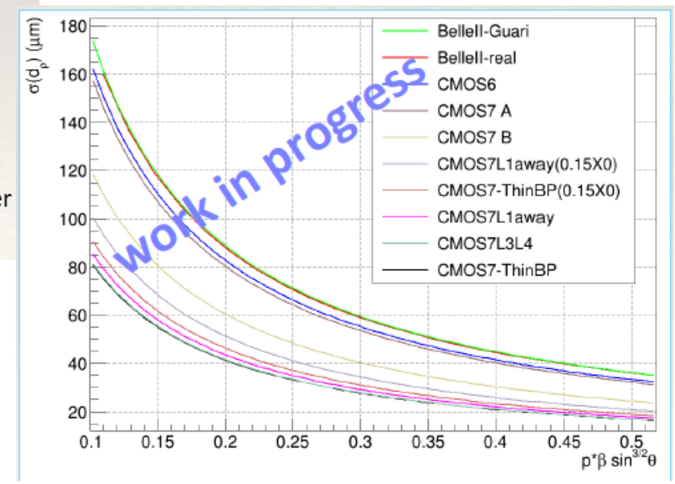
- Detector occupancy dominated by beam induced background.
- Success of the physics program relies on the control of beam induced background.
- Studies started for a machine upgrade to **increase luminosity by a factor of 5 (peak & int.).** Timescale not precisely defined.



- Performances measured during Belle II commissioning in March-July 2018:
  - Extrapolation to design luminosity of BEAST measurements: SVD (PXD) occupancy rates ~1% (3%).

    ➛ Detector operation and tracking performance issues:
    Upgrade shall target ‰ occupancy level to cope with 10^6 to 10^8 hits cm^{-2} s^{-1} (at upgrade lumi.).

- **Possible upgraded vertex detector,**
  according to on-going discussion between Belle II and Micro-electronics @IPHC:
  - Fully pixelated vertex detector with following specs.:
    - faster integration time < 1 μs,
    - low material budget 0.1% (inner) - 0.3% (outer) of X_0 /measurement point,
    - $\sigma_{s.p.}$ = 5-10 μm, not critical.
  - **Based on MIMOSIS (CBM)** with modification of digital parts for triggering (in common with other solutions), and synergy with on-going ALICE R&D for very thin layers



- **New vertex det. geometry & sensor specs.:**
  - Seed Money EUCOR project with KIT, 2019-20.
  - Optimisation of an upgraded vertex detector design.

Summary

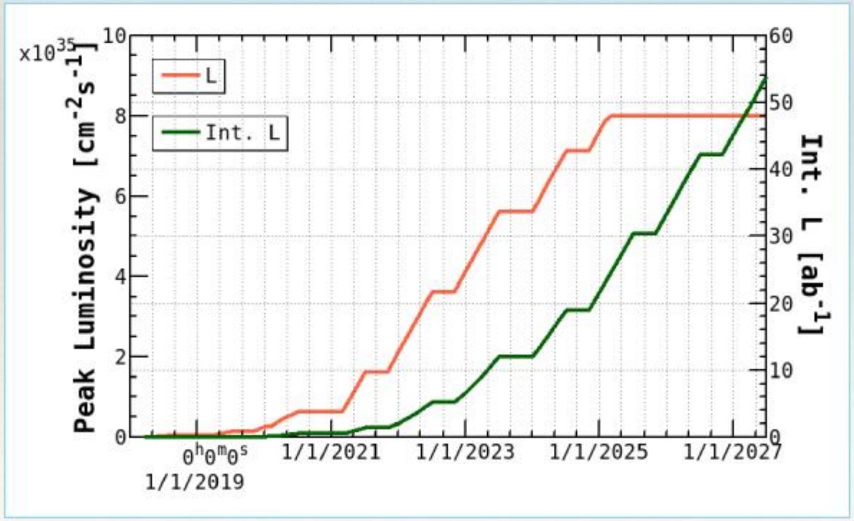
- Not covered
  - ✓ CEPC, LHC-B
- CPS in subatomic physics
  - ✓ Tends to become the standard technology when resolution and material budget are the key factor
  - ✓ The potential of the technology is far from being fully exploited
  - ✓ CPS will continue to benefit from progress of foundries/industry
- Time scale
  - ✓ Fabricating a dedicated sensor for a given application is a long process
  - ✓ Exploit synergies whenever possible

Back up

Belle II physics program

- **Search for new physics in Belle II:**
  - Measurements with unprecedented precision with B, D and τ:
    CP violation, V-A coupling, charged lepton flavour violation, lepton universality (see current observation of flavour anomalies), ...
    Current observation of flavour anomalies: lepton universality?
  - Currently based on **50 ab^{-1}** delivered thanks to **8×10^{35} cm^{-2} s^{-1}**.
  - SuperKEKB e^+e^- collisions at the intensity frontier: only collider until at least 2030 with complementary program to LHC.

- **Luminosity profile and nano-beam induced background:**
  - Detector occupancy dominated by beam induced background.
  - Success of the physics program relies on the control of beam induced background.
  - Studies started for a machine upgrade to **increase luminosity by a factor of 5 (peak & int.).** Timescale not precisely defined.



1

Belle II vertex detector upgrade

- **Current vertex detector:**
  - As installed end of 2018:
    - PXD = 2 innermost layers of DEPFET pixels (only 50 % finally installed).
    - SVD = 4 layers of double-sided silicon strips.

  - Performances measured during Belle II commissioning in March-July 2018:
    - Extrapolation to design luminosity of BEAST measurements: SVD (PXD) occupancy rates ~1% (3%).

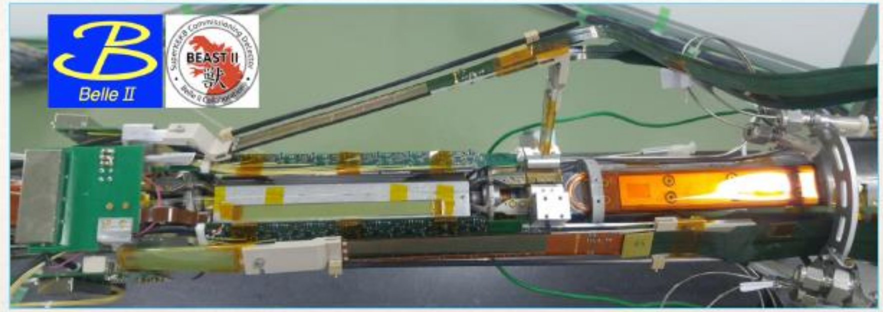
      ➝ Detector operation and tracking performance issues:
      Upgrade shall target ‰ occupancy level to cope with 10^6 to 10^8 hits cm^{-2} s^{-1} (at upgrade lumi.).

- **Possible upgraded vertex detector,**
  according to on-going discussion between Belle II and Micro-electronics @IPHC:
  - Fully pixelated vertex detector with following specs.:
    - faster integration time < 1 µs,
    - low material budget 0.1% (inner) - 0.3% (outer) of X_0 /measurement point,
    - $\sigma_{s.p.}$ = 5-10 µm, not critical.
  - **Based on MIMOSIS (CBM)** with modification of digital parts for triggering (in common with other solutions), and synergy with on-going ALICE R&D for very thin layers

2

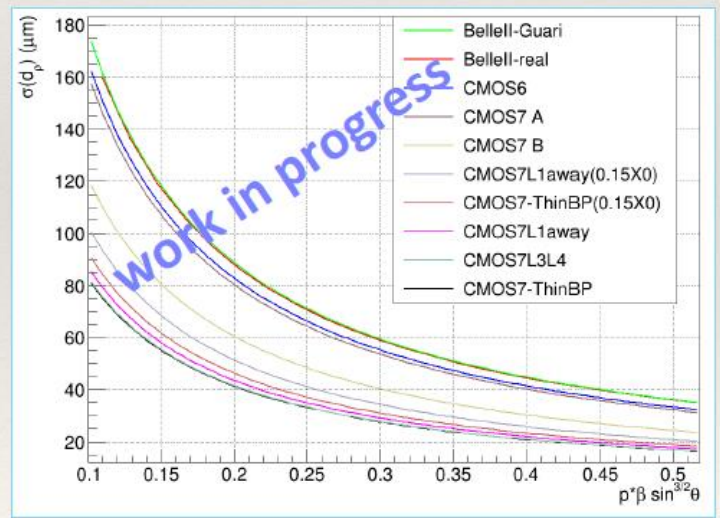
Belle II-IPHC activities in view of an upgrade

- **Evaluation on nano-beam induced background:**
  - IN2P3 & IdEX BEAST project, 2014-18.
  - Design, construction and integration of:
    - System of 2 PLUME ladders in Belle II vertex detector volume.
    - $16{\times}10^6$ channel-detector, cooling, mechanical support, DAQ.
  - Assess added value of double-sided pixel layers.
  - First CMOS sensor in an e^+e^- collider experiment.



- **New vertex det. geometry & sensor specs.:**
  - Seed Money EUCOR project with KIT, 2019-20.
  - Optimisation of an upgraded vertex detector design.

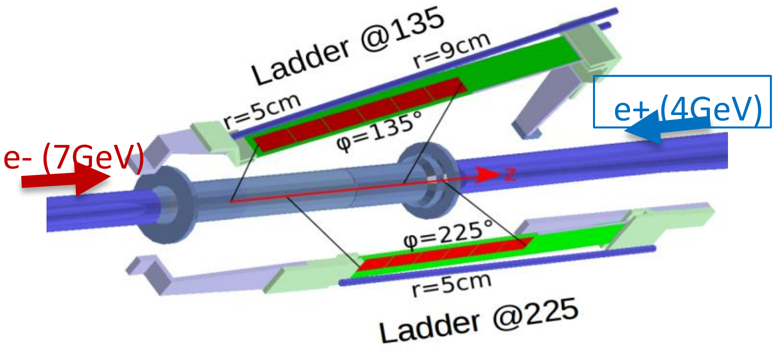
Illustration: transverse Impact Parameter resolution as a function of momentum, for various detector geometries & sensor specs.:



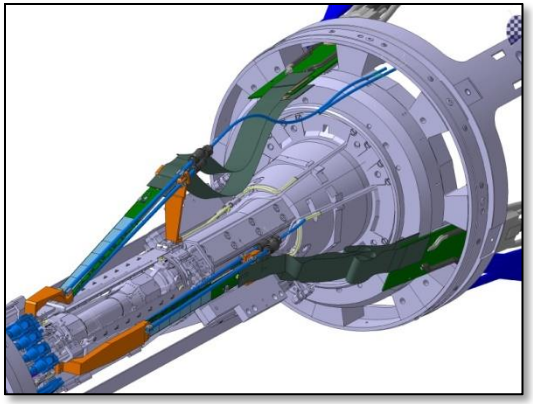
3

PLUME ladders at BEAST-2 for superKEKB

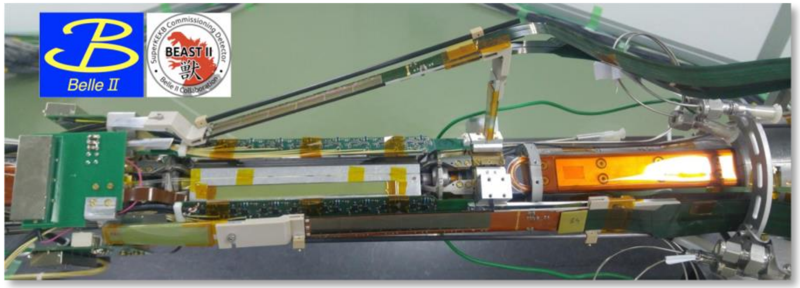
- Motivations
  - ✓ Machine commissionning & beam parameters optimization
  - ✓ Check rad. safety for VXD before BelleII
  - ✓ Identify different sources
    - Touschek, synchrotron, beam gas, injection,
    - bhabha, 2 photons, etc.



- Beast II installed in the VXD volume
  - ✓ 2 PLUME ladders & other radiation monitors



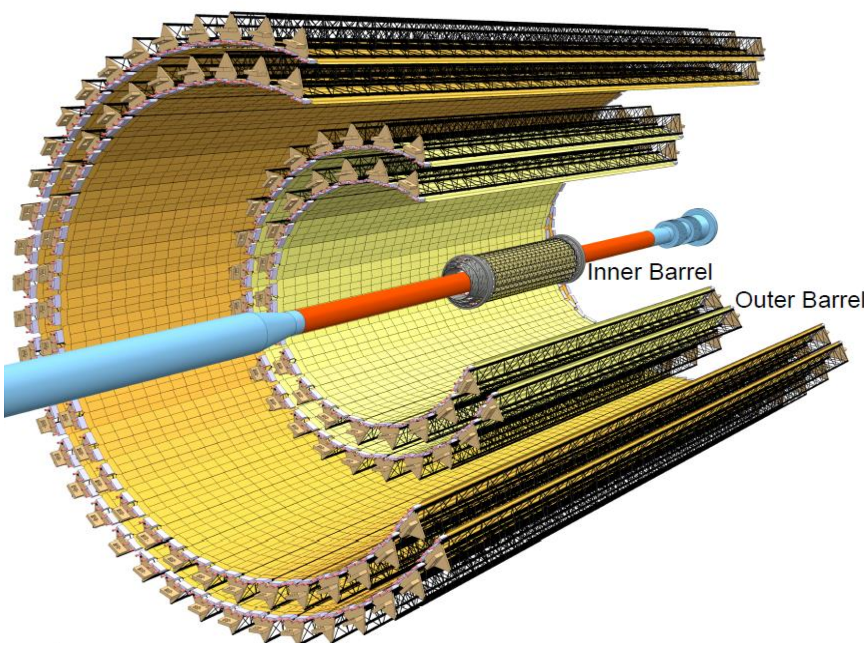
- Running conditions
  - ✓ Continuous running from March 16th to July 17th 2018
  - ✓ Luminosity
    - Peak L ~ 5.5×10^{33} cm^{-2}.s^{-1}
    - Total L ~ 500 pb^{-1} (Belle II detector)
  - ✓ Data
    - 16 Mpixels / 115 µs / sparse read-out
    - Analysis on going

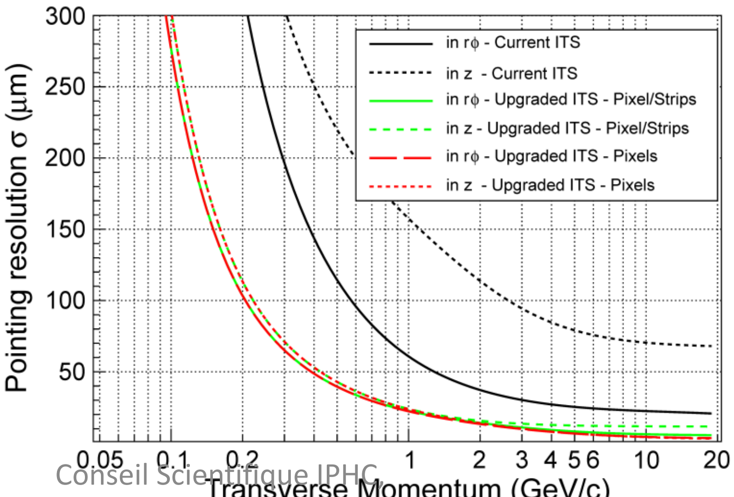


ITS UPGRADES

ITS 2 beyond LS2

Assembly and commissioning phase





Pointing resolution significantly improved

- Factor 3 in rϕ-plane
- Factor 5 along z axis

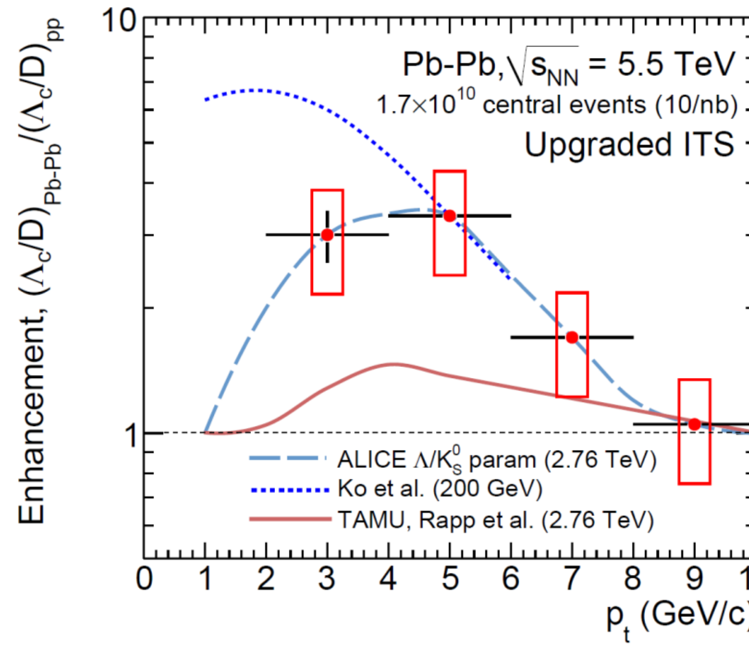
Physics Goals

Measurements of heavy flavor mesons with a higher significance and access to heavy flavor baryons

-> Transport properties of the Quark-Gluon Plasma

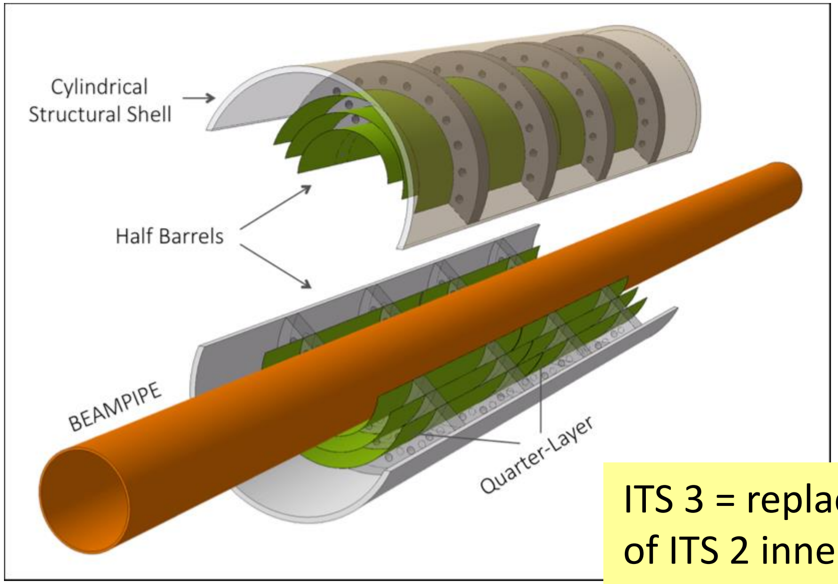
-> Partonic thermalization

-> QGP hadronization mechanisms

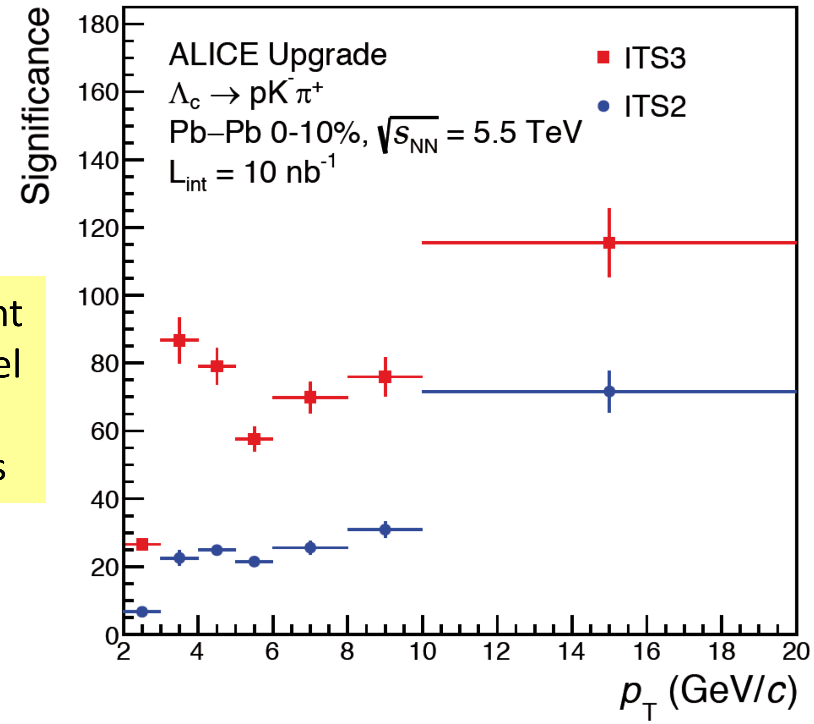


$\Lambda_c \rightarrow p\,K\,\pi$ measurement accessible with the ALICE upgrade and 10 nb^{-1}

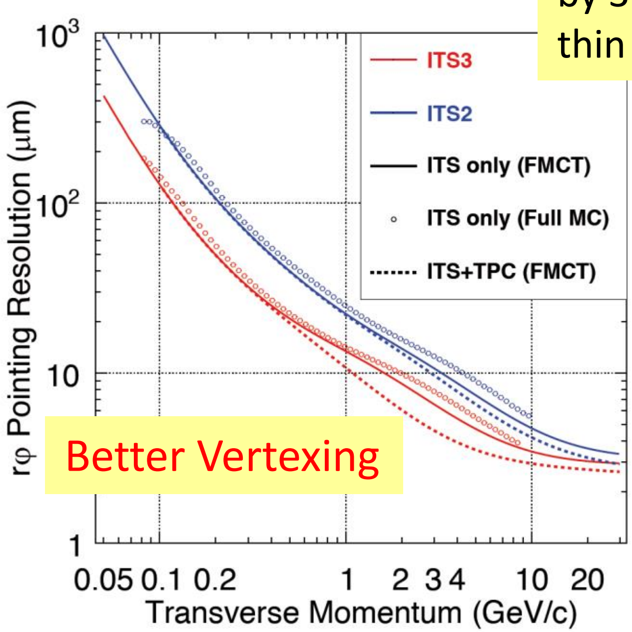
ITS 3 beyond LS3



Improvement of heavy flavor baryon measurements
Extension to lower pT's
From ITS 2 to ITS 3 : S/B x 10 , significance x 4



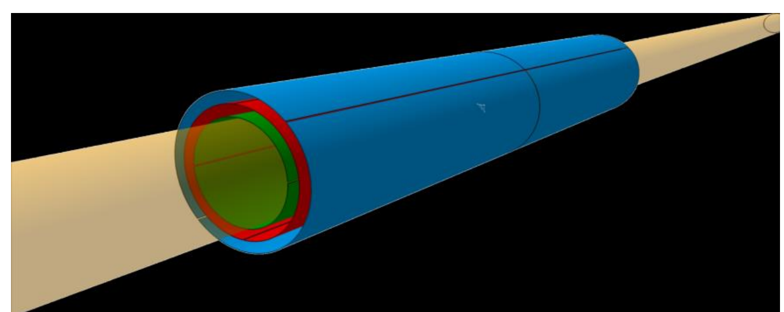
ITS 3 = replacement of ITS 2 inner barrel by 3 layers of very thin CMOS sensors



Better Vertexing

Improvement of ≈ factor 2 at all pT's

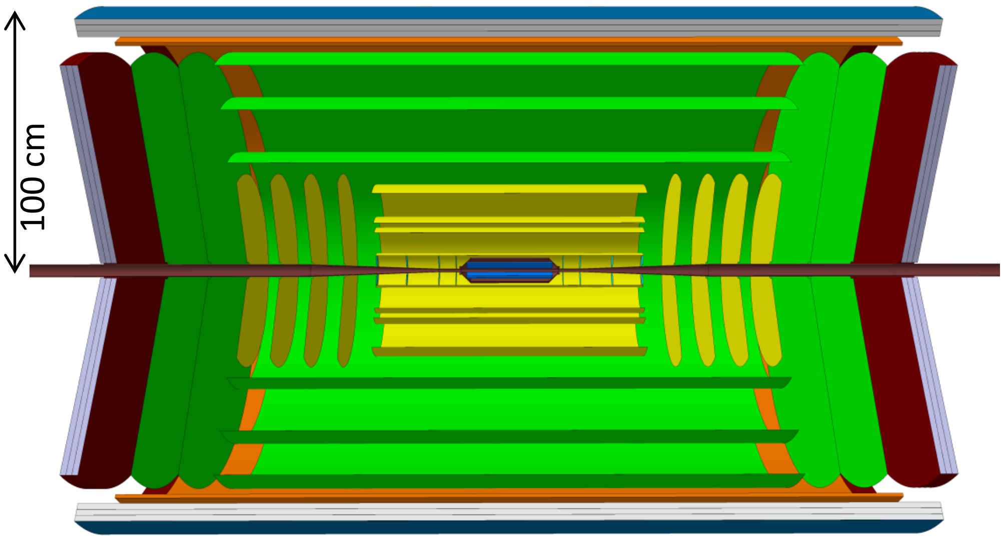
Pipe: r ≈ 16mm L0: r ≈ 18mm L1: r ≈ 24mm L2: r ≈ 30 mm



Sensor thickness: 20 – 40μm (0.03 - 0.05% X0)

Next Generation HI Experiment at LHC
An “All-Silicon” Detector beyond LS4

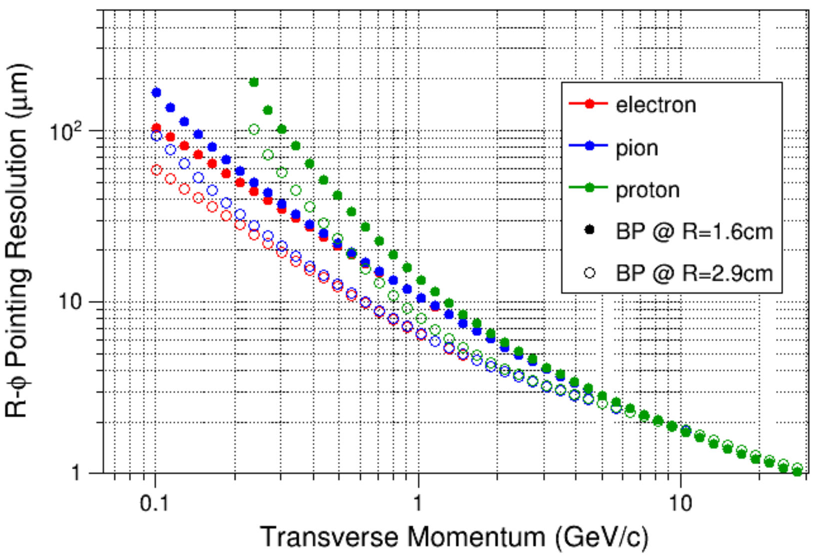
arXiv:1902.01211
[physics.ins-det]



Tracker: ~10 tracking barrel layers based on CMOS sensors
Hadron ID: TOF with outer silicon layers
Electron ID: pre-shower
FOCAl (-> 8 units of rapidity)

Physics Goals

Very high precision measurement of open heavy-flavors: single charmed and multiply charmed, charmed-beautiful, beautiful hadrons down to very low pT

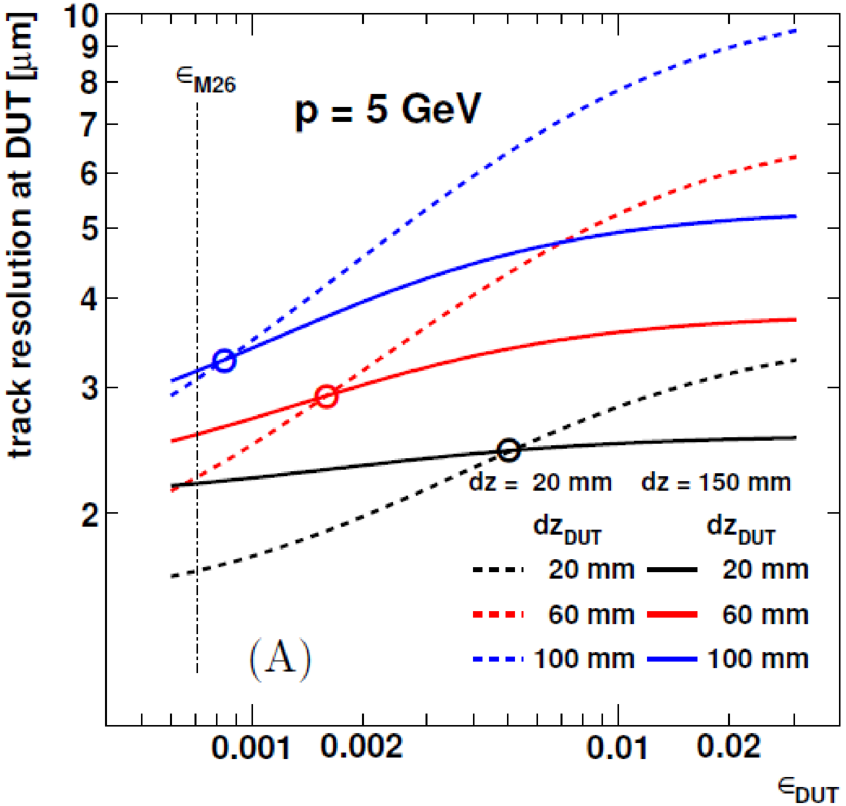


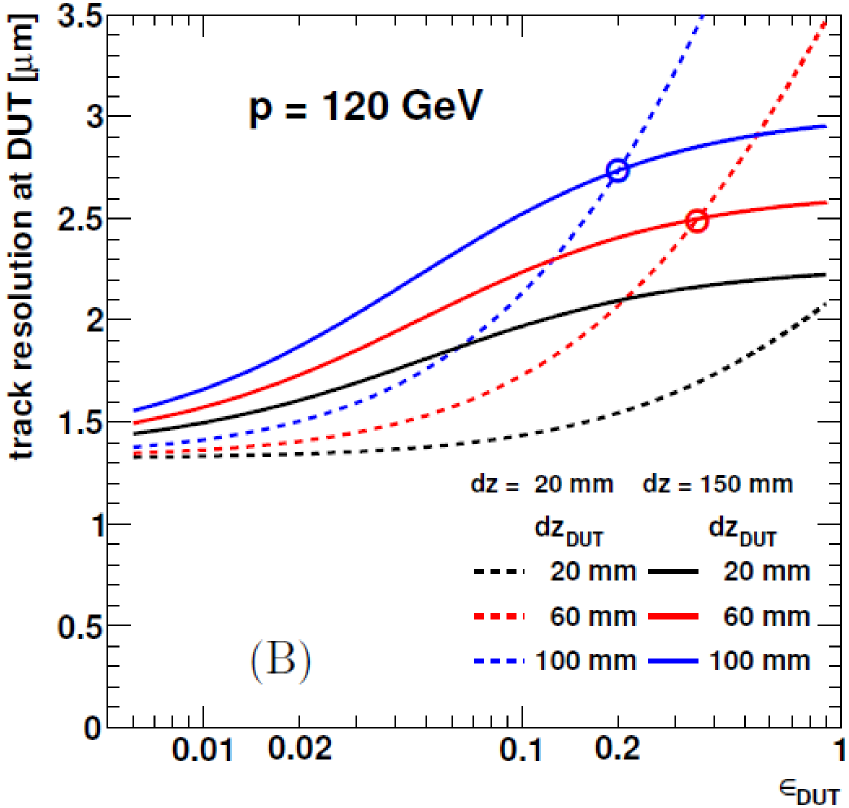
Pointing resolution (pions): ≈ 10 μm @ 1 GeV/c
<50μm @ 200 MeV/c

Spatial resolution
- Innermost 3 layers: ~ 1μm
- Outer layers: ~ 5μm

High precision time measurement in the outermost layer (< 30 ps) material

Eudet Telescope resolution





Reminder: ILD Vertex Detector requirements (DBD @ 500 GeV)

- Physics: Mat. budget and granularity

$$\sigma_b < 5 \oplus 10/p\beta \sin^{3/2}\theta \ \mu m.$$

(a & b parameters)

✓ $\sigma_{R\phi}$ ~ 3 µm (pitch ~ 17 µm)

✓ O(0.15%X_0/layer) + 0.14%X_0 (beam pipe)

- Experimental constraints

✓ Occupancy (Beam background)

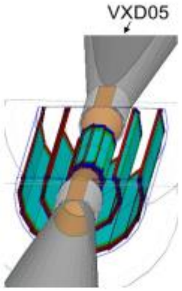
~ 5 part/cm^2/BX ⇨ few % occupancy max ?

✓ Radiation hardness :

O(100 kRad) & O($1x10^{11}$ $n_{eq\ (1MeV)}$) /yr

✓ Power dissipation :

~ 50 mW/cm^2 ⇨Power cycling, ~3% duty cycle



	R (mm)	$\lvert z\rvert$ (mm)	$\lvert\cos\theta\rvert$
Layer 1	16	62.5	0.97
Layer 2	18	62.5	0.96
Layer 3	37	125	0.96
Layer 4	39	125	0.95
Layer 5	58	125	0.91
Layer 6	60	125	0.9

Beam background

- Low momentum (10-100 MeV/c) real tracks !
- uncertainties on M.C. simulations / final geom.

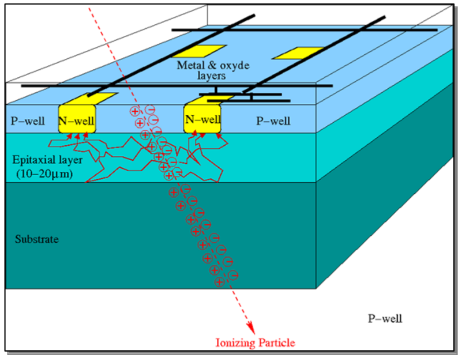
⇨ Safety factors needed (> x5)

- Vertex detector roles:
  - ⇨ b/c/τ-tagging
  - ⇨ Stand alone tracking capabilities (low pT)
  - ⇨ VTX/Jet charge determination, etc.
- Lower occupancies means
  - ⇨ Reduced combinatorial to reduce fake tracks
  - ⇨ Reduced pile-up for physics analysis

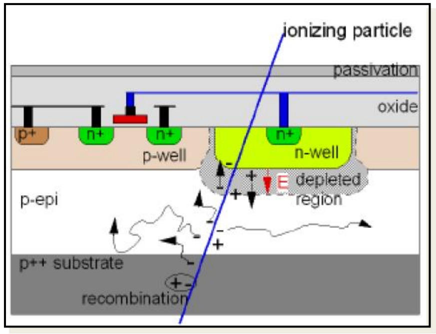
⇨ Strong motivations to get reduced occupancy / faster read-out

CMOS pixel sensor (CPS) for charged particle detection

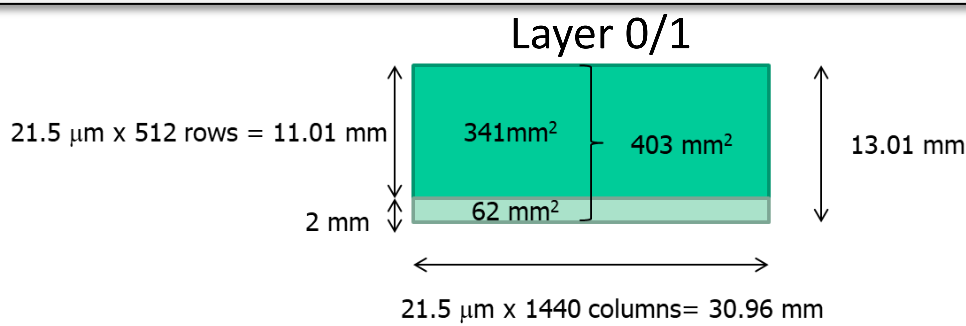
- Main features
  - ✓ Monolithic (Signal created in low doped thin epitaxial layer ~10-30 µm)
  - ✓ Thermal diffusion of e- (Limited depleted region)
  - ✓ Charge collection: N-Well diodes (Charge sharing ⇨ resolution)
  - ✓ Continuous charge collection (No dead time)

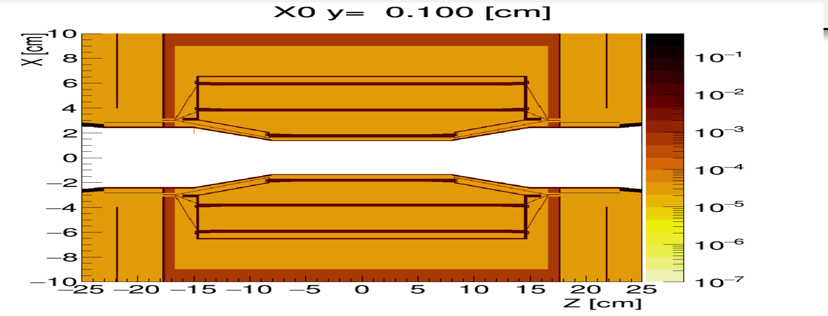


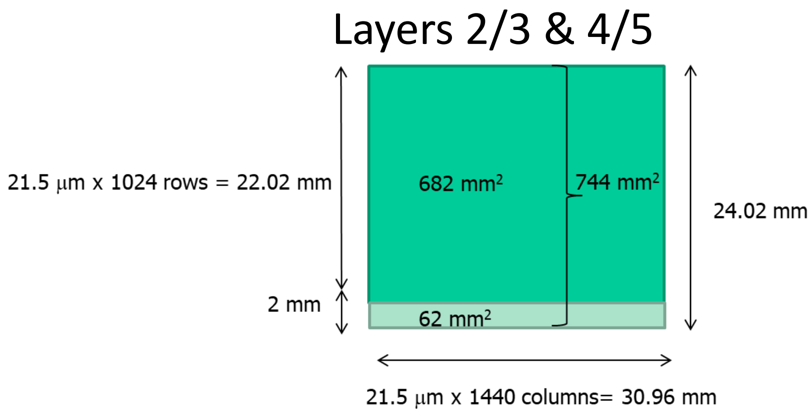
- Main advantages
  - ✓ Granularity
  - ✓ Material budget
  - ✓ Signal processing integrated in the sensor
  - ✓ Flexible running conditions (Temperature, Power, Rad. Tol.)
  - ✓ Industrial mass production
    - Advantages on costs, yields, fast evolution of the technology,
    - Possible frequent submissions
- Main limitation
  - ✓ Industry addresses applications far from HEP experiments concerns

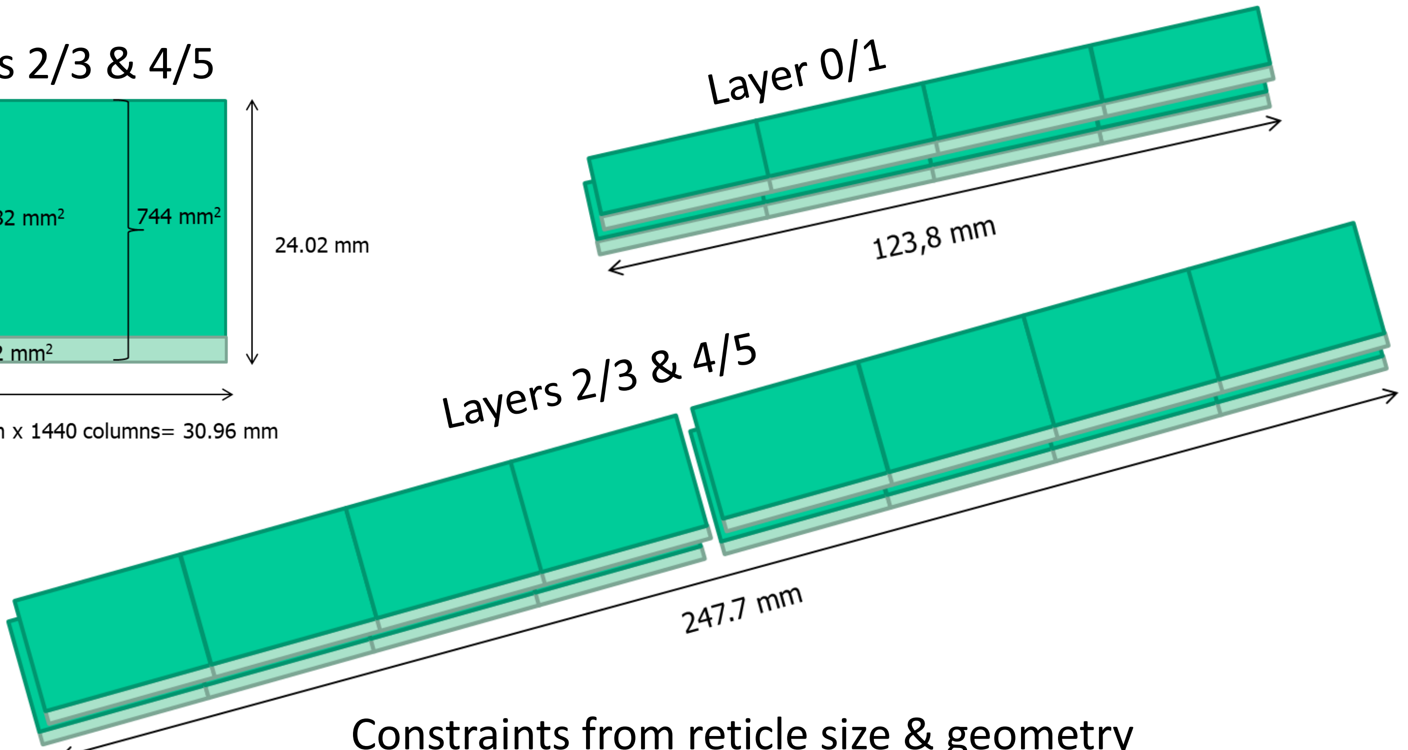


ILD: Chip dimensions & ladders









Constraints from reticle size & geometry

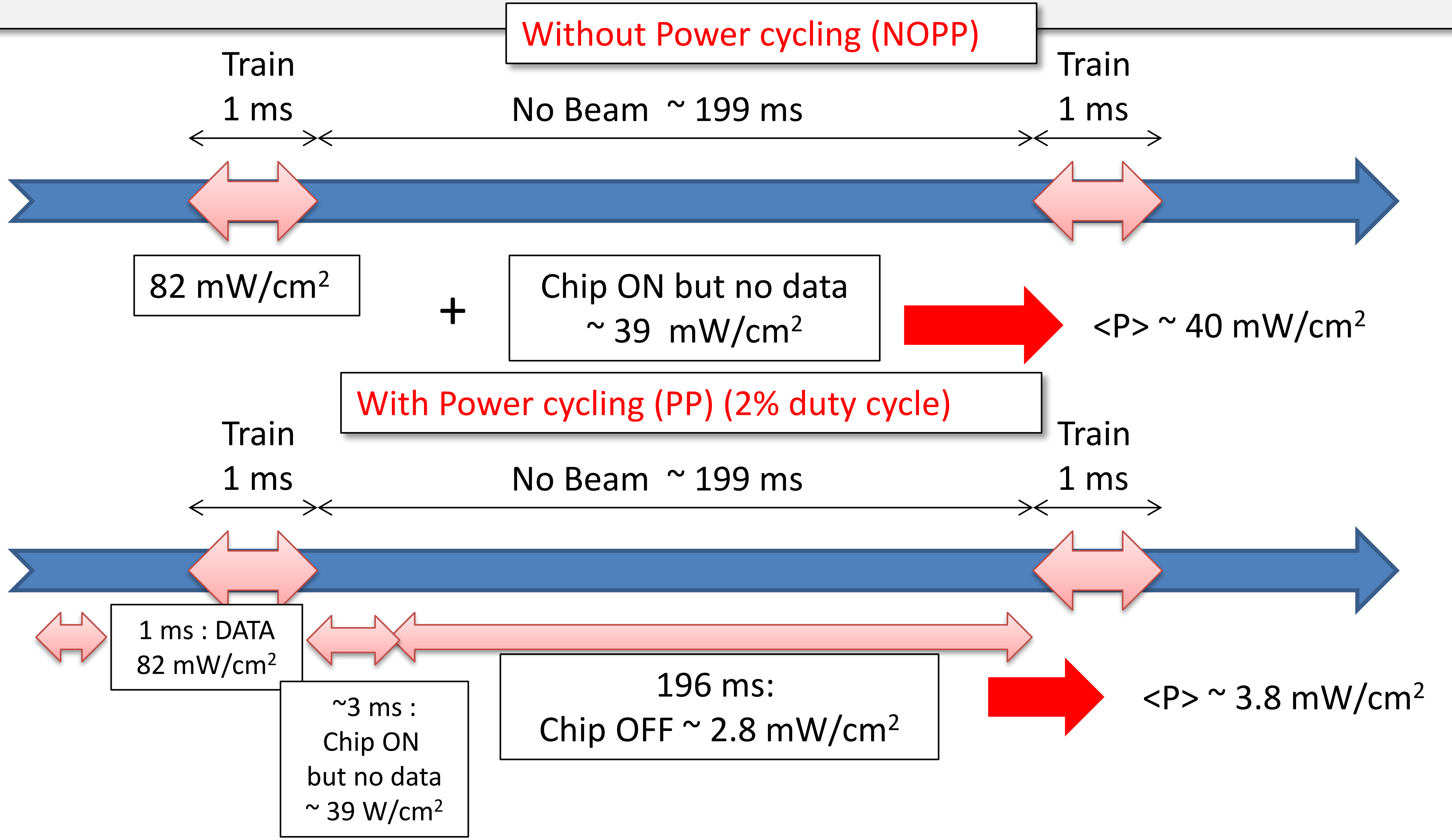
Minimize overlaps and dead space between chips

ILD: VXD dimensions

Figures per layers						
Layer	0	1	2	3	4	5
Layer Radius (mm)	16	18	37	39	58	60
Layer $\|z\|max$ (mm)	61.9	61.9	123.8	123.8	123.8	123.8
Chip Pixel Number in X	1440	1440	1440	1440	1440	1440
Chip Pixel Number in Y	512	512	1024	1024	1024	1024
Chip Pixel PitchX (μm)	21.5	21.5	21.5	21.5	21.5	21.5
Chip Pixel PitchY (μm)	21.5	21.5	21.5	21.5	21.5	21.5
Chip Dimension X (mm) (sensitive area)	30.96	30.96	30.96	30.96	30.96	30.96
Chip Dimension Y (mm) (sensitive area)	11.01	11.01	22.02	22.02	22.02	22.02
Chip Dimension Y (mm) (non sensitive area)	2.0	2.0	2.0	2.0	2.0	2.0
Chip Surface (mm^2) (sensitive area)	341	341	682	682	682	682
Chip Surface (mm^2) (non sensitive area)	62	62	62	62	62	62
Chip Surface (mm^2) (total)	403	403	744	744	744	744
Ladder Length (mm) (sensitive area)	123.8	123.8	123.8	123.8	123.8	123.8
Ladder Width (mm) (sensitive area)	11.01	11.01	22.02	22.02	22.02	22.02
N chip per ladder on each side	4	4	4	4	4	4
Layer Surface (cm^2) (sensitive area)	136.3	136.3	599.7	599.7	926.9	926.9
N Chips Per Layer	40	40	88	88	136	136
Total surface (cm^2) (sensitive area)	3484					

Figures per double layers			
	Layer 0/1	Layer 2/3	Layer 4/5
N Chips in z	4	$4+4=8$	$4+4=8$
N Ladders	10	$2\times 11=22$	$2\times 17=34$
N Chips Per double Layer	80	176	272
N Chips (per architecture)	80	448	
N Total Chips	528		

Power scheme for VXD-ILD (inner layer)



Hypothesis: 3 double sided layers (3483 cm^2), PSIRA architecture (4 μs / 4 μm), DBD background @ $\sqrt{s}$ = 500 GeV, no safety factor

Power: Results

- Chip read-out speed
  - 2 ms - 4 ms
- Power pulsing
  - Power ON, no beam during 1-3 ms
    - ➢ Leading parameter With NO P.P.
  - Power OFF: 10-30 mW/chip
    - ➢ Leading parameter with P.P.
- Outer layers
  - Lower occupancy
  - Power is dominated by outer layers
- Beam background rate
  - DBD – DBD x 2

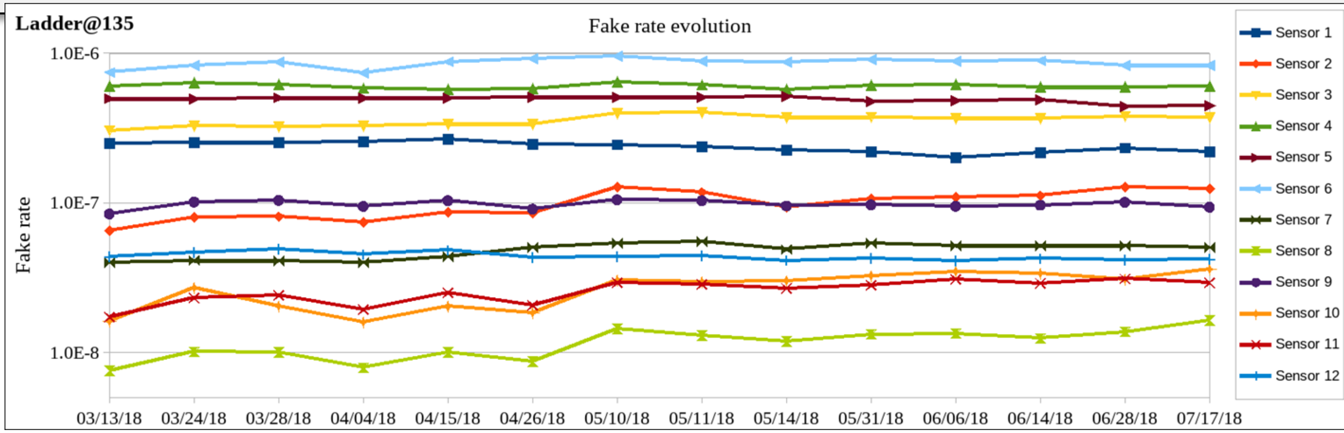
Power Analog $(mW/chip)$	49.22
Power Bias $(mW/chip)$	4.5
Power PriorityEncoder $(mW/chip)$	4.219
Power DigitalPeriphery $(mW/chip)$	64.27
Power PLL $(mW/chip)$	18.5
Power Serializer With Data $(mW/chip)$	86.06
Power Serializer With No Data $(mW/chip)$	0
Power LVDS $(mW/chip)$	56.4

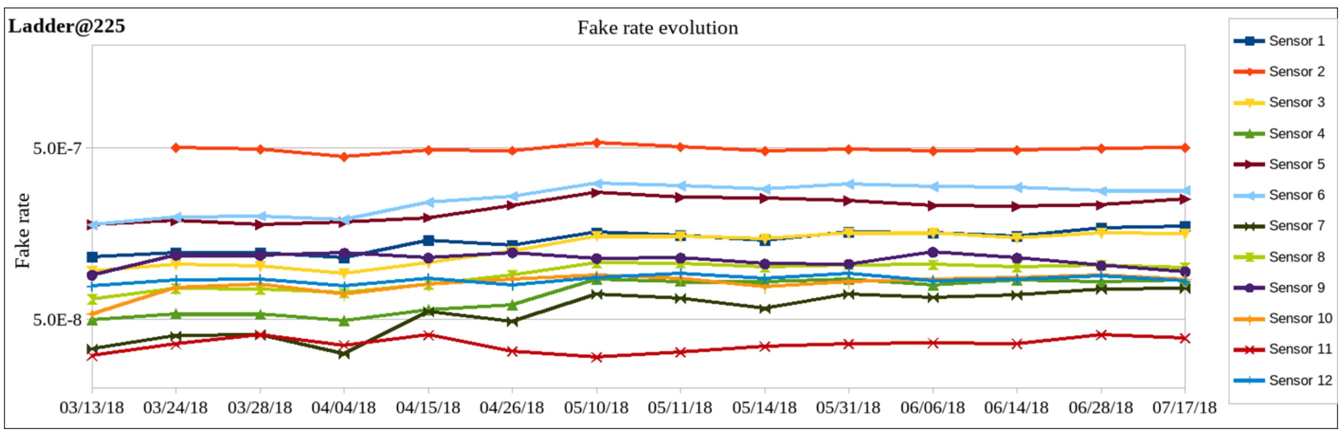
Period	Relative Energy
E during train	225 mJ ~ 4 %
E between train (Power ON)	380 mJ ~ 6 %
E between train (Power OFF)	5740 mJ ~ 90 %

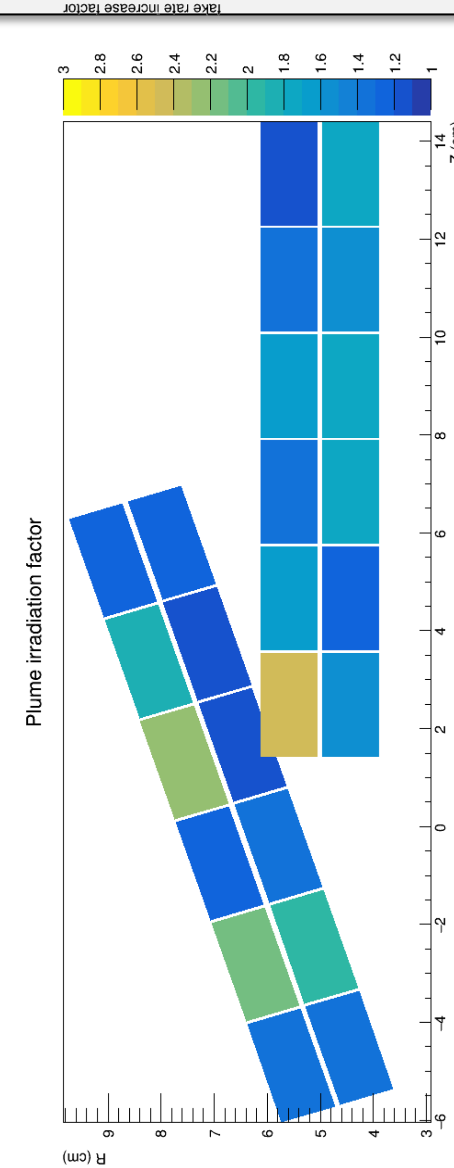
Layers	Relative Power
Layers 0/1	~ 10 %
Layers 2/3	~ 35%
Layers 4/5	~ 55 %

Beam background rate	Read-out speed	<Power (NO P.P.)	<Power> (P.P.)	
	(µs)	(W)	Conservative	Ambitious
DBD	4 µs	102 W	~31 W	~12 W
DBD	2 µs	122 W		
DBD x 2	4 µs	107 W		
DBD x 2	2 µs	127 W		

Plume in Beast 2: Fake rate stability



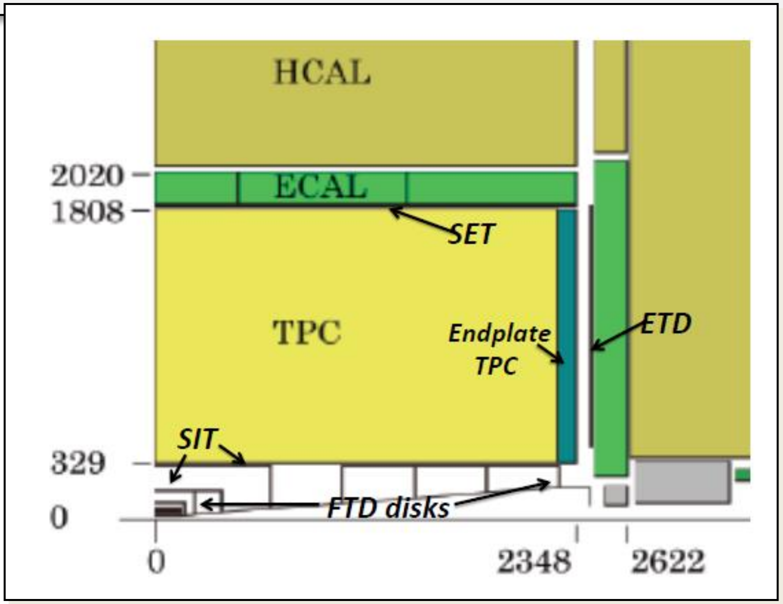




- S/N threshold ≥ 8 ⇨ Fake rate below 10^{-6}
- Average fakerate increase factor = 1.6 ⇨ TID < 1kGy

⇨ Continuous running in stable conditions

ILD dimensions



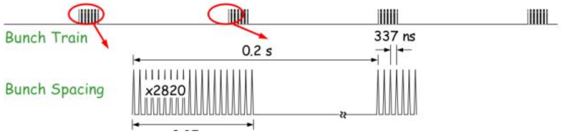
Barrel system						
System	R(in)	R(out) z /mm		comments		
VTX	16	60	125	3 double layers	Silicon pixel sensors,	
				layer 1: $\sigma < 3\mu m$	layer 2: $\sigma < 6\mu m$	layer 3-6 $\sigma < 4\mu m$
Silicon						
- SIT	153	300	644	2 silicon strip layers	$\sigma = 7\mu m$	
- SET	1811		2300	2 silicon strip layers	$\sigma = 7\mu m$	
- TPC	330	1808	2350	MPGD readout	$1 \times 6\text{mm}^2$ pads	$\sigma = 60\mu m$ at zero drift
ECAL	1843	2028	2350	W absorber	SIECAL	30 Silicon sensor layers, 5×5 mm^2 cells
					EcECAL	30 Scintillator layers, 5×45 mm^2 strips
HCAL	2058	3410	2350	Fe absorber	AHCAL	48 Scintillator layers, $3 \times 3\text{cm}^2$ cells
					SDHCAL	48 Gas RPC layers, 1×1 cm^2 cells
Coil	3440	4400	3950	3.5 T field	2λ	
Muon	4450	7755	280	14 scintillator layers		

SIT characteristics (current baseline = false double-sided Si microstrips)					
Geometry			Characteristics		Material
R[mm]	Z[mm]	cosθ	Resolution R-ϕ[μm]	Time [ns]	RL[%]
153	368	0.910	R: σ=7.0,	307.7 (153.8)	0.65
300	644	0.902	z: σ=50.0	σ=80.0	0.65

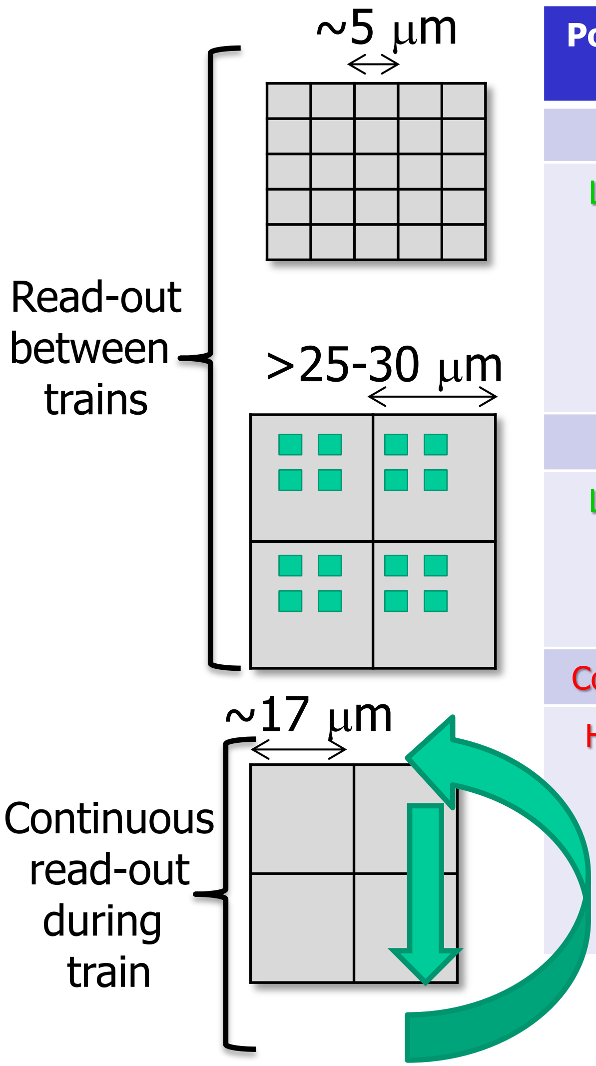
SET characteristics (current baseline = false double-sided Si microstrips)					
Geometry			Characteristics		Material
R[mm]	Z[mm]	cosθ	Resolution R-ϕ[μm]	Time [ns]	RL[%]
1811	2350	0.789	R: σ=7.0,	307.7 (153.8)	0.65

ETD characteristics (current baseline = single-sided Si micro-strips, same as SET ones)				
Geometry			Characteristics	Material
R[mm]	Z[mm]	cosθ	Resolution R-ϕ[μm]	RL[%]
419.3-1822.7	2420	0.985-0.799	x:σ=7.0	0.65

FTD characteristics (design baseline: pixels for two inner disks, microst				
Geometry			Characteristics	Material
R[mm]	Z[mm]	cosθ	Resolution R-ϕ[μm]	RL[%]
39-164	220	0.985-0.802	σ=3-6	0.25-0.5
49.6-164	371.3	0.991-0.914		0.25-0.5
70.1-308	644.9	0.994-0.902	σ=7.0	0.65
100.3-309	1046.1	0.994-0.959		0.65
130.4-309	1447.3	0.995-0.998		0.65
160.5-309	1848.5	0.996-0.986		0.65
190.5-309	2250	0.996-0.990		0.65



Read-out strategies vs resolution/occupancy



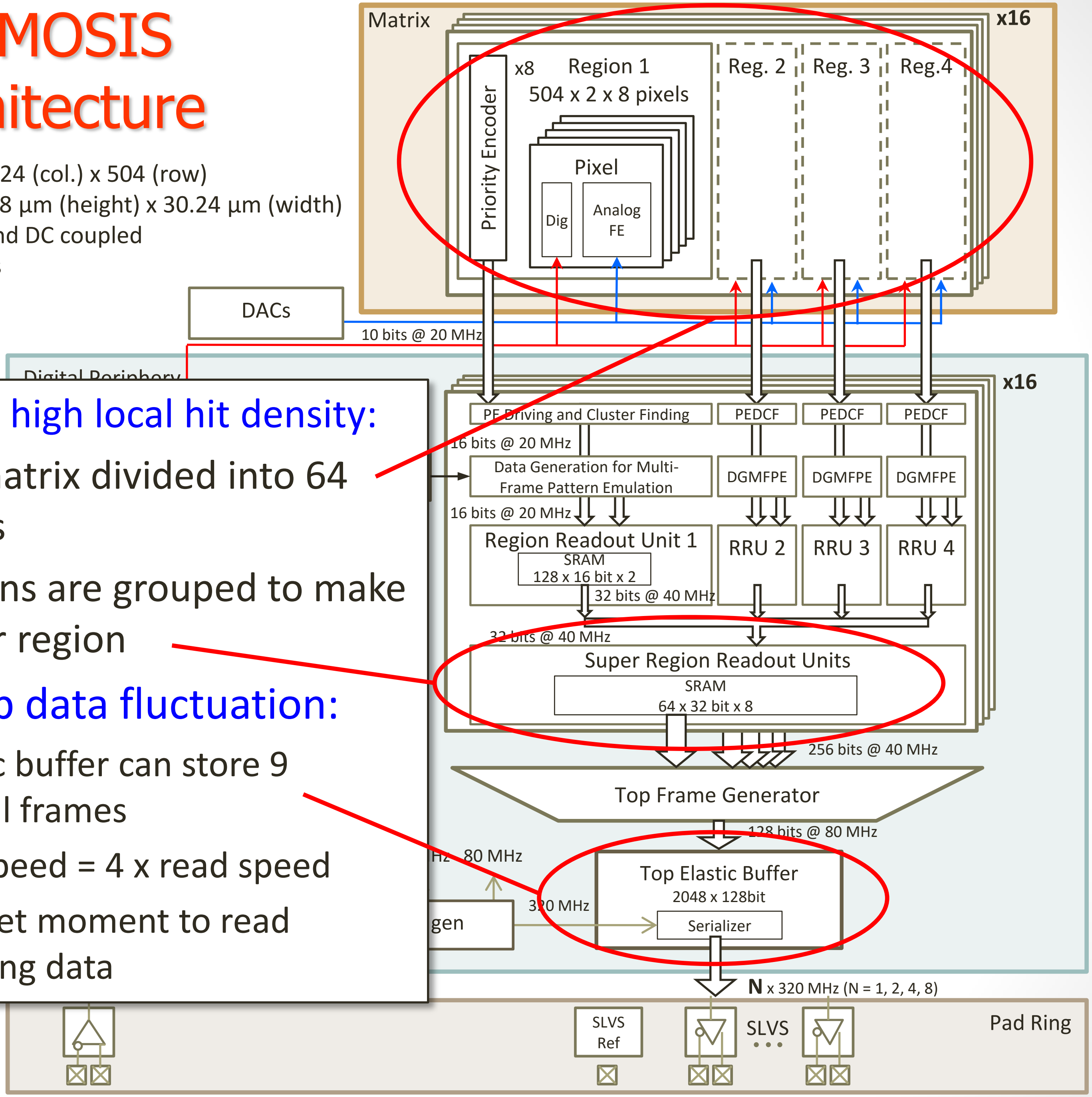
Power	Time resolution	Spatial resolution	Advantages	Caveats
Fine pixels (e.g. FPCCD)				
Low	1 complete train	~ 1 µm	Spatial Resolution Hit separation Beam background tagging capabilities ? (cluster shapes)	⇨x16 #pixels to read-out in 200ms ⇨No time stamping ⇨Occupancy issues ?
In pixel circuitry to store hits with time stamping (e.g. chronopixels, SOI)				
Low	Single or few bunches (>~ 0.5 µs)	>~ 5 µm	Hit time stamping Well suited to outer layers	⇨BX time stamping storage in conflict with granularity
Continuous read-out during train (e.g. DEPFET, CMOS): rolling shutter or priority encoding.				
High	Few to 10s bunches (5-50 µs)	~ 3 µm	Time & spatial resolution compromise	Power cycling mandatory ? ⇨F(Lorentz) ~ 10^s grams ⇨Distribute 100s Amps shortly before train ⇨heat cycles the ladders.

⇨ Figures may evolve significantly with R&D and access to new technologies
e.g. feature size ⇨Power, read-out speed, granularity, etc.

⇨Different options / room for mixed strategies ?
e.g. double sided ladders: 1-fast / 1-precise

MIMOSIS architecture

Matrix dimension: 1024 (col.) x 504 (row)
Pixel dimension: 26.88 µm (height) x 30.24 µm (width)
2 kind of pixels: AC and DC coupled
Integration time: 5 µs



- To sustain high local hit density:
  - Pixel matrix divided into 64 regions
  - 4 regions are grouped to make a super region
- To absorb data fluctuation:
  - 1 Elastic buffer can store 9 maximal frames
  - Write speed = 4 x read speed
  - Use quiet moment to read remaining data

Charge collection Diffusion vs Drift

- Resolution governed by
  - Pitch
  - S/N & Collecting diode
    - ➢ Charge sharing
    - ➢ epi. thickness, resistivity, etc.
  - Signal encoding (binary or ADC)

- Drift reduces charge sharing
  - ⇨ Reduces cluster size
  - ⇨ degrades resolution
  - ⇨ Improve S/N in seed
  - ⇨ Better Radiation hardness
  - ⇨ Faster charge collection time (<10 ns)