Testbeam 2019 – Status at LAL

Dominique Breton, Julien Bonis, Alexandre Gallas, Jimmy Jeglot, Adrian Irles, Jihane Maalmi, Roman Pöschl, Alice Thiebault, Dirk Zerwas

Testbeam preparation meeting 20/3/19

Objectives:

- Comparison of ASU based on BGA and of ASU based on COB
  Two of each type = 4 ASUs

- Test of new SL-Boards

Availability of hardware

- FEV-BGA
  - 1 FEV11 completely cabled
  - 2 FEV12 will be cabled until middle of April

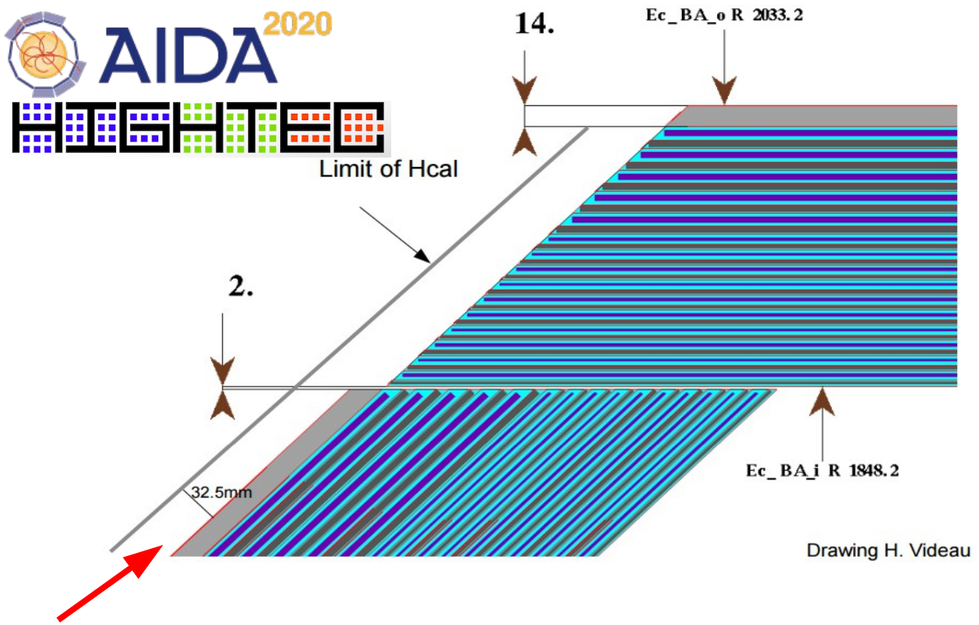
- FEV_COB
  - 1 FEV COB equipped with ASICs,
  - 2 FEV_COB will be bonded until beginning of April

- 10 SL Boards -> Reminder see next slide

- Huge number of GradConn Connectors

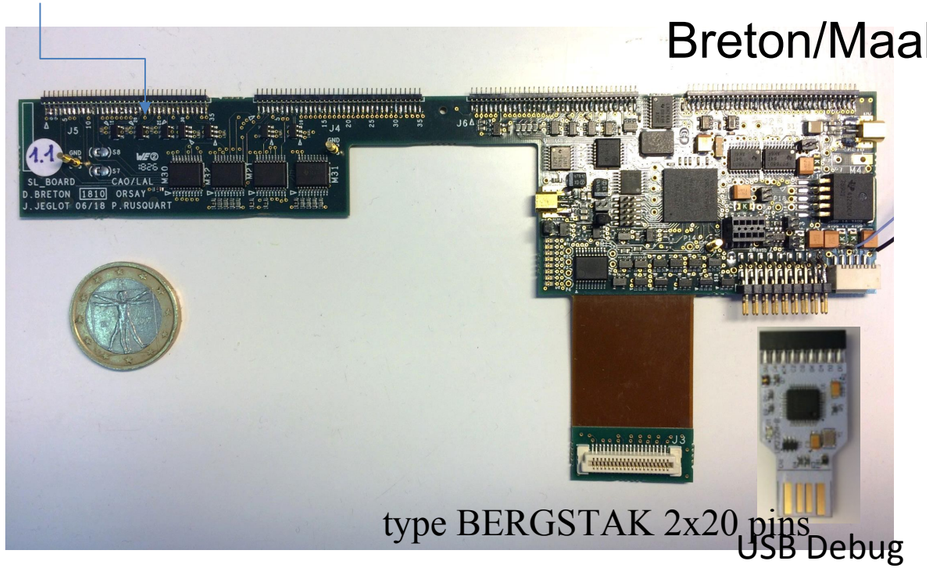
- 1 SMBv4 for check-out of ASUs

Digital electronics – Getting fit for ILD



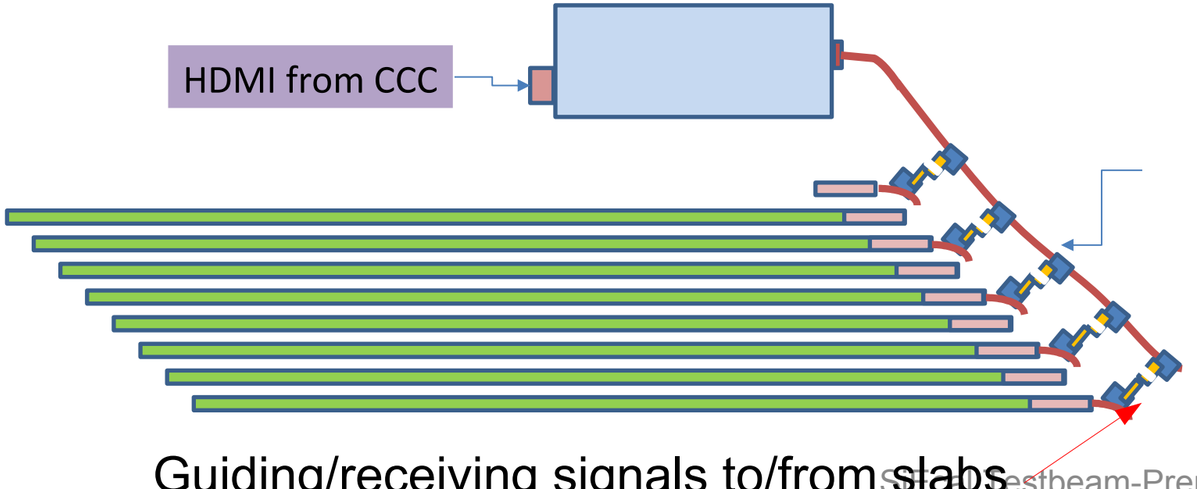
Approximately 6cm between Ecal and Hcal

Breton/Maalmi/Jeglot

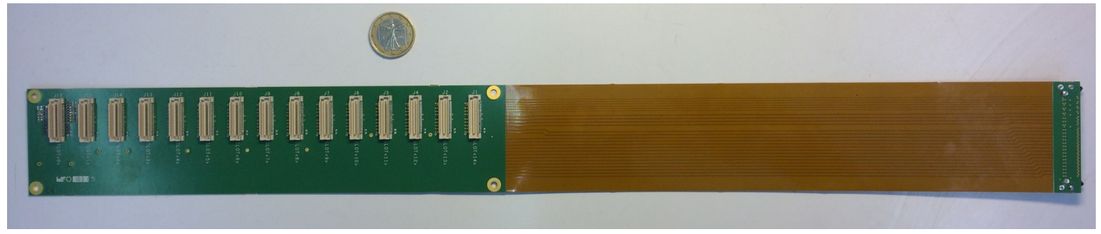


SL Board at the end of layer

CORE Kapton – replaces bulky HDMI cables

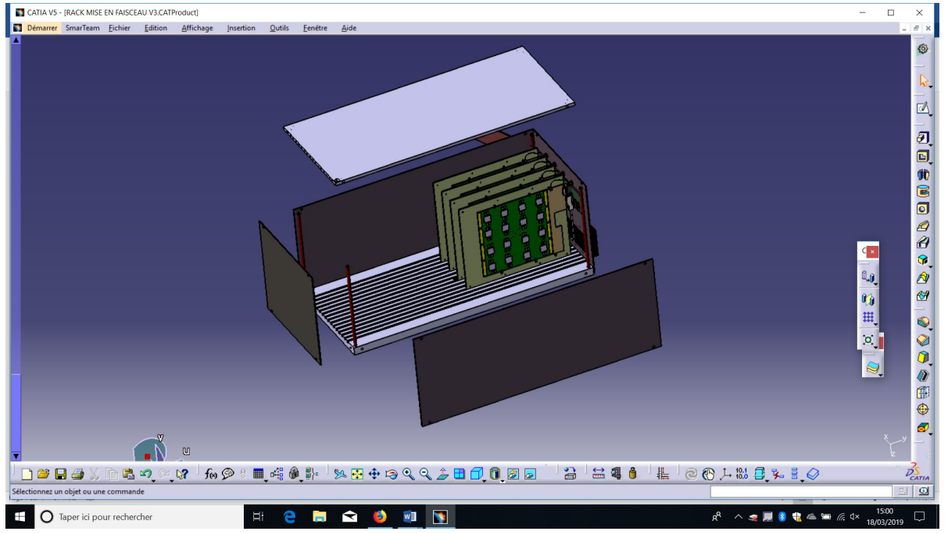


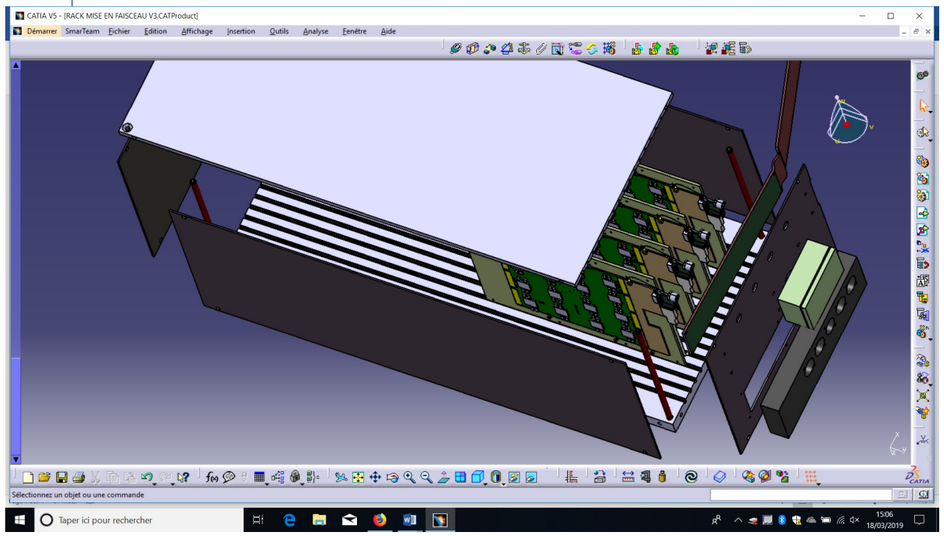
Guiding/receiving signals to/from slabs

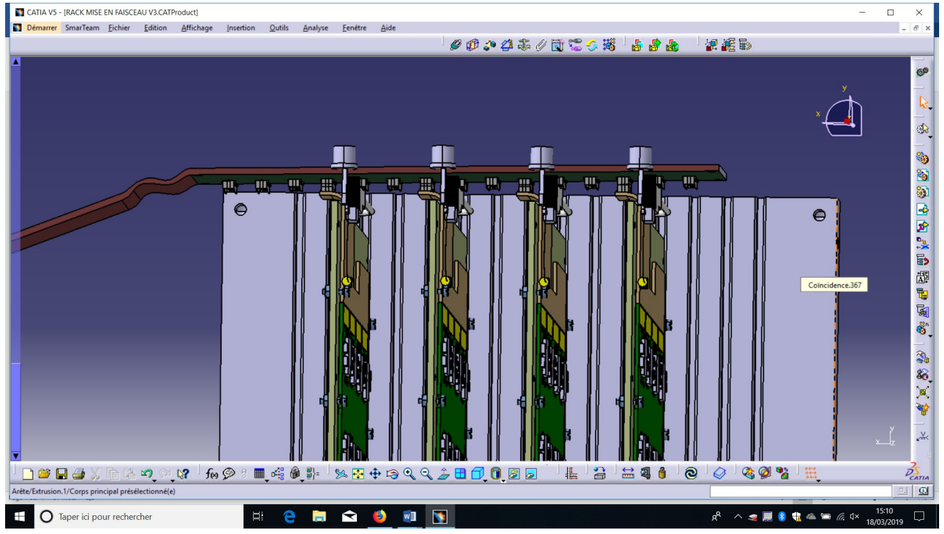


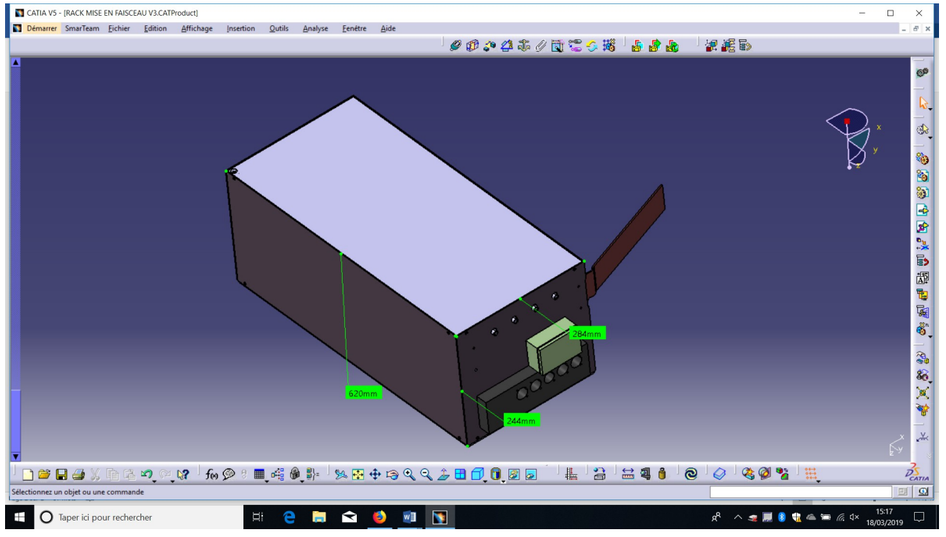
- Hardware exists:
- Firmware for communication with ASICs about to be written

Preparation work – Mechanical Structure









Preparation work – Mechanical Structure Explications

Rack for short slabs for beam test :

- support dimensioned for for ASU+SL-board
- support can integrate 7 short slabs courts et 8 W layers (or 15 short slabs after some modifs.)
- Vertical positioning of short slabs courts between 2 grooved plates, light tight closing and cables passages

Status of beam test preparation – ASUs and electronics

- All ASU (w/o wafers) available or available soon (already now enough for immediate tests)
  - Enough SK2a for chip bonding

- Check-out with SMBv4 board

- SMBV4 available but needs to be equipped with GradConn Connectors and need some minor soldiering work
  - SMBv4 availability is critical to ensure well functioning ASUs
  - GradConn connectors will get mounted until beginning of April
  - Soldiering work in collaboration with Remi during next two weeks

- Firmware for SL Board about to be written
  - Will take however at least two more months

Status of beam test preparation - Cabling

- LV crate cabled and available
- About to cable box for HV distribution and current measurement with Keithley
- Patch panel cabling can start soon, i.e. next week
  - Need to settle cable lengths between panel and layers
- In addition several auxiliary cables for testbench work have been manufactured or will be manufactured
- Thanks to Francisco Campos

Silicon wafers

- Four layers are equivalent to 16 wafers

- At LAL we dispose 2 full size wafers of 500mum
  - Two more wafers from LLR and from LPNHE in exchange for TLU Purchase

- Need 10 more from “French Stock”
- What is the “French Stock”?

- In contact with LPNHE for availability of gluing robot

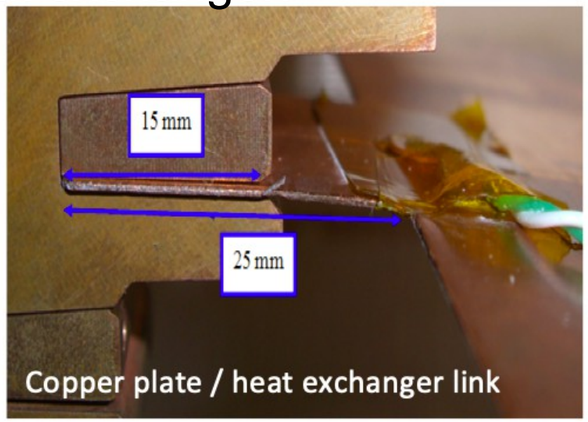
- Schedule depends critically on availability of SMBv4 (see above) but expect that gluing could start ~beginning of may at the latest (modulo bad surprises from ASUs)

Conclusion

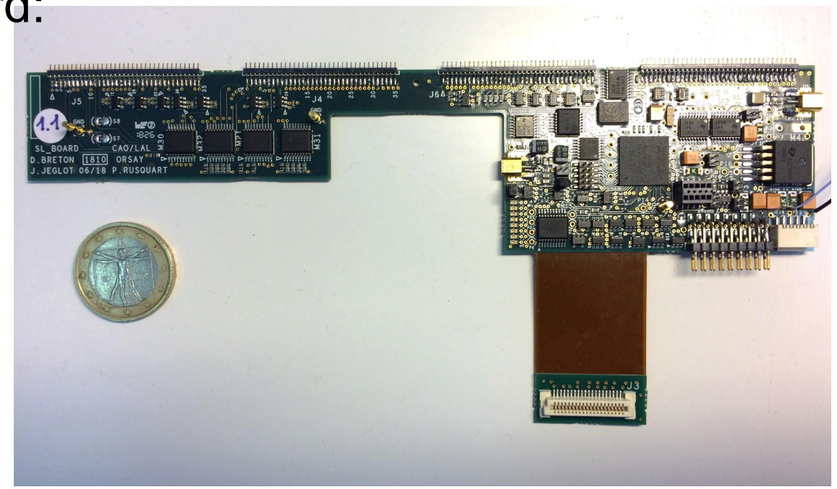
- On track for beam test
- The “scene is settled” but April will be critical month
- Regular (~weekly) technical briefings at LAL to monitor progress

SiEcal - “Local Integration – End of layers” I

Heat exchanger:



SL-Board:



- Need to bring the individual pieces together

- A first meeting between developers of Cooling system and developers of SL-Card revealed no showstopper on integration

Summary and conclusion

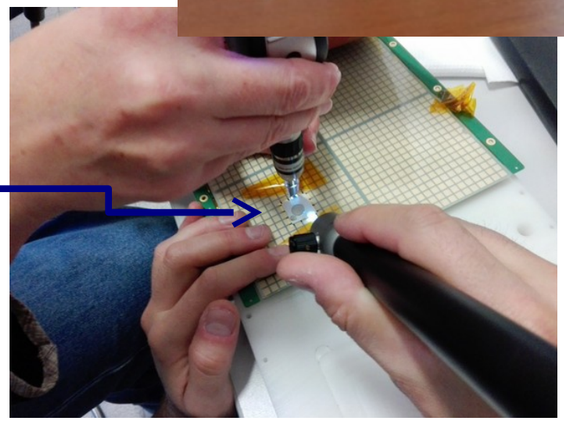
- R&D for SiEcal addresses all elements relevant for an installation into the ILD detector
- Current effort concentrates on space reduction of individual components (i.e. Digital r/o)
- Alltogether we believe that we can build the SiEcal largely as designed
- Design of SiEcal puts several constraints on other detectors
- 5 Hubs of type Hub1/stave between Ecal and Hcal may constitute a heat source (~10 W each)
  - Should not forget the 50 Hub2/stave with ~3-5 W consommation each
- Need a decision on how TPC will be fixed
- Need a decision whether we will be allowed to stay on the platform
  - If not need to find space at corresponding height in service gallery
- Update of ICD in progress

Backup

SiEcal – News from COB

- **LAL/OMEGA collaboration with Corean Group of SKKU (EOS company for the PCB)**
  - FEV11_COB: **10 boards of 1.2mm**, good planarity and good electrical response.
  - SK2a wirebonded at CERN (Study by LPNHE and P2IO Platform CAPTINNOV)

- **Successful debugging w/o sensors:**
  - (~4% of noisy channels, good response to injected signals)



Visual inspection of the result of the gluing

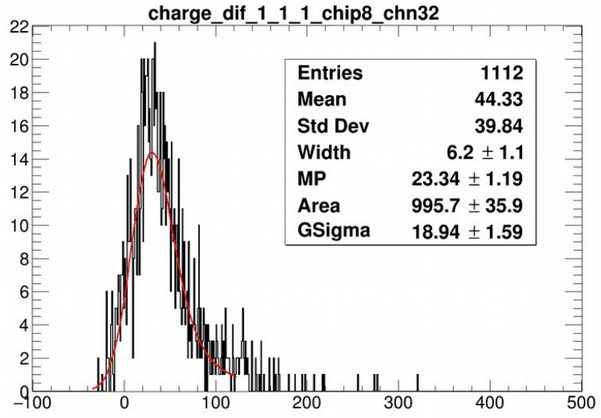
- **Debugging with sensors (baby wafers 3x3 px)**
  - The system was not ready for test at DESY@2018.
  - New wafer testbench setup in LAL borrowed from LPNHE.
  - Duplication ongoing at LAL (using the CAPTINOV platform)

- ● 3 baby wafers characterized, glued and tested with cosmics. Test with radioactive sources are in preparation.

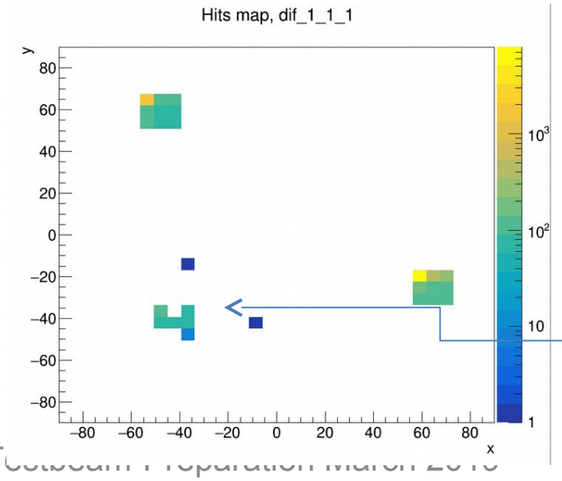
A. Example of MIP spectrum from cosmic rays.

B. 3.6pF

Plot from V. Lohezic



A. Example of MIP spectrum from cosmic rays.



A. Hit map with for cosmic runs.

B. (different mapping to BGA versions)

C. Baby wafer tested in DESY. Some glue is spilled.