THE CMS HIGH GRANULARITY CALORIMETER FOR HL-LHC

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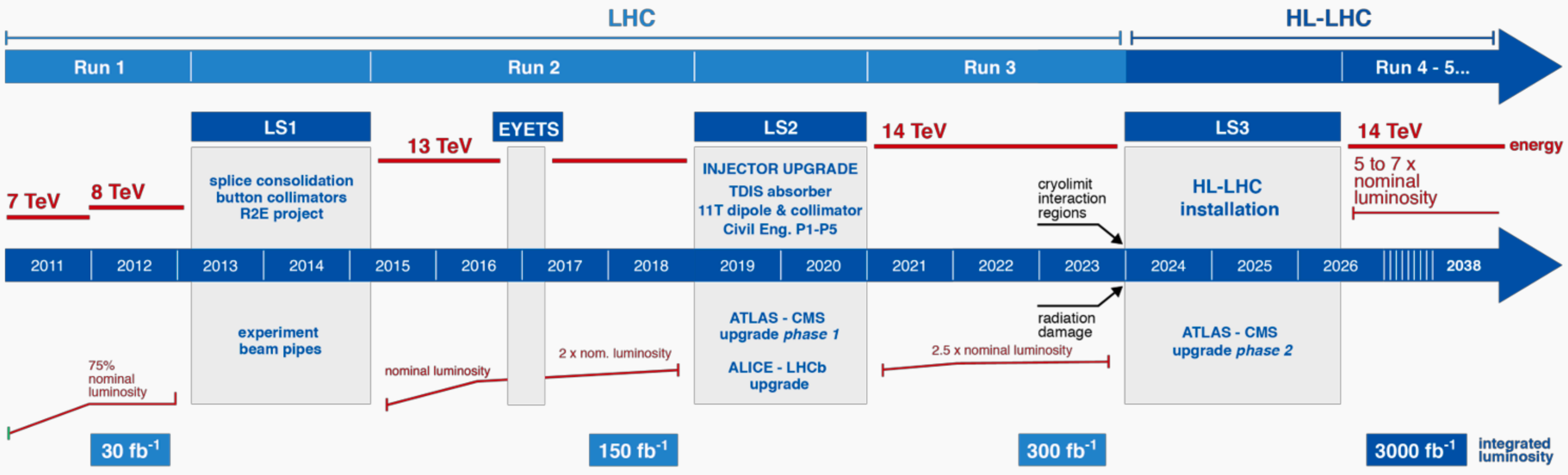
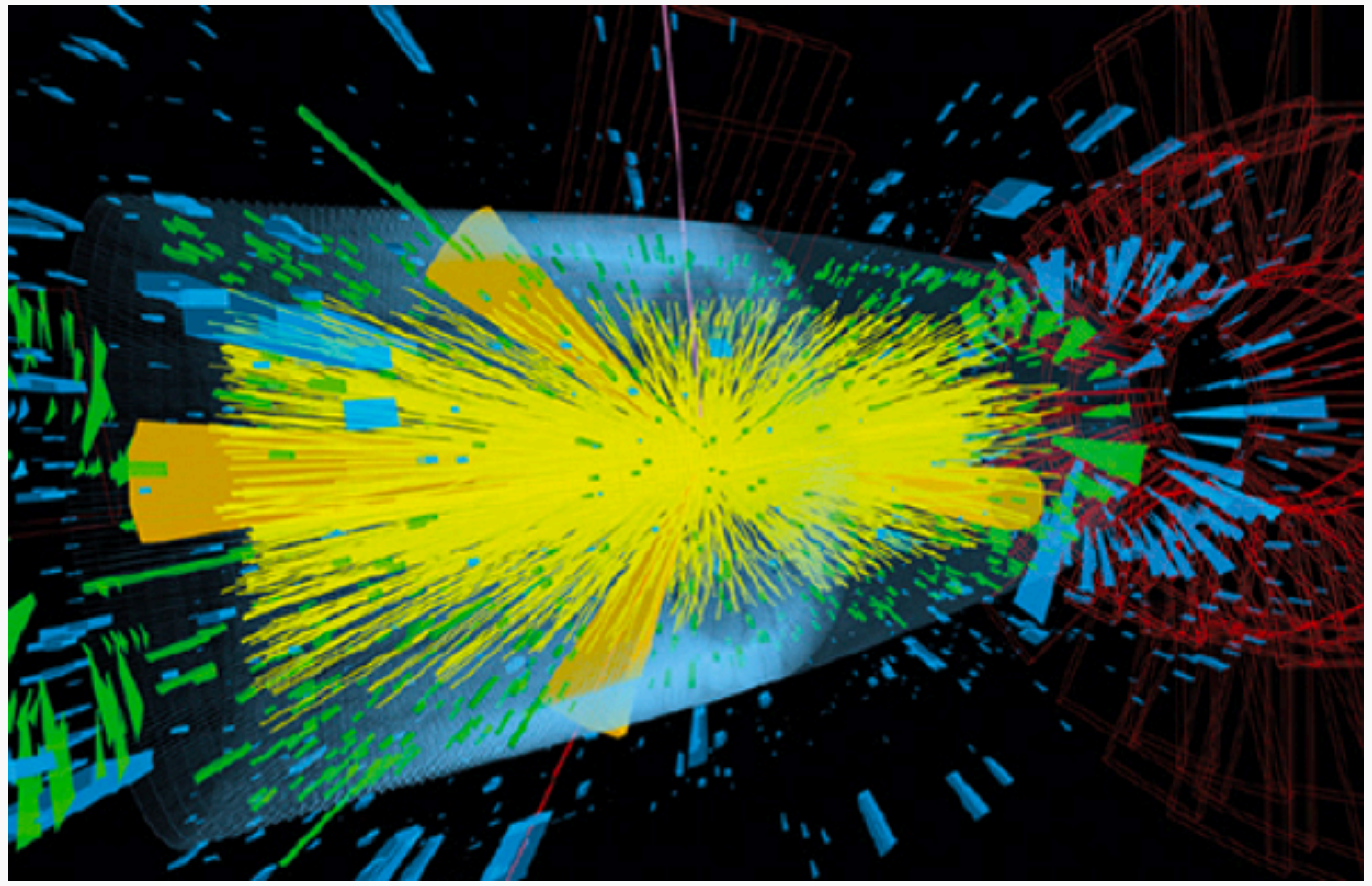
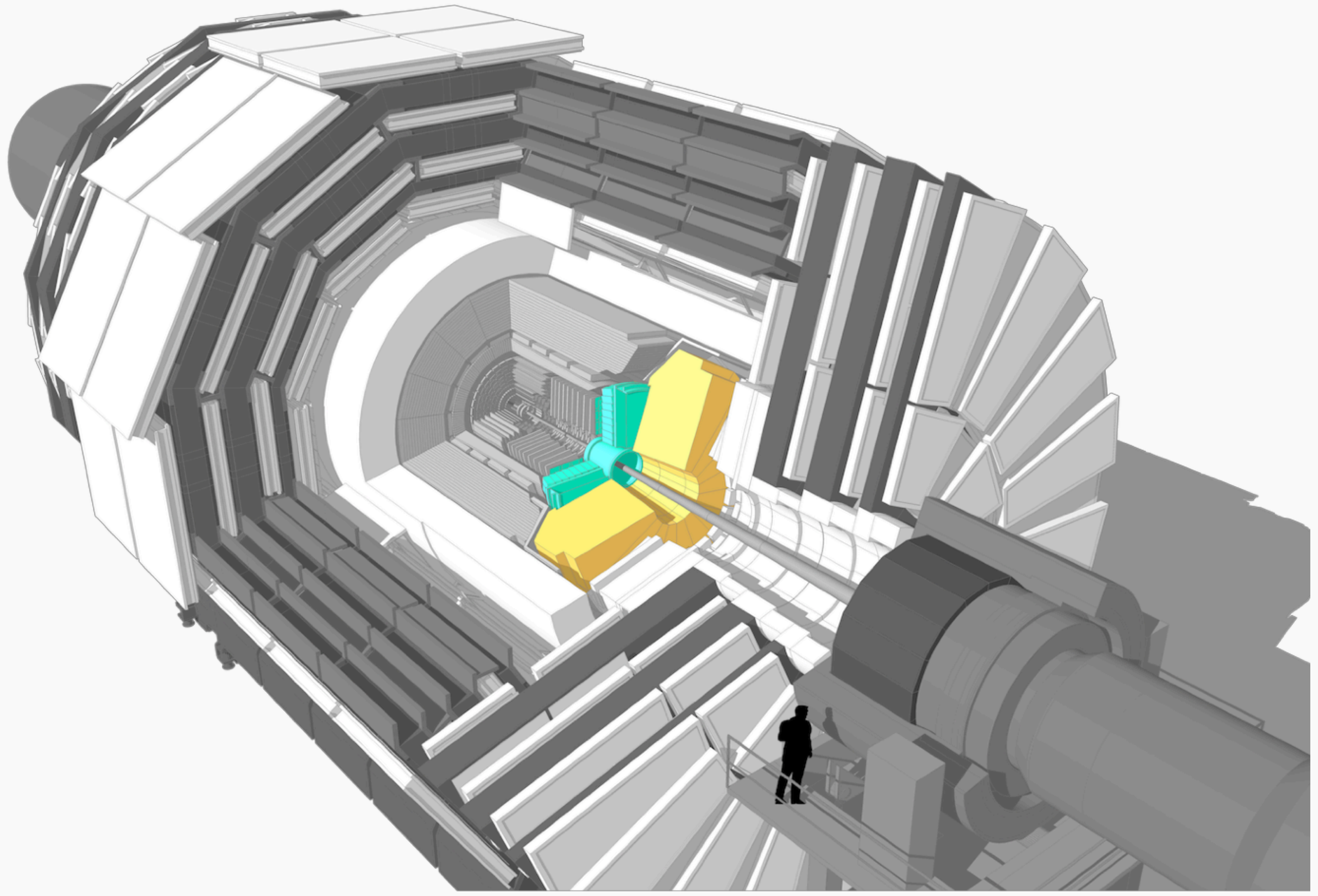
CHALLENGES AT THE HIGH-LUMINOSITY LHC

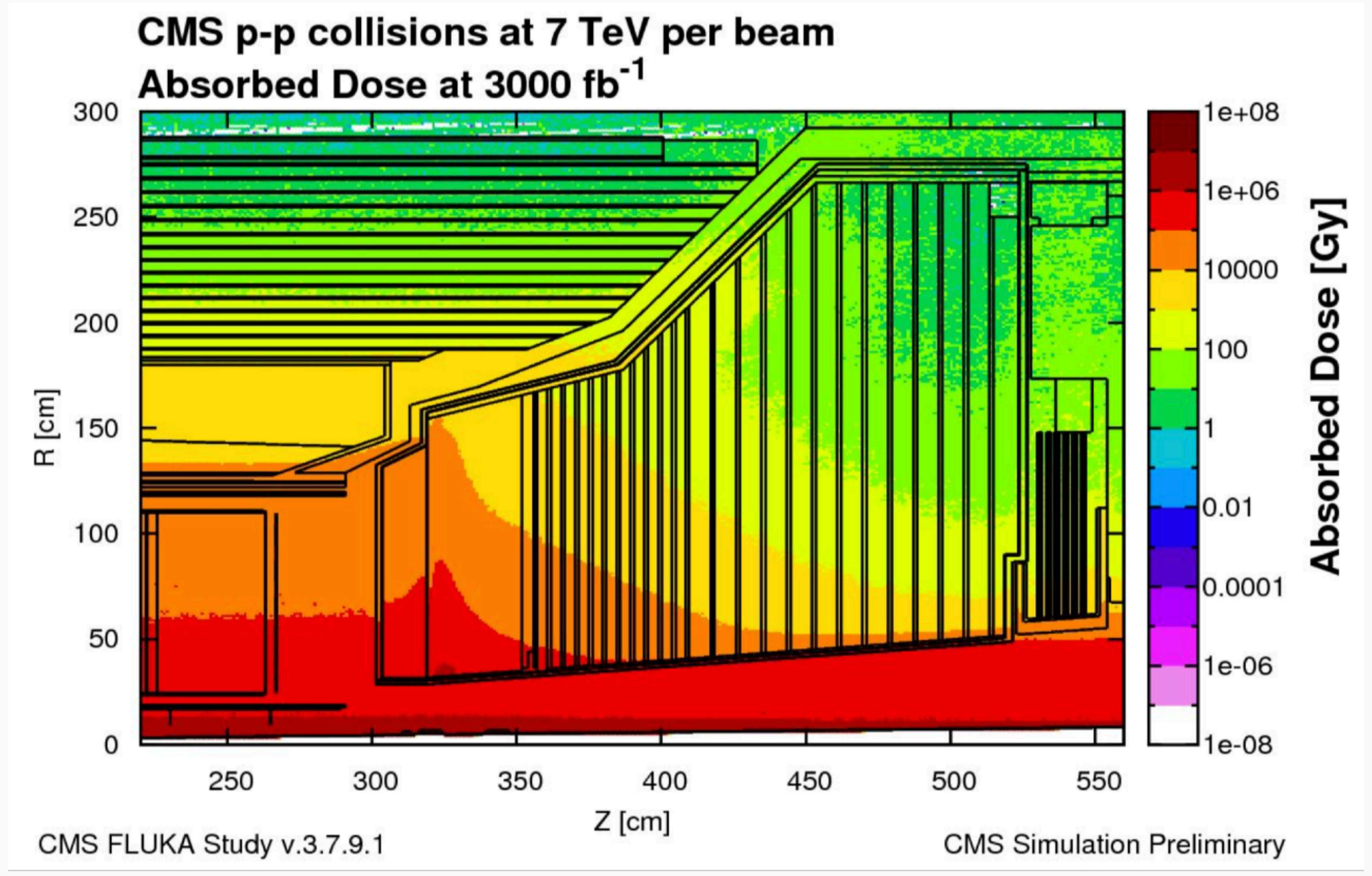
- The HL-LHC will provide >5 (x10) instantaneous (integrated) luminosity of LHC
  - Increased radiation and pileup levels 140-200 >> 3-4x larger than in Run2
- Current CMS detectors designed for 300/fb
  - Comprehensive Phase-2 detector upgrade programme to cope with HL-LHC
  - Tight timeline: LS3 in 2023 and Run4 starts in 2026!





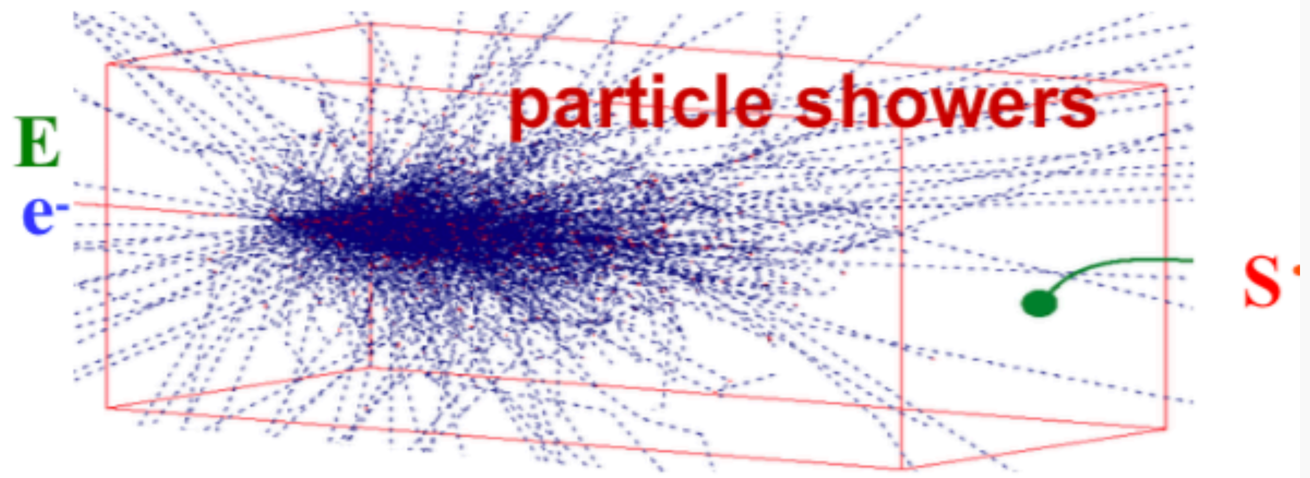
CMS CALORIMETER ENDCAP FOR THE HL-LHC





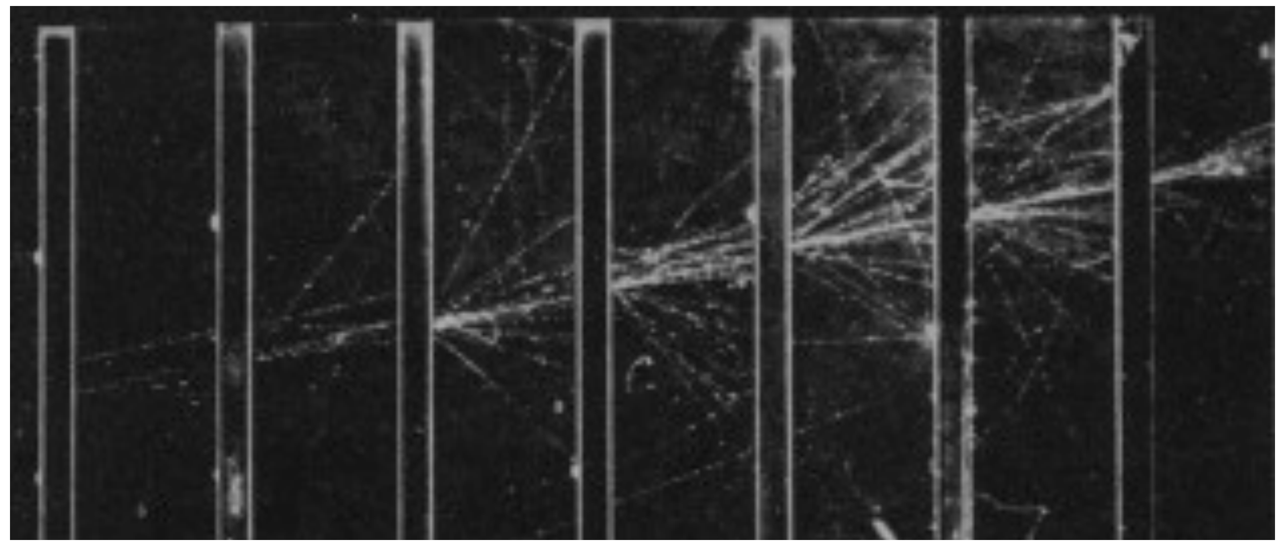
- CMS endcap calorimeters will need to be replaced:
  - ECAL crystals and HCAL scintillators suffer from irreparable radiation damage after 500/fb
- The **High Granularity Calorimeter (HGCAL)** will become the new Calorimeter Endcap (CE):
  - **Radiation hard detectors** based on a mix of silicon and scintillator technology
  - High transverse and longitudinal granularity + timing (5D!) for **enhanced particle flow reconstruction and ID/pileup mitigation**
  - Preserve or even improve **sensitivity** in the interesting and busy **forward region for VBF/VBS**

CALORIMETERS IN HEP



Convert energy **E** of incident particles to detector response **S**:

$S \propto E$

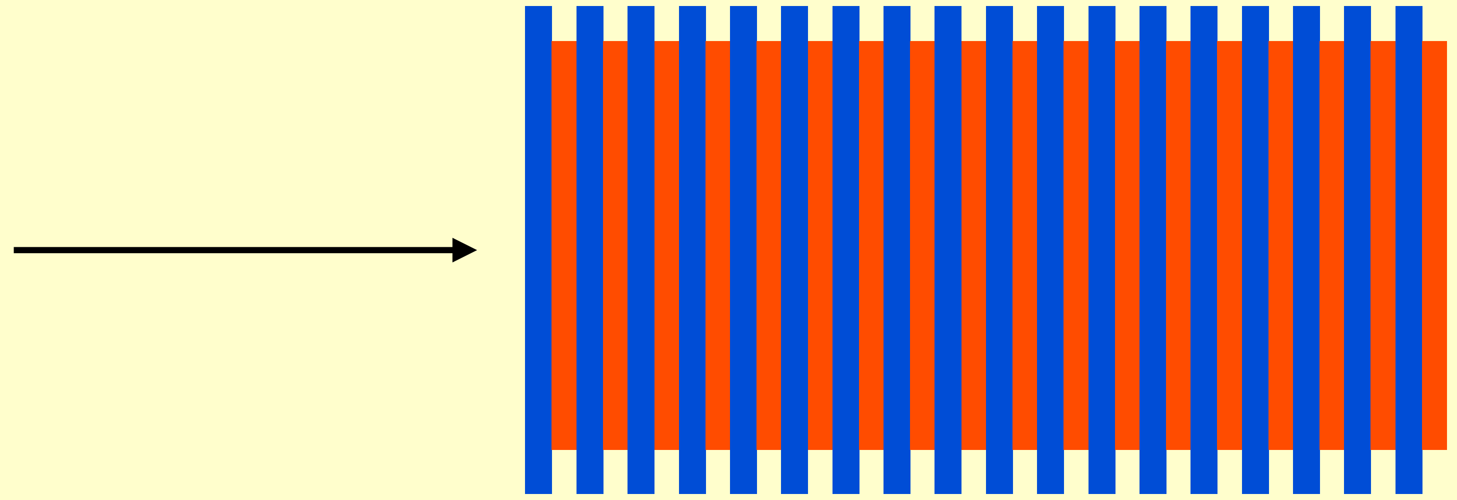


Lead absorbers in cloud chamber

There are two general classes of calorimeter:

Sampling calorimeters:

Layers of passive absorber (such as Pb, or Cu) alternate with active detector layers such as Si, scintillator or liquid argon



Homogeneous calorimeters:

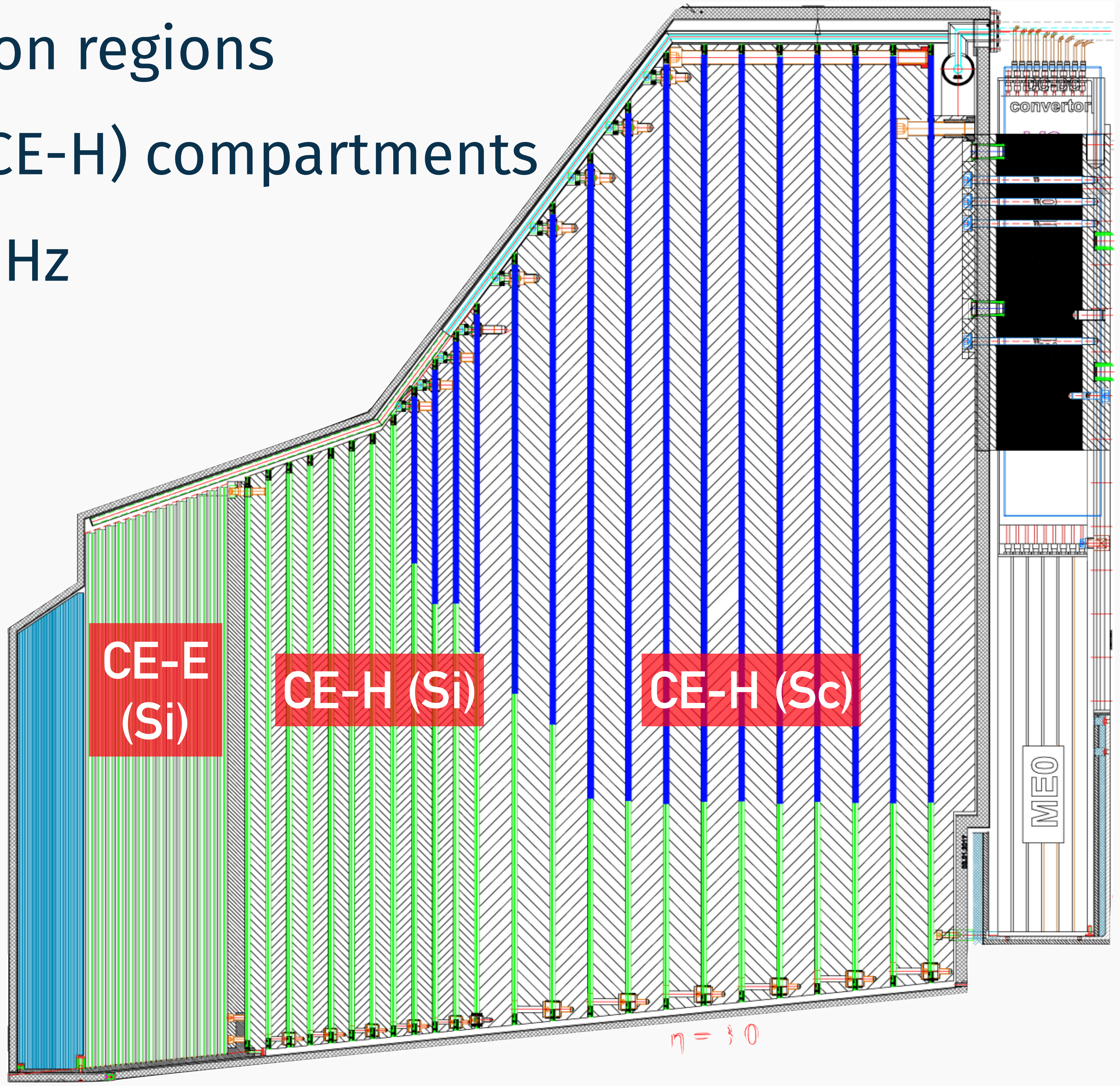
A single medium serves as both absorber and detector, eg: liquified Xe or Kr, dense crystal scintillators (BGO, $PbWO_4$ **…….**), lead loaded glass.

More info on calorimeters, e.g. here

THE CMS HIGH GRANULARITY CALORIMETER

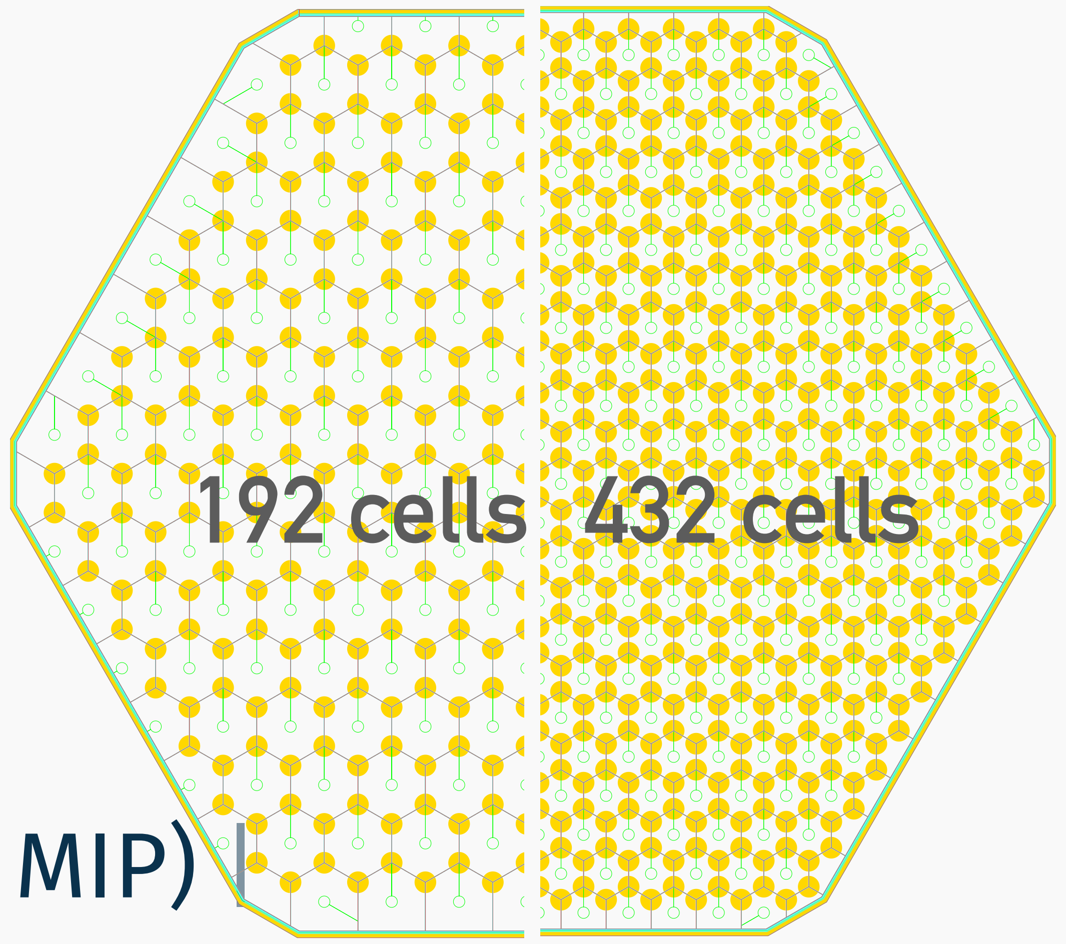
- The high luminosity and high granularity are a big challenge for the detector design:
  - Silicon/scintillator detectors in the high/low radiation regions
  - 28 layers in the ECAL (CE-E) + 24 layers in the HCAL (CE-H) compartments
  - Triggering and reading data of >6M channels at 40 MHz

Endcap coverage: $1.5 < \lvert\eta\rvert < 3.0$		
Total	Silicon sensors	Scintillator
Area	600 m^2	500 m^2
Number of modules	27 000	4 000
Cell size	0.5 — 1 cm^2	4 — 30 cm^2
N of channels	6 000 000	400 000
Power	Total at end of HL-LHC: ~180 kW @ -30^{o}C	

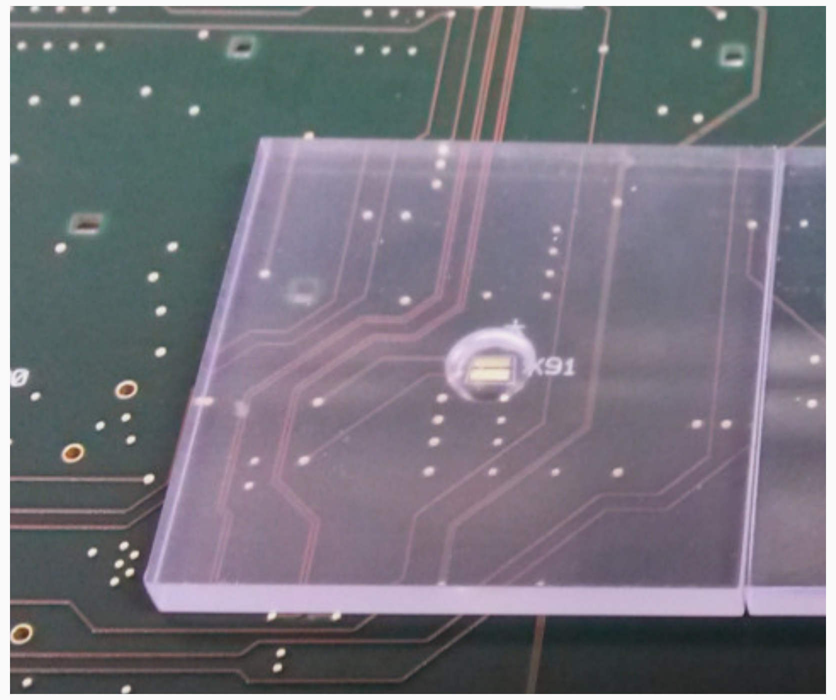


KEY INGREDIENTS OF HGCAL

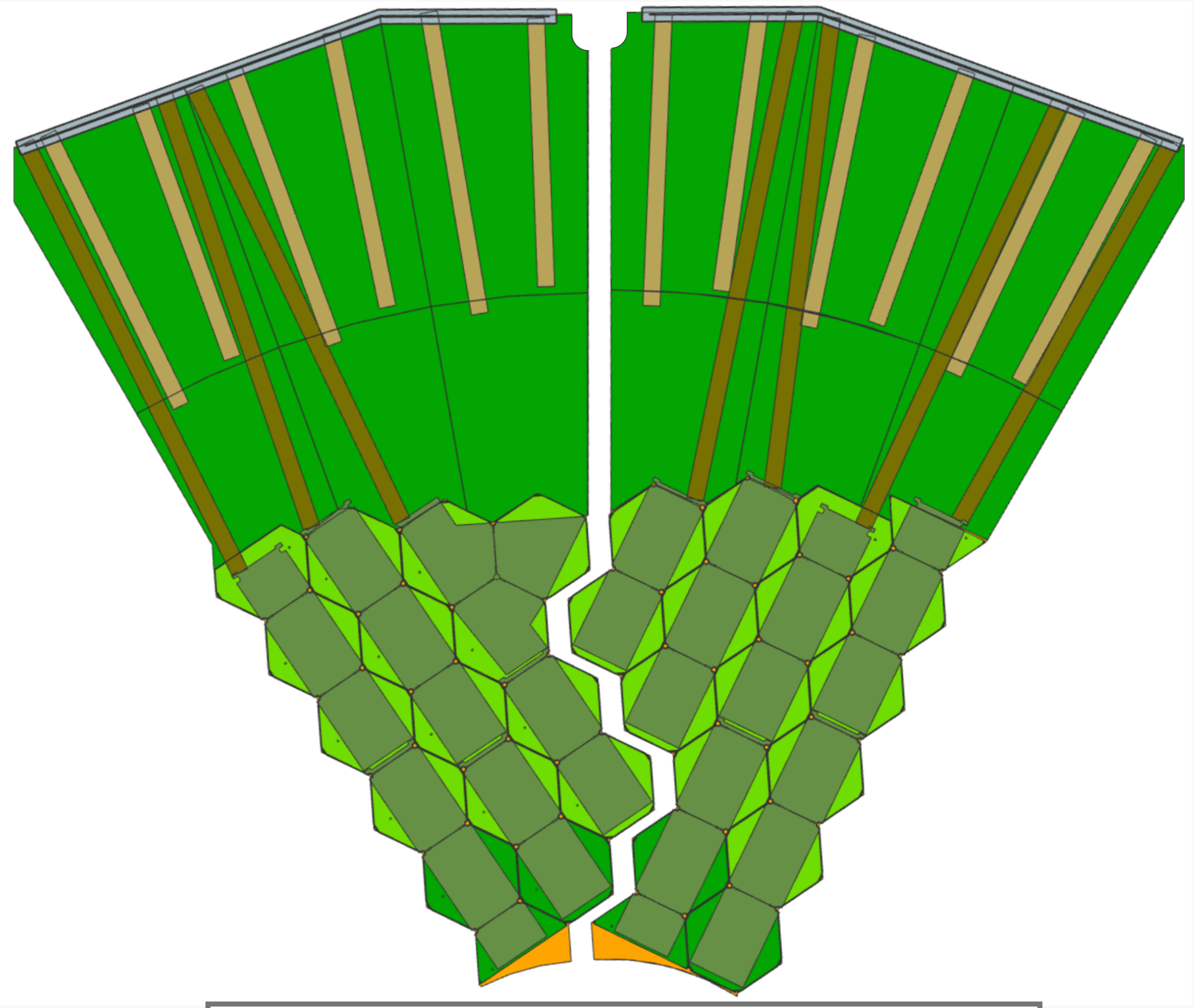
- Active elements:
  - 8” hexagonal silicon wafers p/n-type | thickness: 120/200/300 um | 192/432 cells | HV bias up to 1kV
  - SiPM-on-tile scintillator readout (à la CALICE AHCAL)
- Electronics:
  - Front-End ASIC: rad. hard | low noise | high dynamic range (1-1000 MIP) | timing measurement | < 15 mW/ch consumption
    - High range with low power due to time-over-threshold (TOT)
    - Time-of-arrival (TOA) method with time precision of 20 ps
  - Trigger data from ASICs (300 TB/s) fed through concentrators to the back-end system (2 TB/s) in multi-stage approach
- Engineering:
  - 30º/60º cassettes tiled with hexagonal silicon modules and partially mixed with scintillator tile boards
  - Full detector volume cooled to -30ºC



Silicon sensors



SiPM-on-tile (AHCAL)

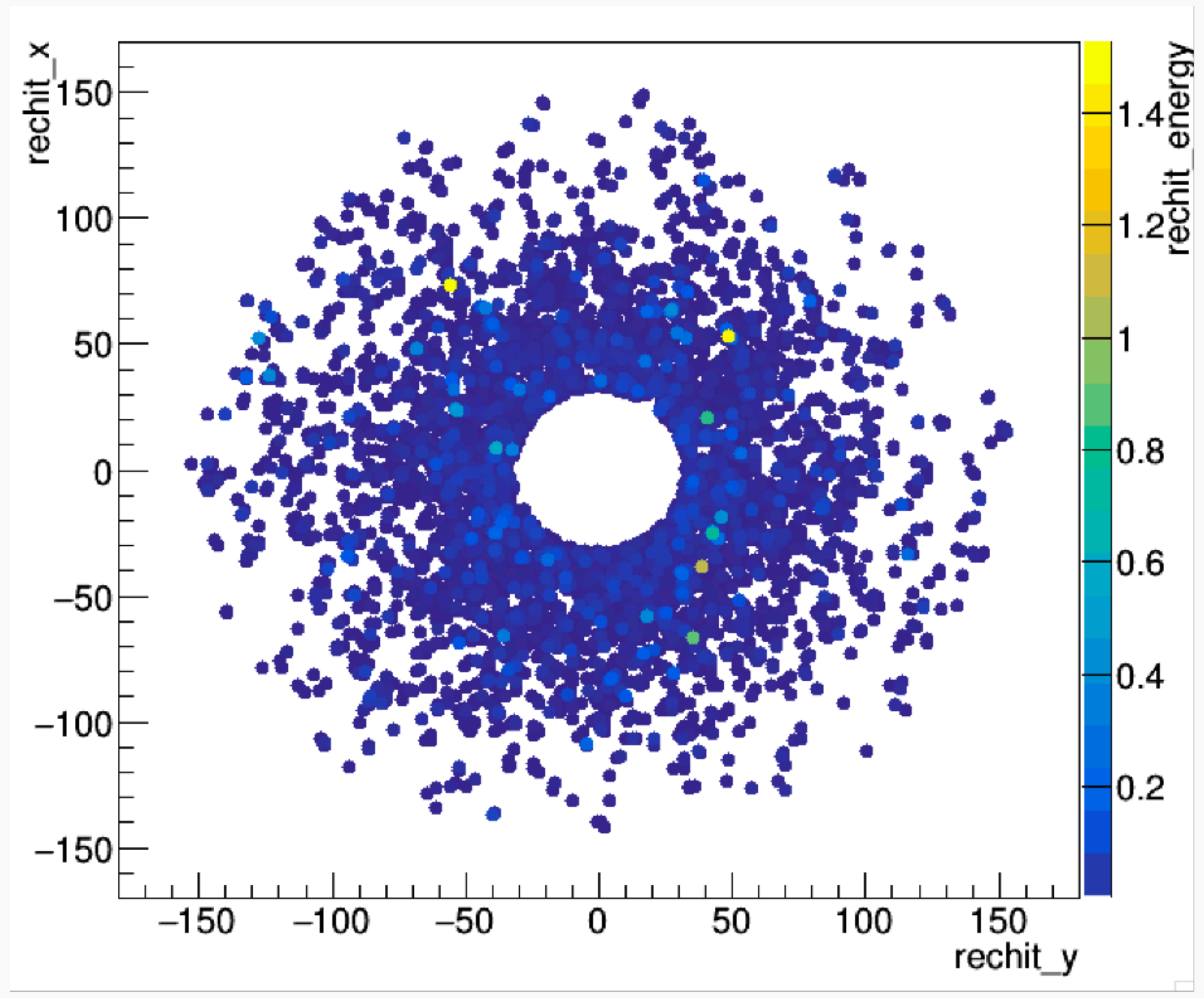


Si+Sci mixed cassette

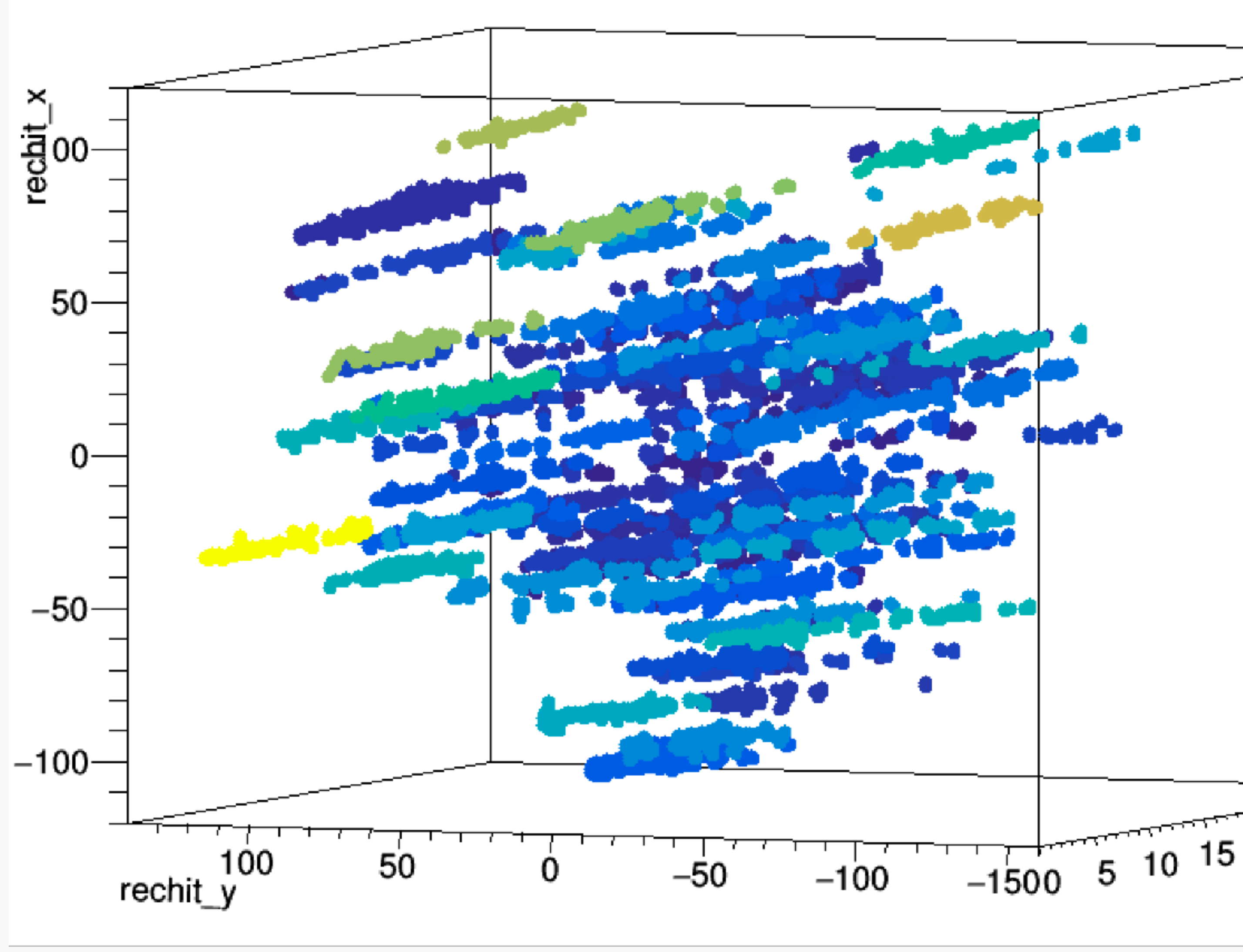
PHYSICS PERFORMANCE

PHYSICS PERFORMANCE

- The high occupancy and pileup are both big challenges for the particle reconstruction
  - But HGCAL is an 5D imaging calorimeter: 3D position, energy and time
    - ➤ Ultimate detector to perform Particle Flow
- The very first step is the clustering of the hits. Currently, the clustering is done in two steps:
  - 2D clustering in every layer using an energy density-based imaging algorithm
  - 3D clustering in an IP-pointing cylinder
- Great opportunity for novel tracking, clustering and imaging techniques as DBSCAN and CNNs!



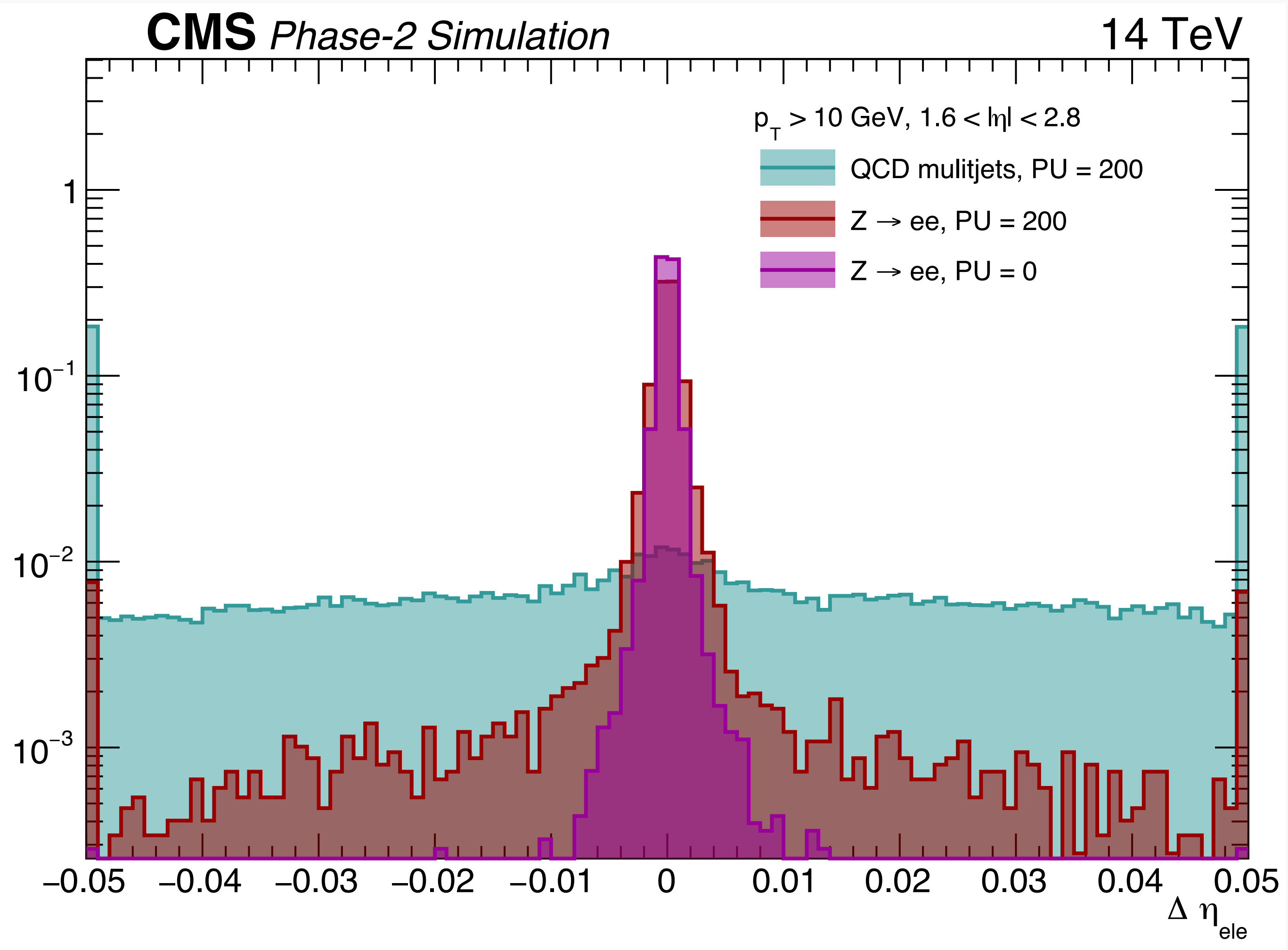
All hits in layer 1 for a 200 PU event



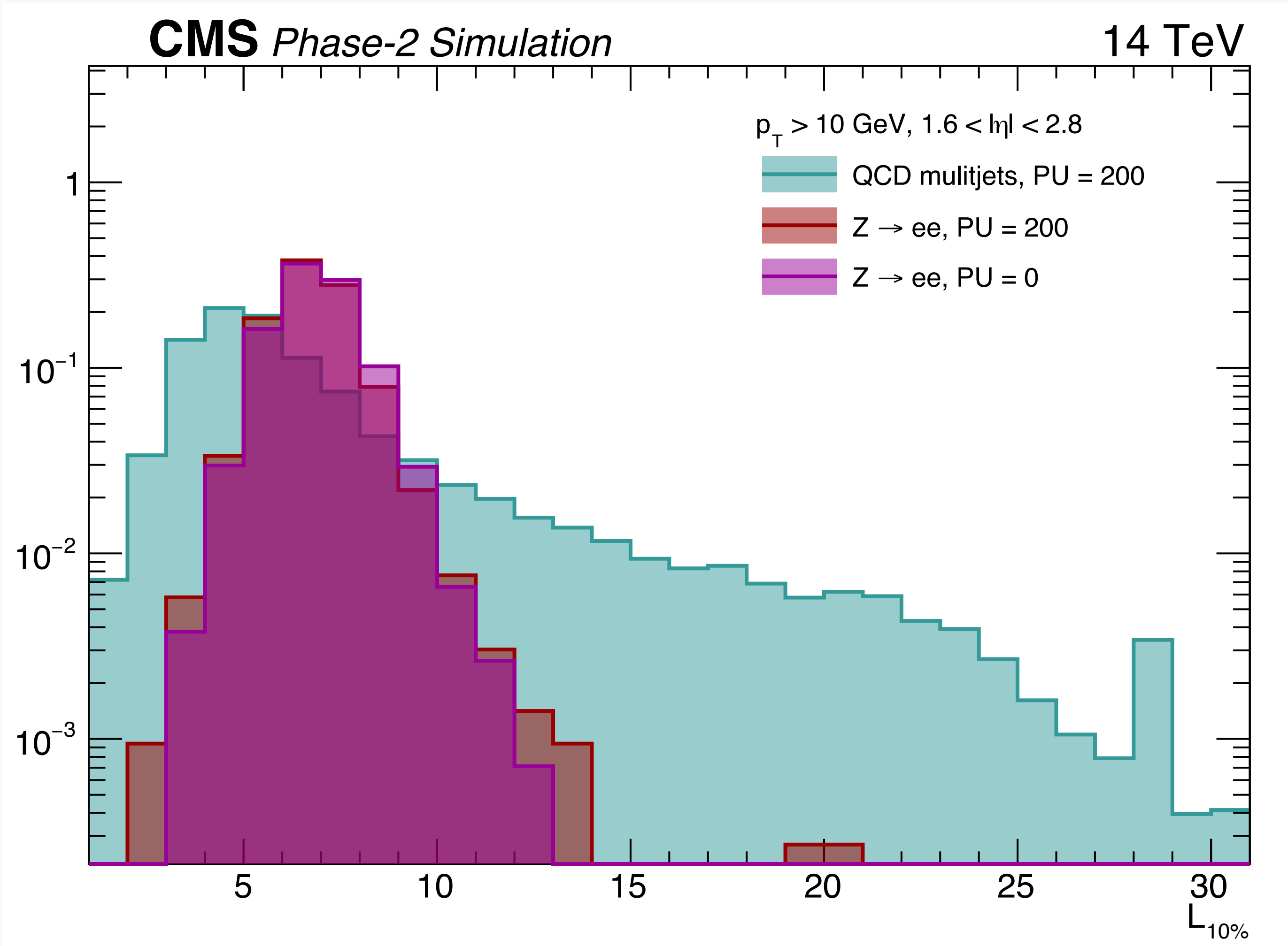
Clustered hits for clusters with pt > 1 GeV

ELECTRON IDENTIFICATION

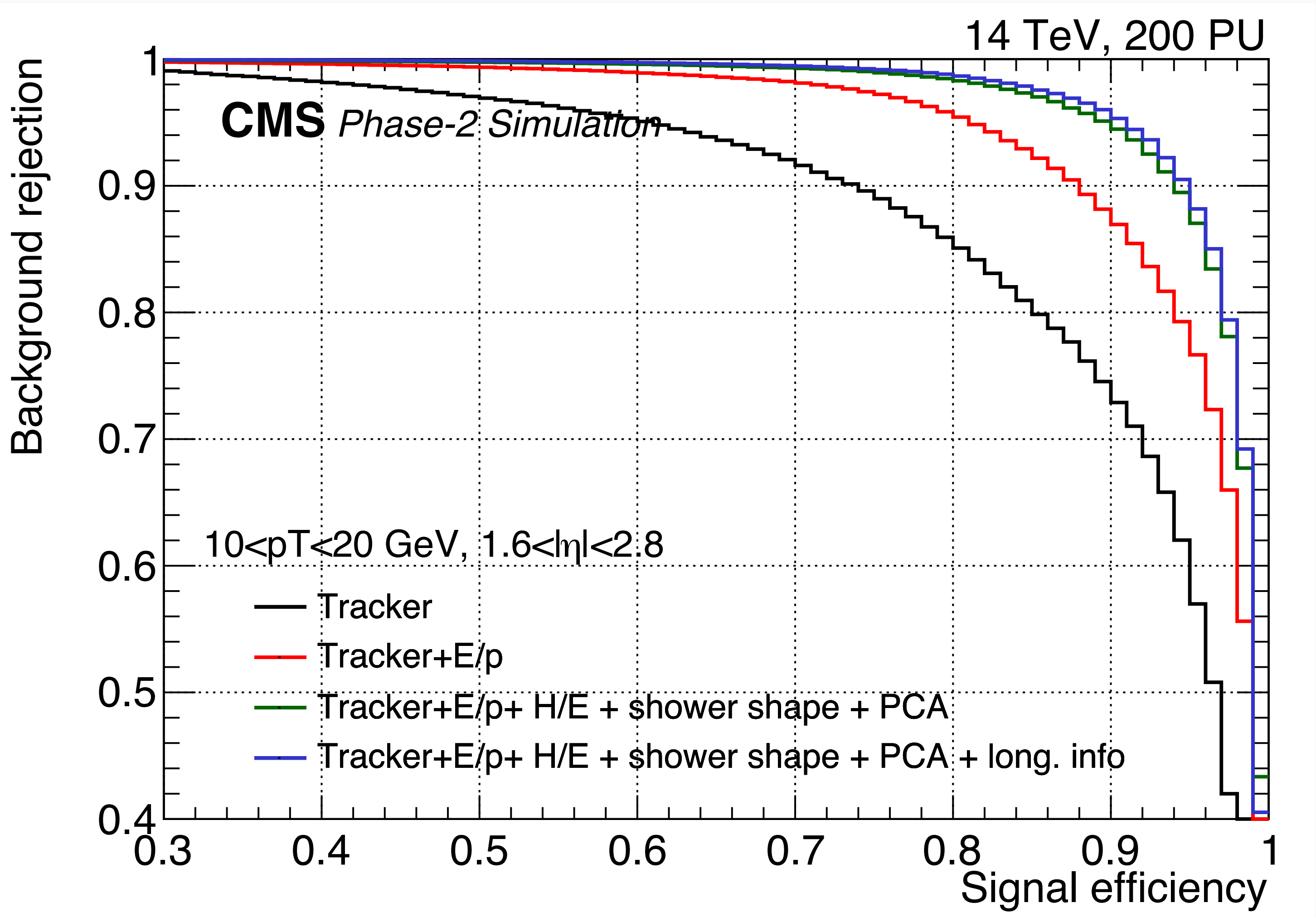
- Electrons are a ‘standard candle’ for Particle Flow:
  EM showers are compact ($R_{Moliere}$ ~ 3 cm), of known shape and associated with a track
  - 3D information allows reconstruction of the shower axis (e.g. using Principal Component Analysis) and the measurement of shower shapes with an unprecedented precision
  - Axis pointing improves rejection of PU photons with respect to bremsstrahlung



Track-cluster deltaEta



First layer with 10% energy fraction

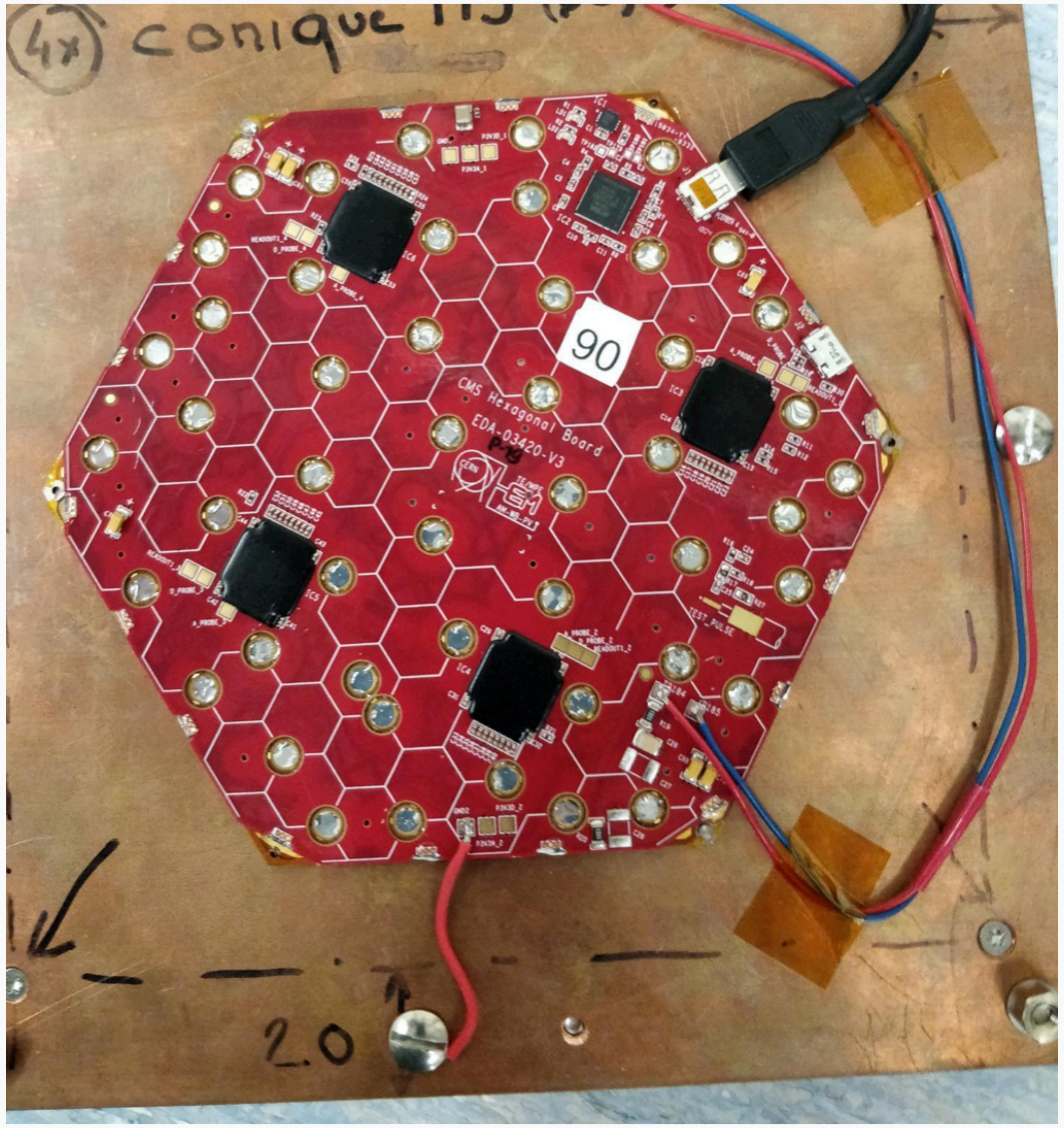


Electron ID for p_T in 10-20 GeV

BEAM TESTS

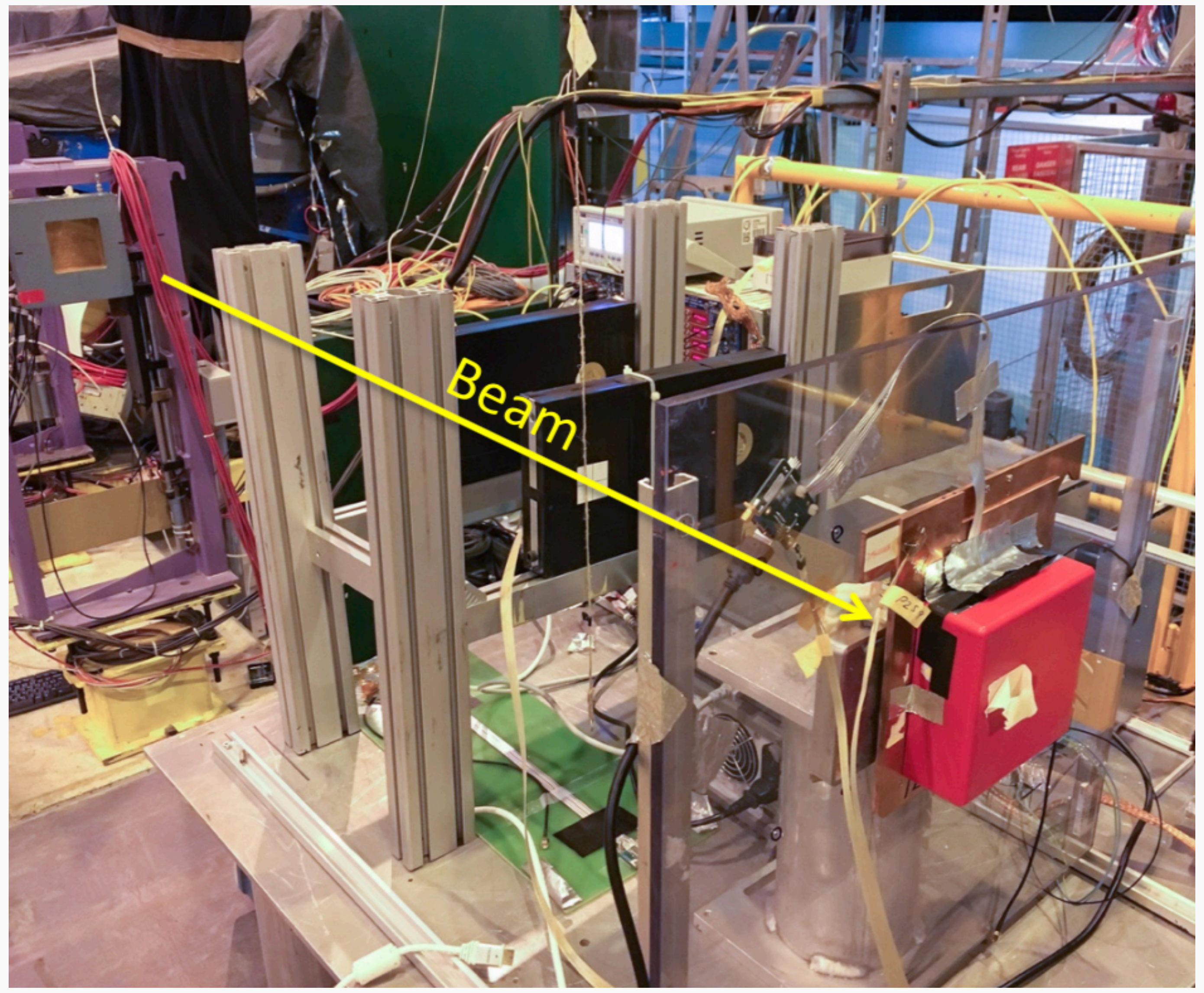
BEAM TESTS

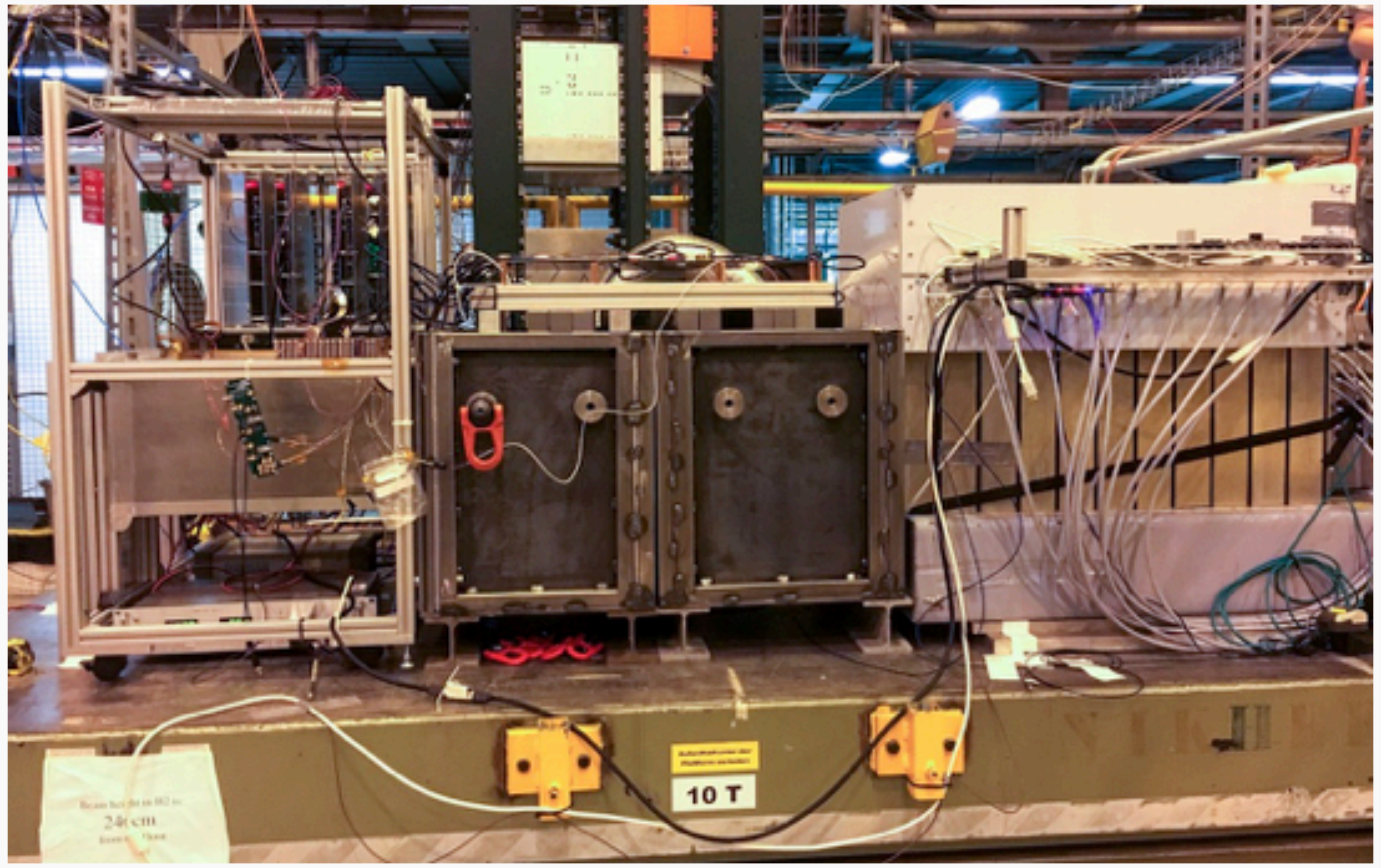
- Several beam tests performed in 2016-2018
- Main objectives for beam tests:
  - Physics performance of the CE-E and CE-H silicon / scintillator parts
  - Verification of the MC simulation
  - Validation of basic FE ASIC architecture in beam conditions: TOT and TOA
  - Technological prototyping of the detector modules
  - System test development in parallel

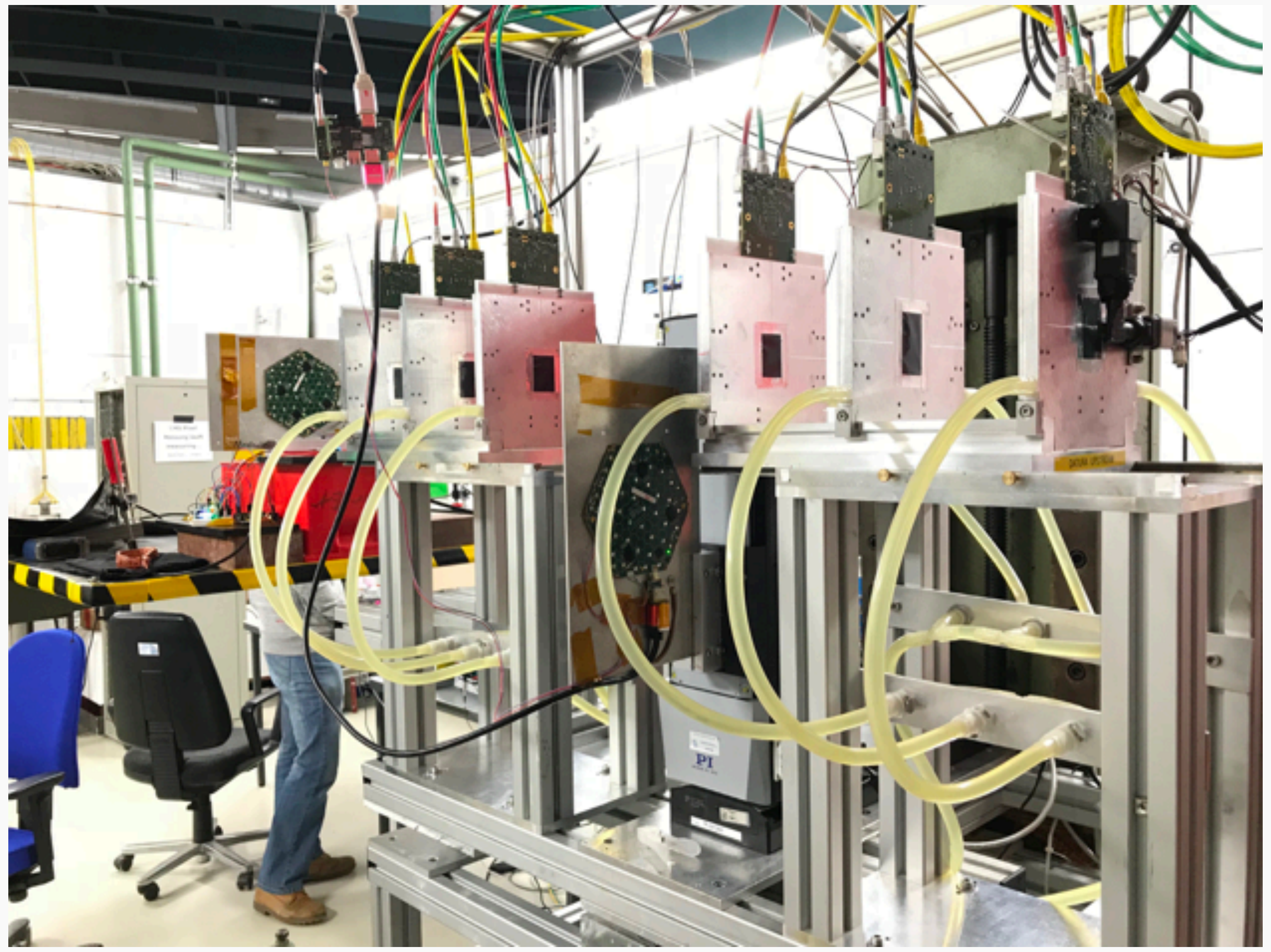


6” hexagonal silicon module prototype

BEAM TESTS 2017-2018







May 2017 @ CERN

- "Commissioning" of new module, ASIC and DAQ
- Development of new DAQ SW
- New signal reconstruction
- ➡ Proof-of-concept of new HGCAL test beam setup

July 2017 @ CERN

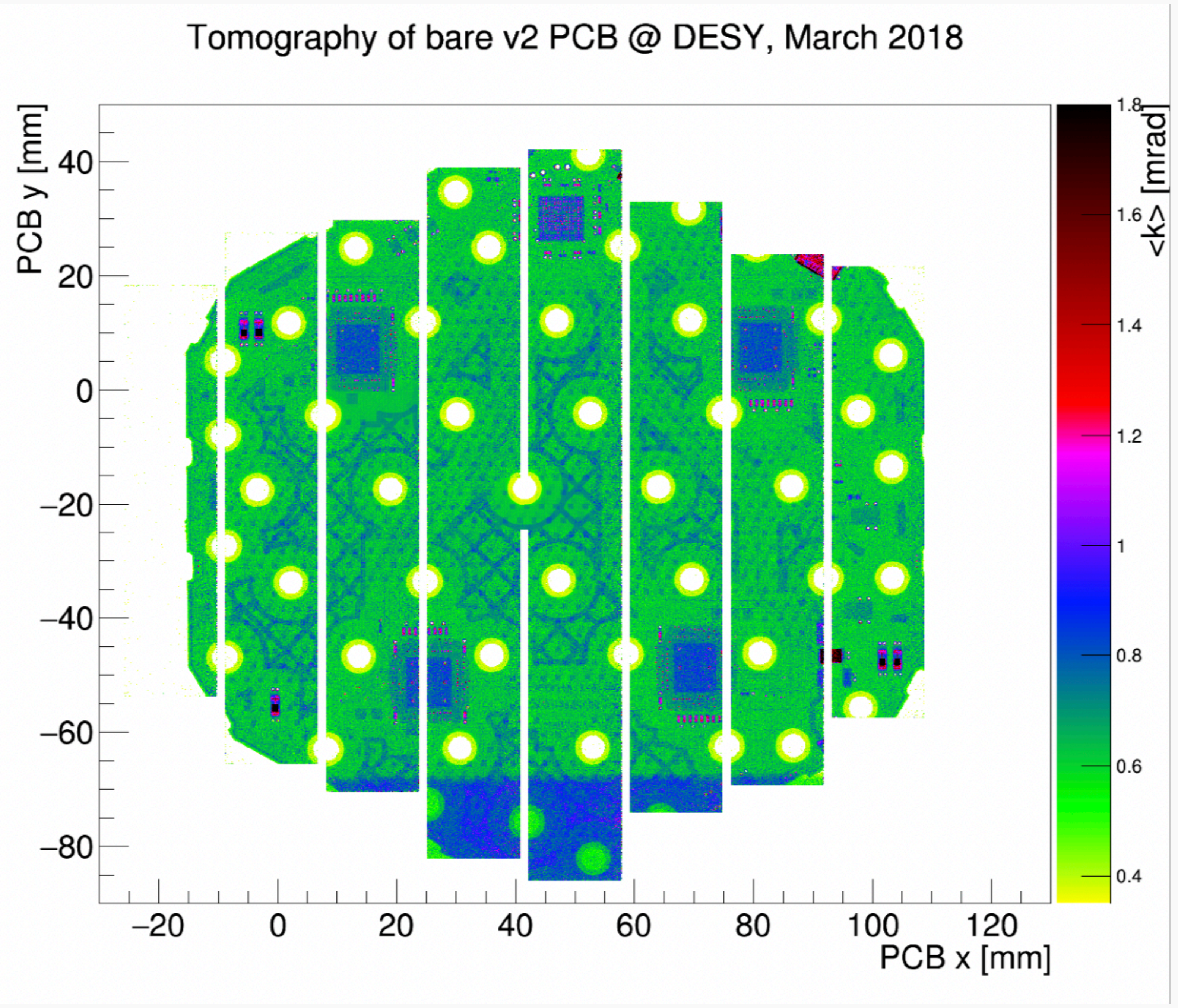
- First large-scale setup with silicon CE-E, CE-H (total: 10 modules)
- CALICE AHCAL with 12 layers to represent BH from Technical Proposal (CE-H)
- Validation of combined data taking and CE-H-Si setup with 7-module layer

March 2018 @ DESY

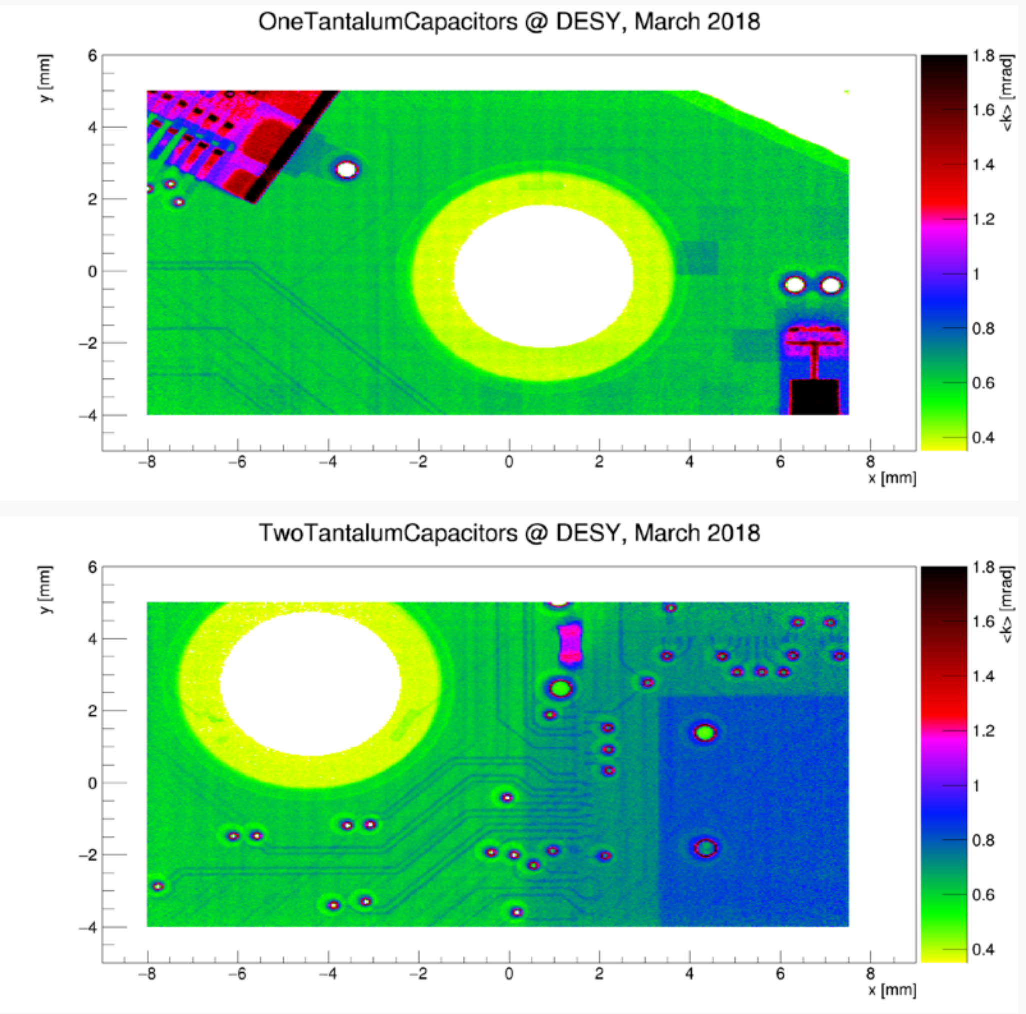
- Studies of single module response using low energy electrons (≤6 GeV)
- "Tomography" of module PCBs
- AIDA beam telescope for precision tracking (σxy ~ 10 μm)

DESY: SIGNAL EFFICIENCY

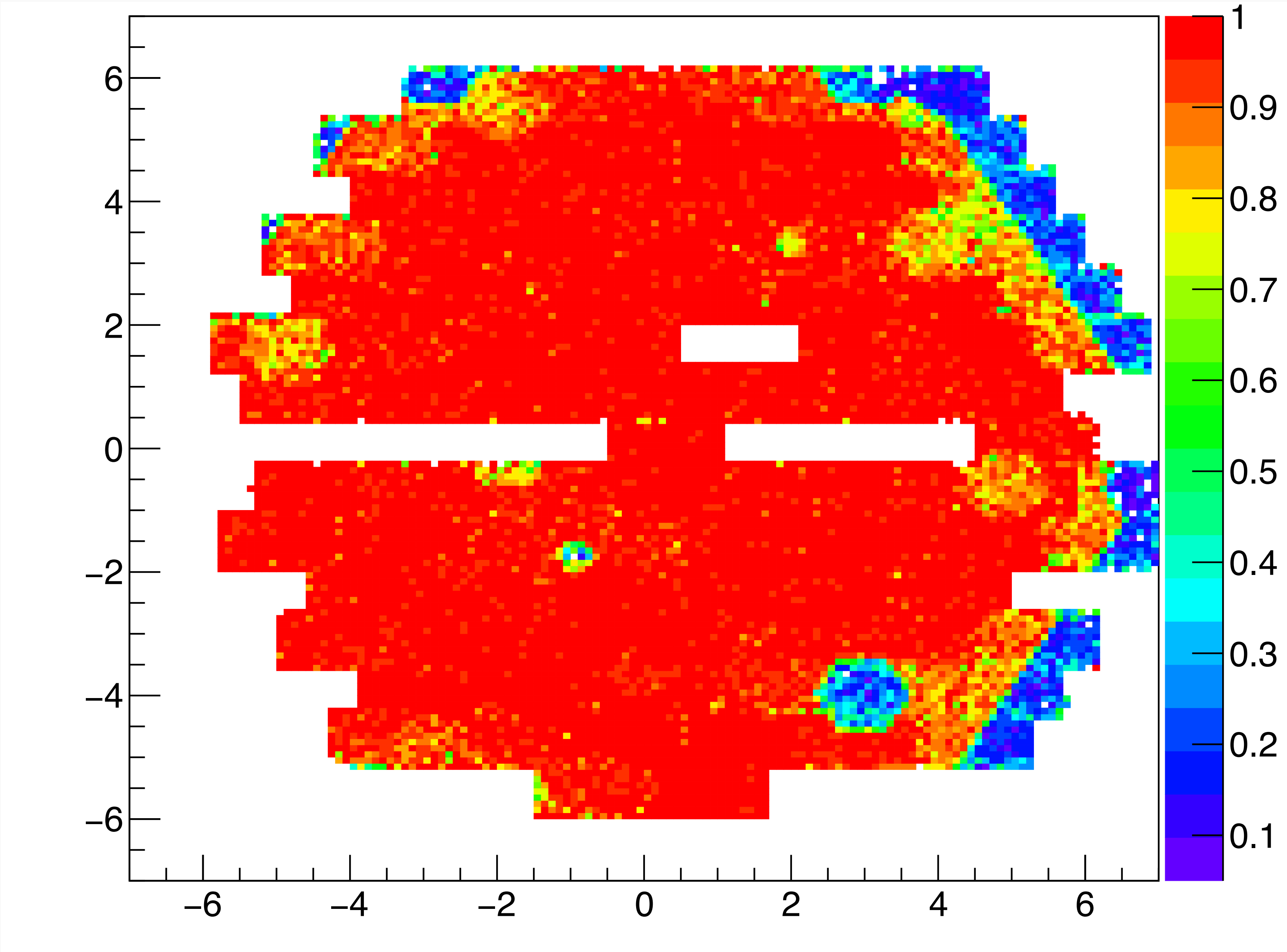
- **Tomography** to **verify the telescope** tracking and **estimate PCB material budget**
- Measure MIP/signal efficiency with external tracking from DWC
  - In order to study the impact of inter-cell gaps (10-40um) on signal efficiency
- **Efficiency** measured at DESY and CERN agrees and **compatible with 100%**



<Track kink angle> ~ material budget



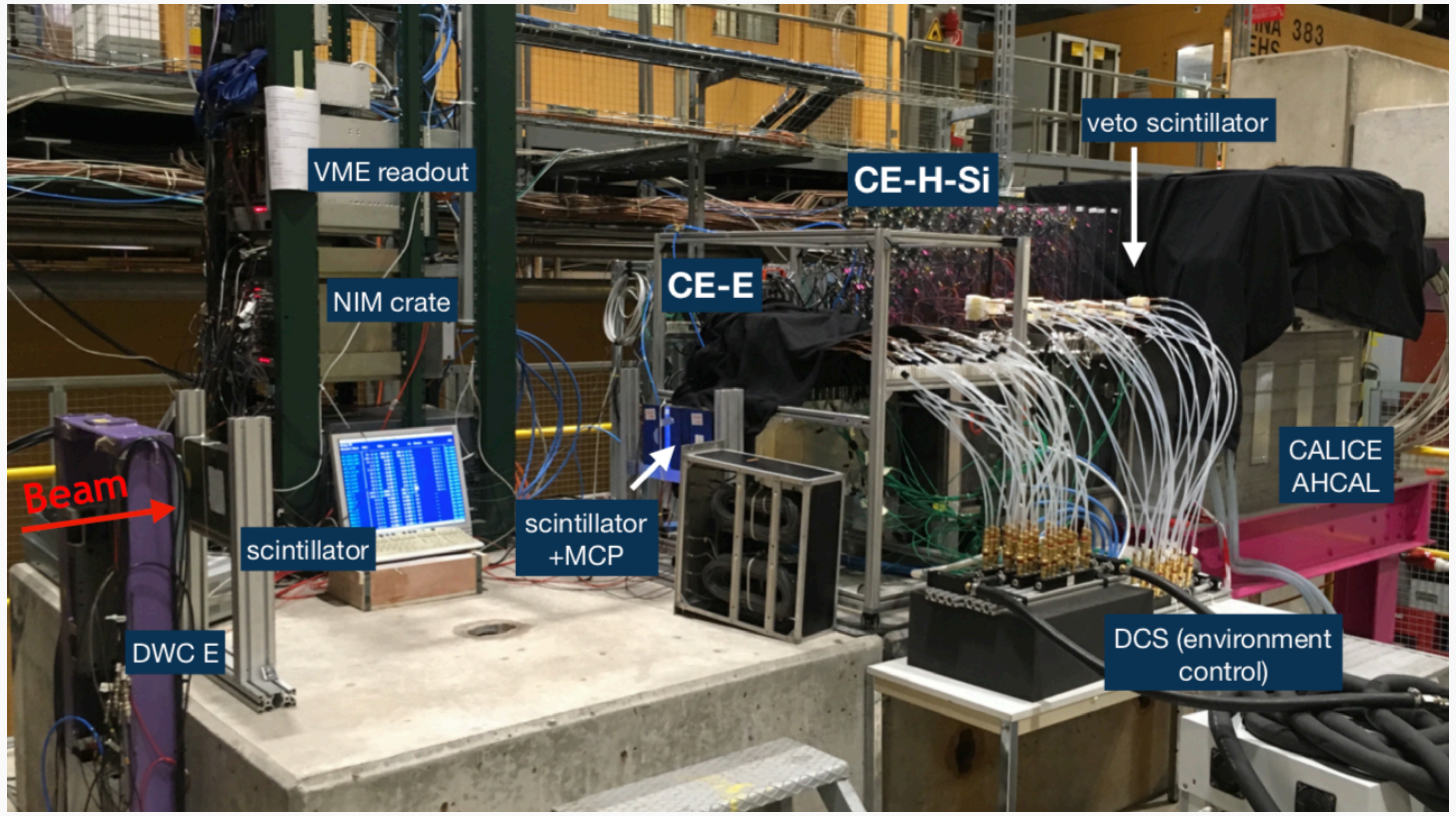
Tomography: details of the PCB visible due to good track resolution (10 µm)

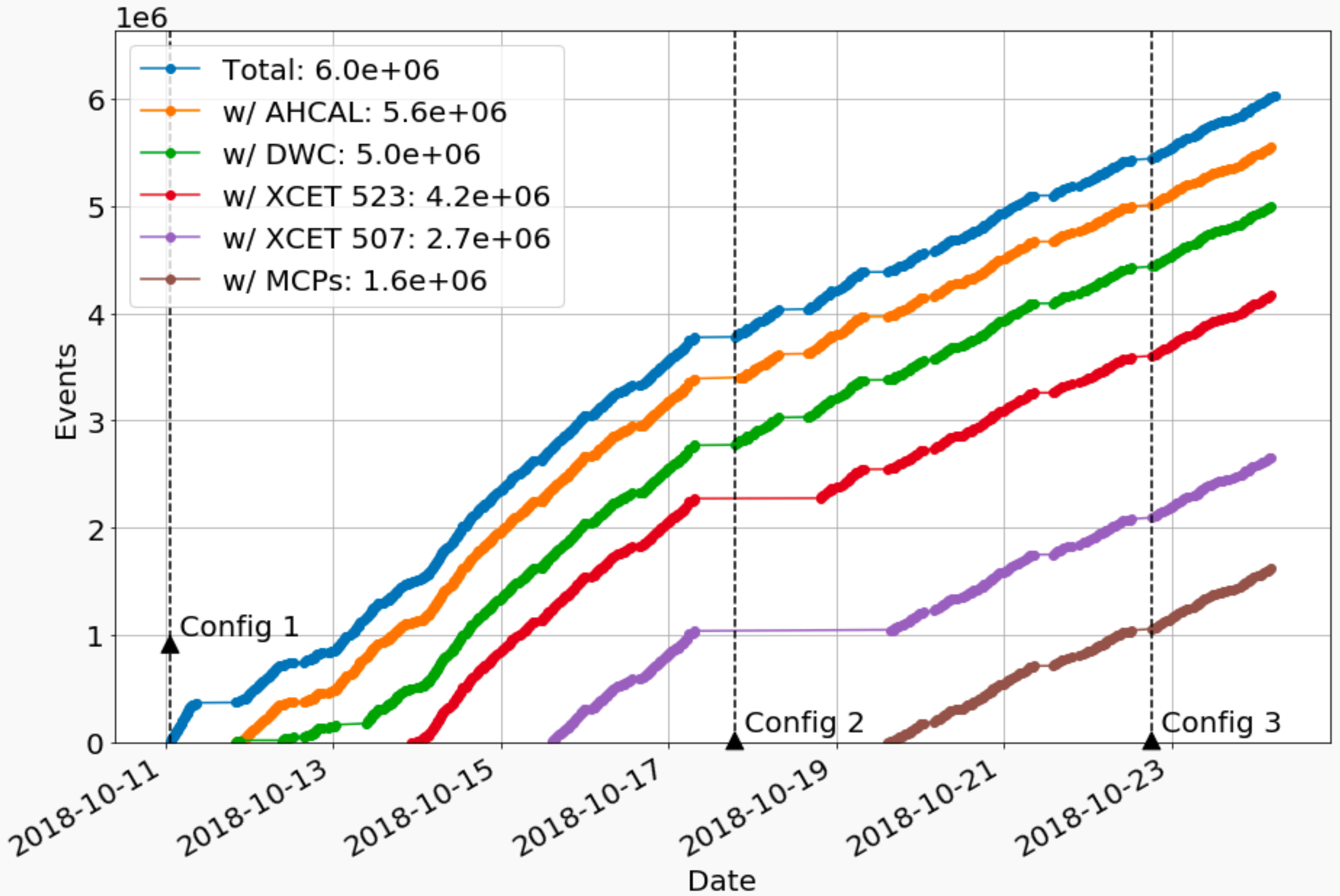


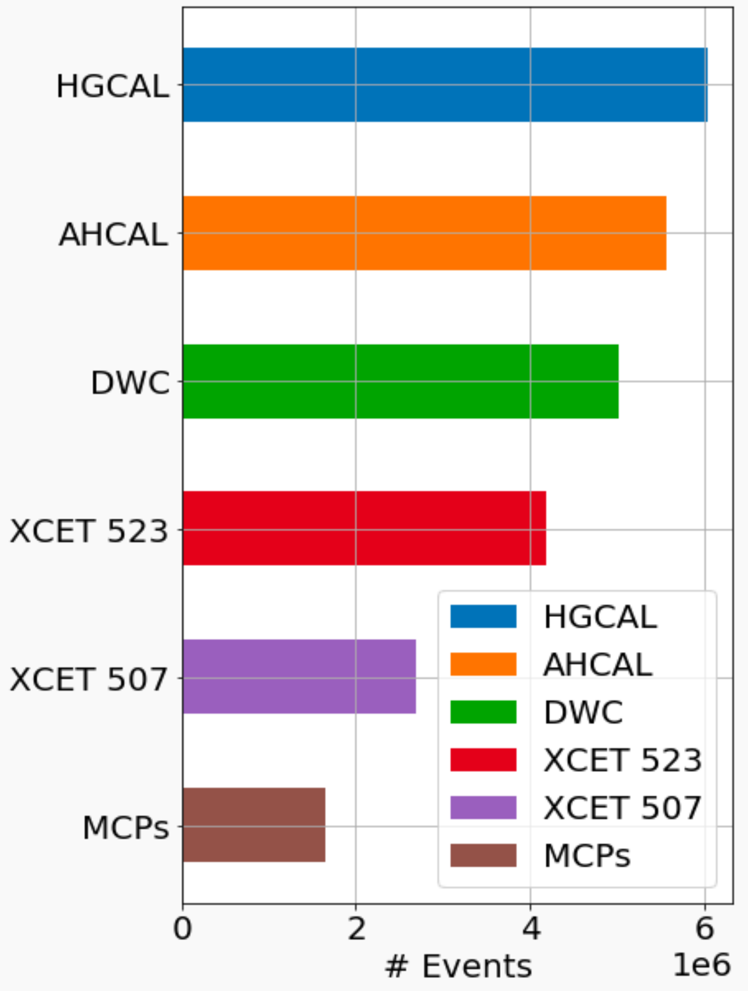
"MIP" signal efficiency ~100%

OCTOBER 2018 TEST BEAM

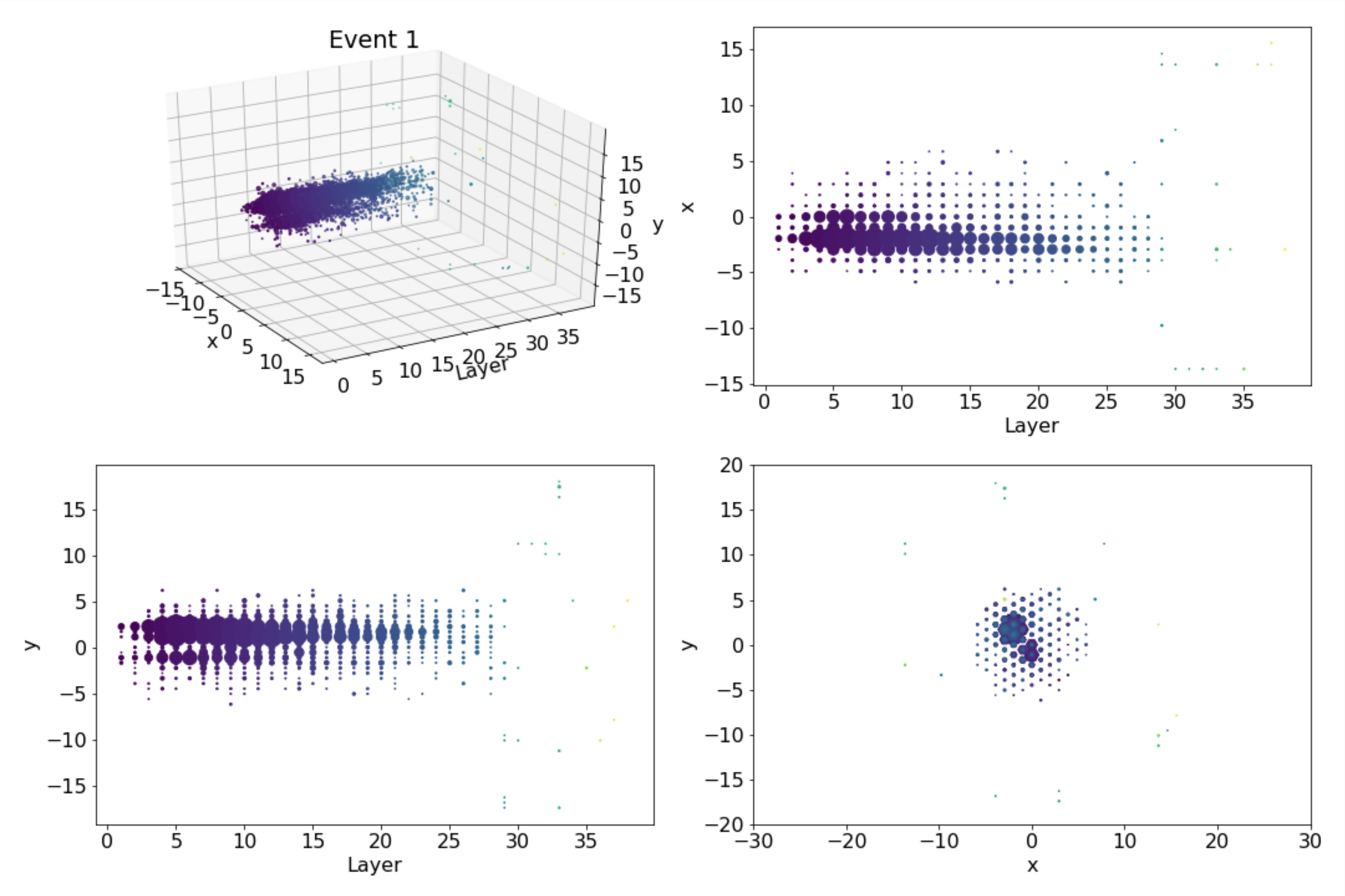
- 28-layer CE-E setup from June + 12-layer CE-H-Si setup (total: 94 modules)
  - 3 configurations (full CE-E vs full CE-H)
  - Bias, current and environmental control, active water cooling (same as in June)
  - Delay Wire Chambers, threshold Cherenkov counters, MCP-PMTs for timing reference
  - CALICE AHCAL as scintillator CE-H
  - Trigger: 2x scintillators in front of CE-E + 1x additional (veto) behind CE-H-Si
- Beams: μ and e, π up to 300 GeV
  - ➡ **Large-scale test of O(100) HGCAL modules**
    More than 6 million events recorded!



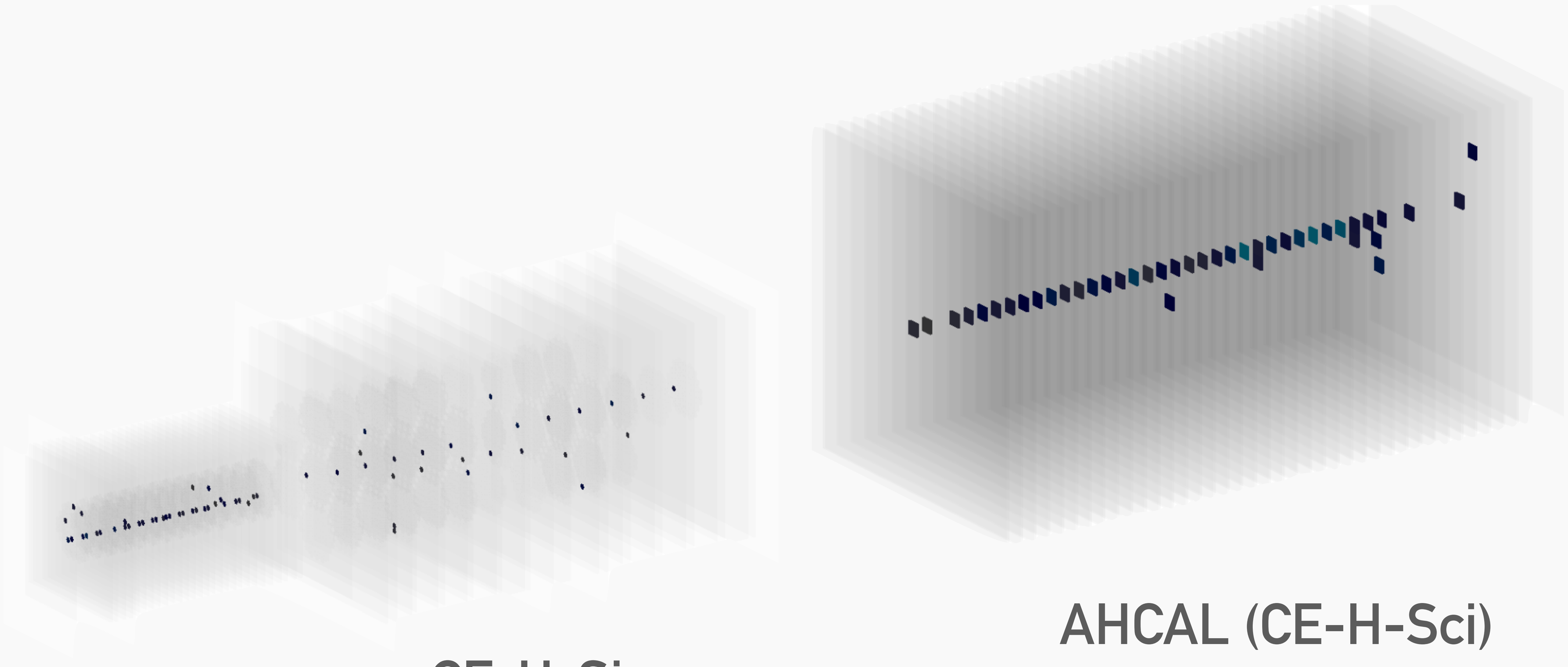




OCTOBER 2018 TEST BEAM

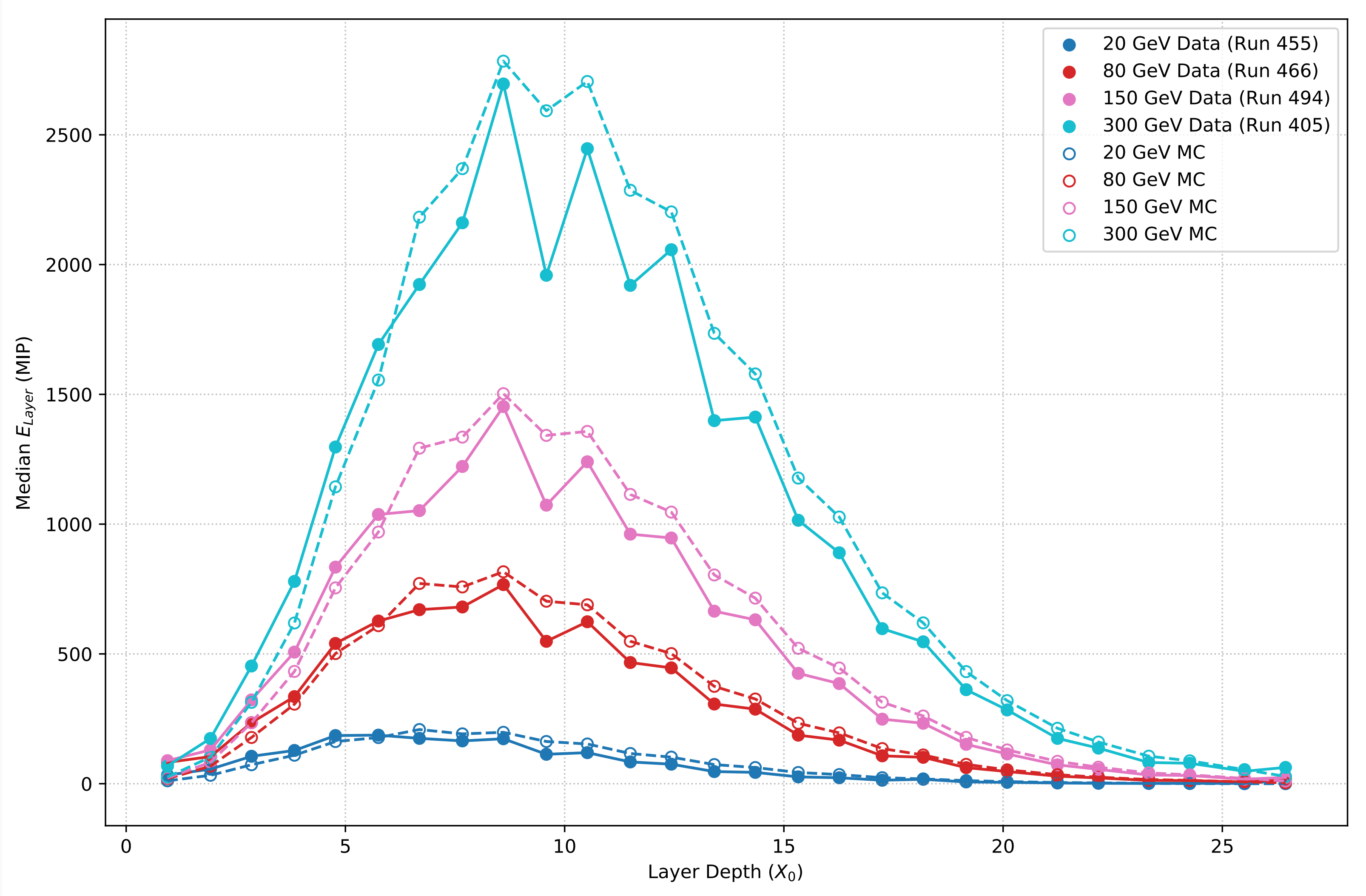


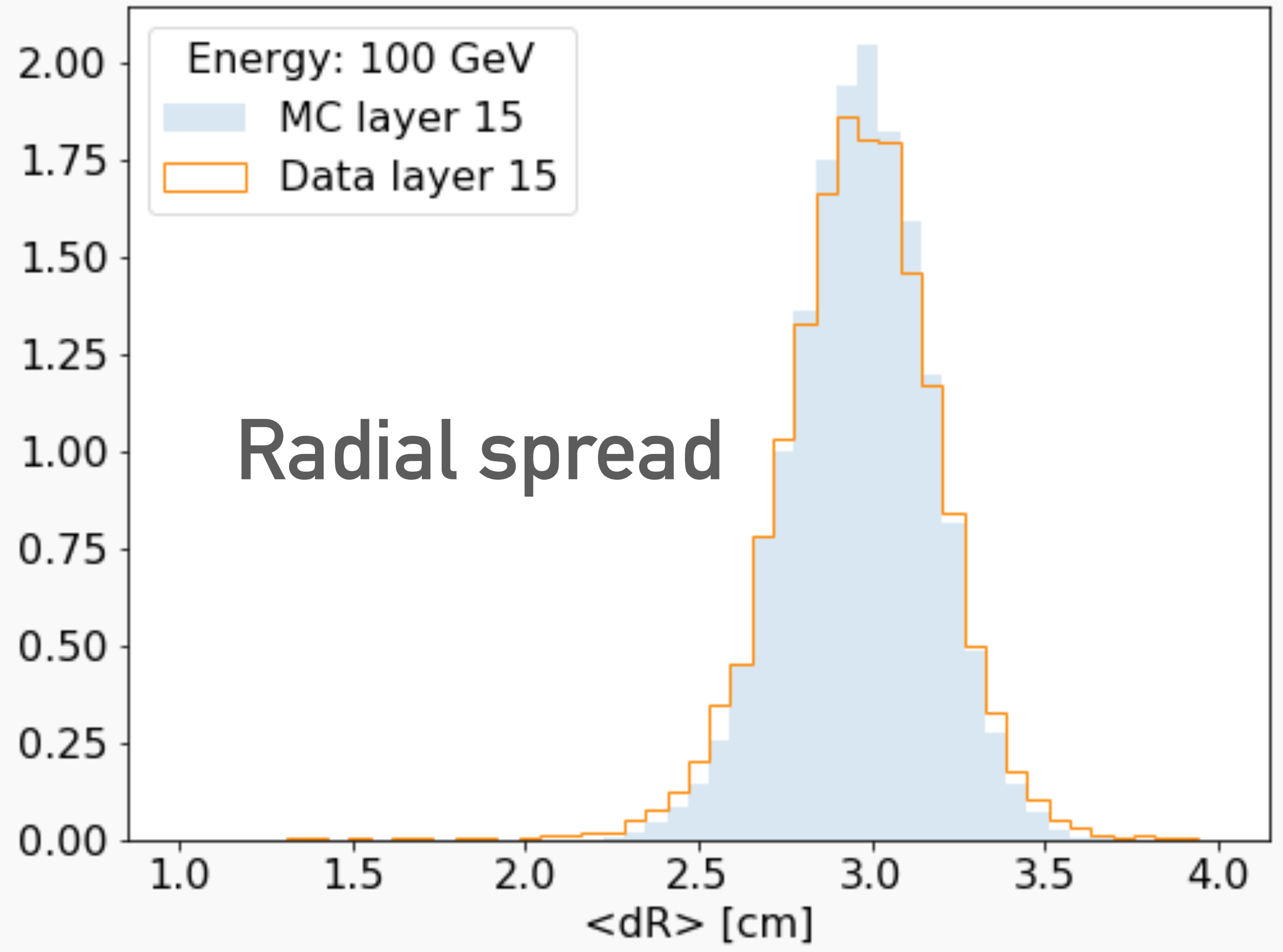
2-component event in
300 GeV electron beam

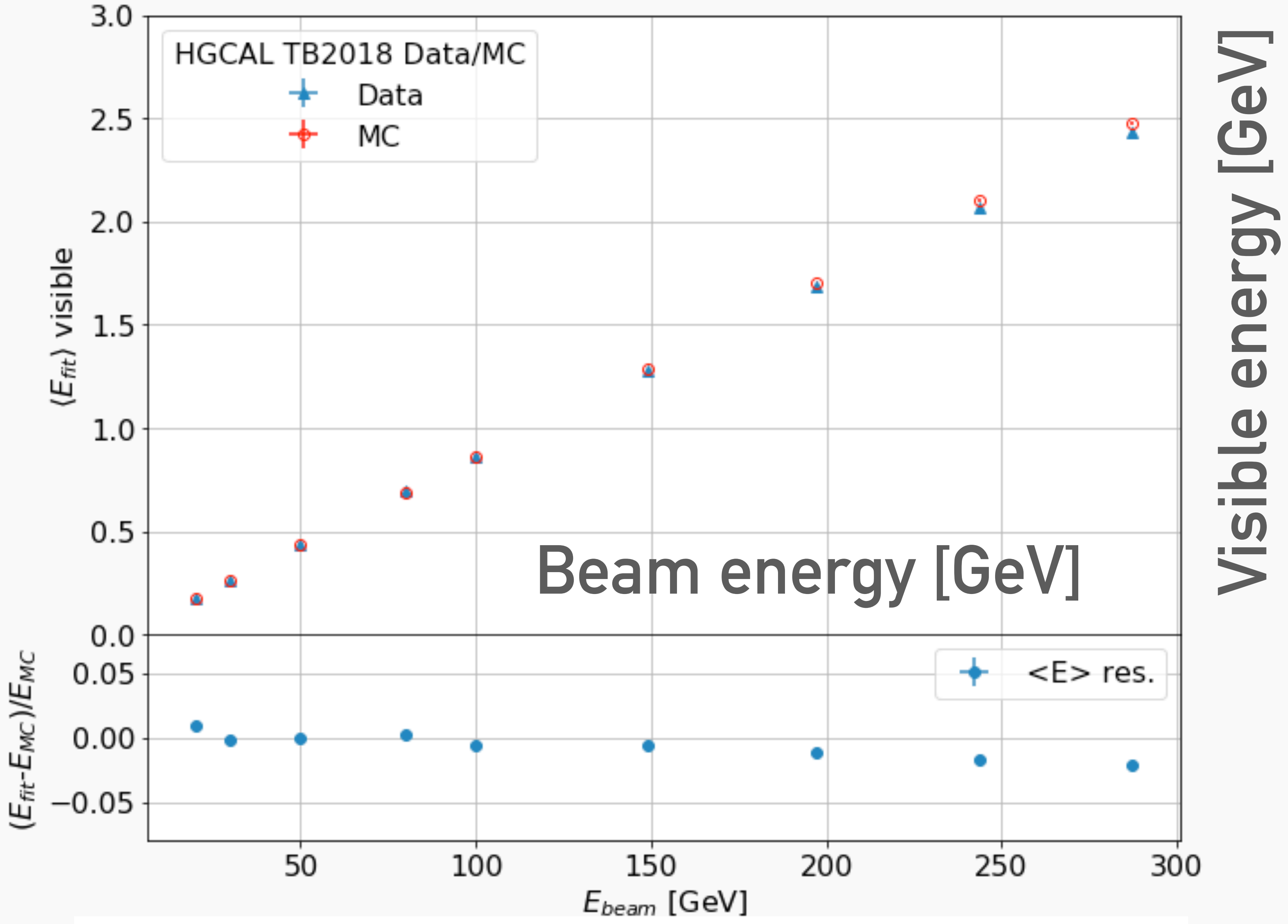


200 GeV Muon

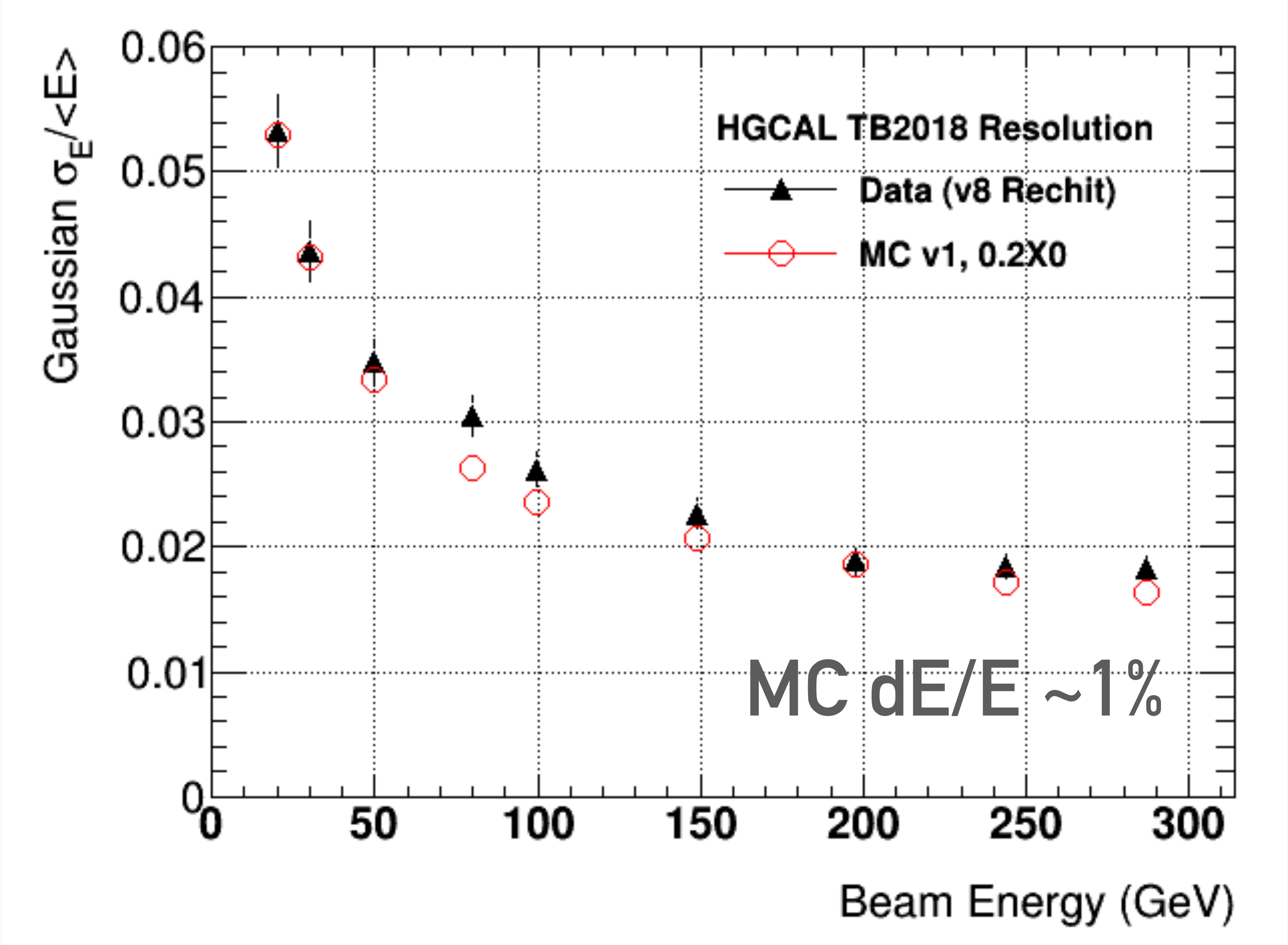
ELECTRONS





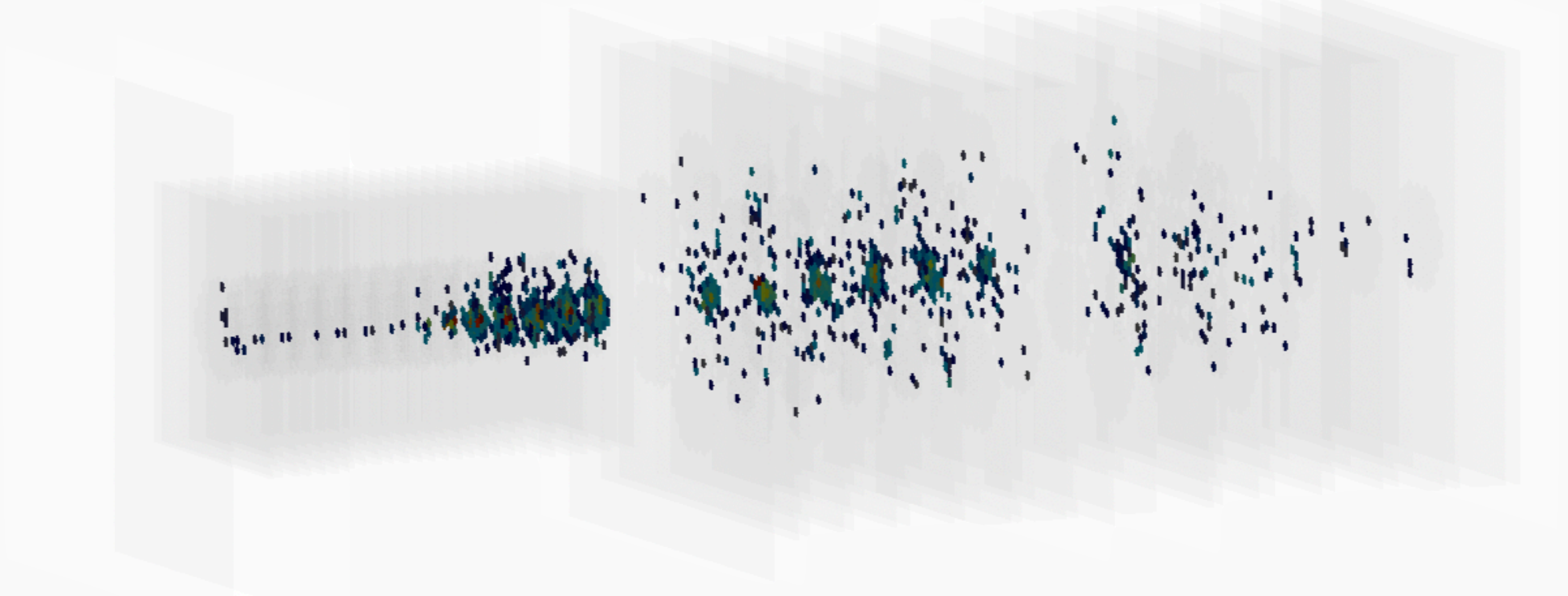


- **Agreement for longitudinal and transverse shower profiles**
  - Long. profile wiggles possible due to back-scattering in CuW
- **Good linearity** in energy response up until 300 GeV
  - Data/MC energy scale difference below 4%
- **Data and MC resolutions agree with TDR expectation**
- Working with SPS scientists to better understand beam line

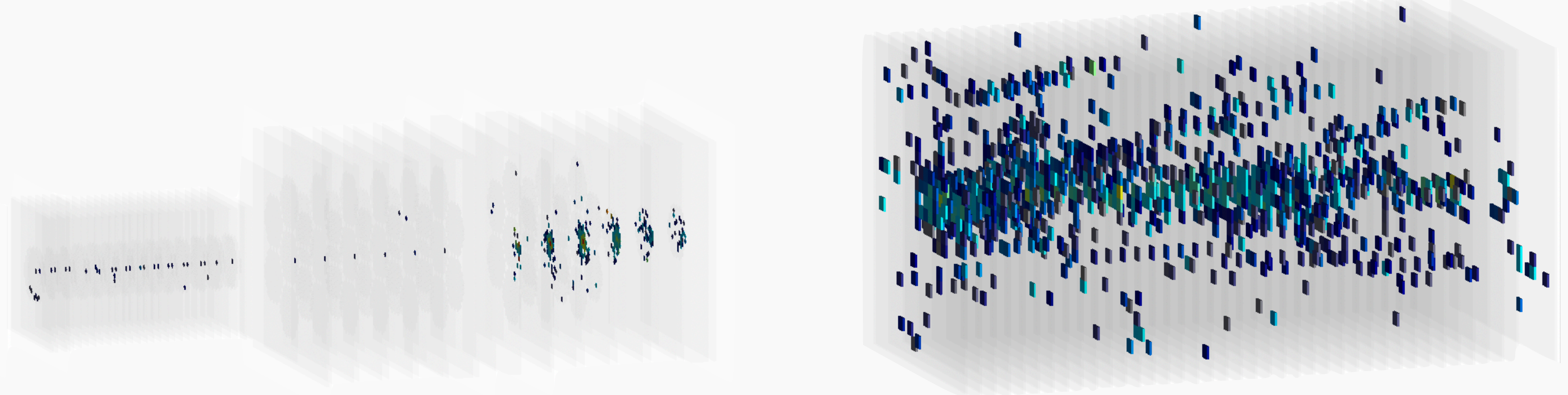


PIONS

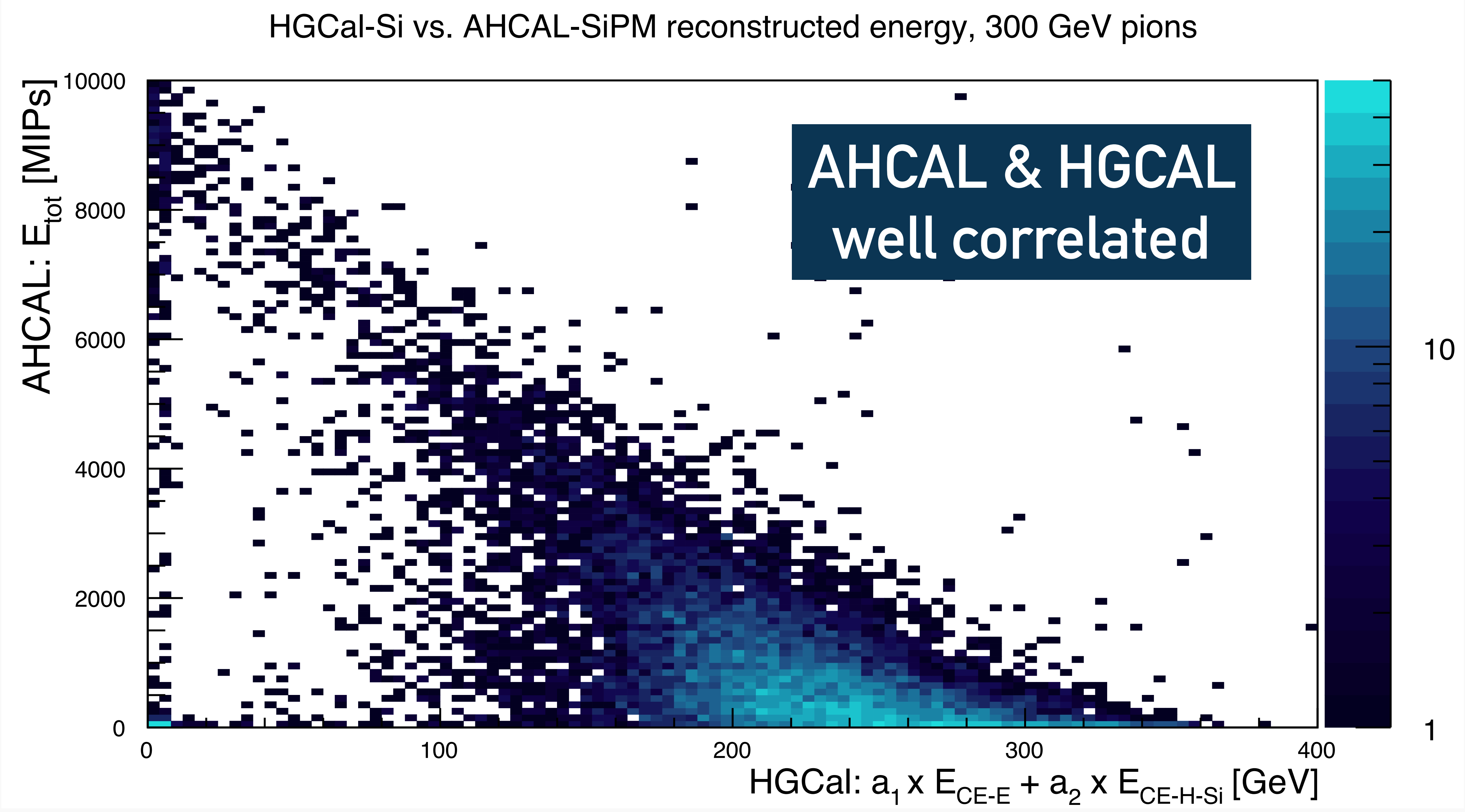
300 GeV pion starting showering in CE-E



300 GeV pion starting showering in CE-H-Si



- **Preliminary** results on pions
  - Studying combination of CE-H, CE-H-Si and AHCAL data
- **Starting AHCAL-HGCAL combination**
  - Event synchronisation ok
  - Good position and energy correlation



SUMMARY

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- CMS High Granularity Calorimeter is a very challenging detector
  - Harsh radiation environment, high pileup & occupancy
  - Large number of channels, low noise, large dynamic range, high speed, low power …

- TDR approved in April 2018: cds.cern.ch/record/2293646
- 5D (3D position + energy + time) measurement of showers provides unique opportunities in particle reconstruction for identification and pileup mitigation
- Test beam campaign help to validate technology and physics performance
- Engineering Design Review to review full design scheduled for early-2021

TB DATA ANALYSIS DEMO

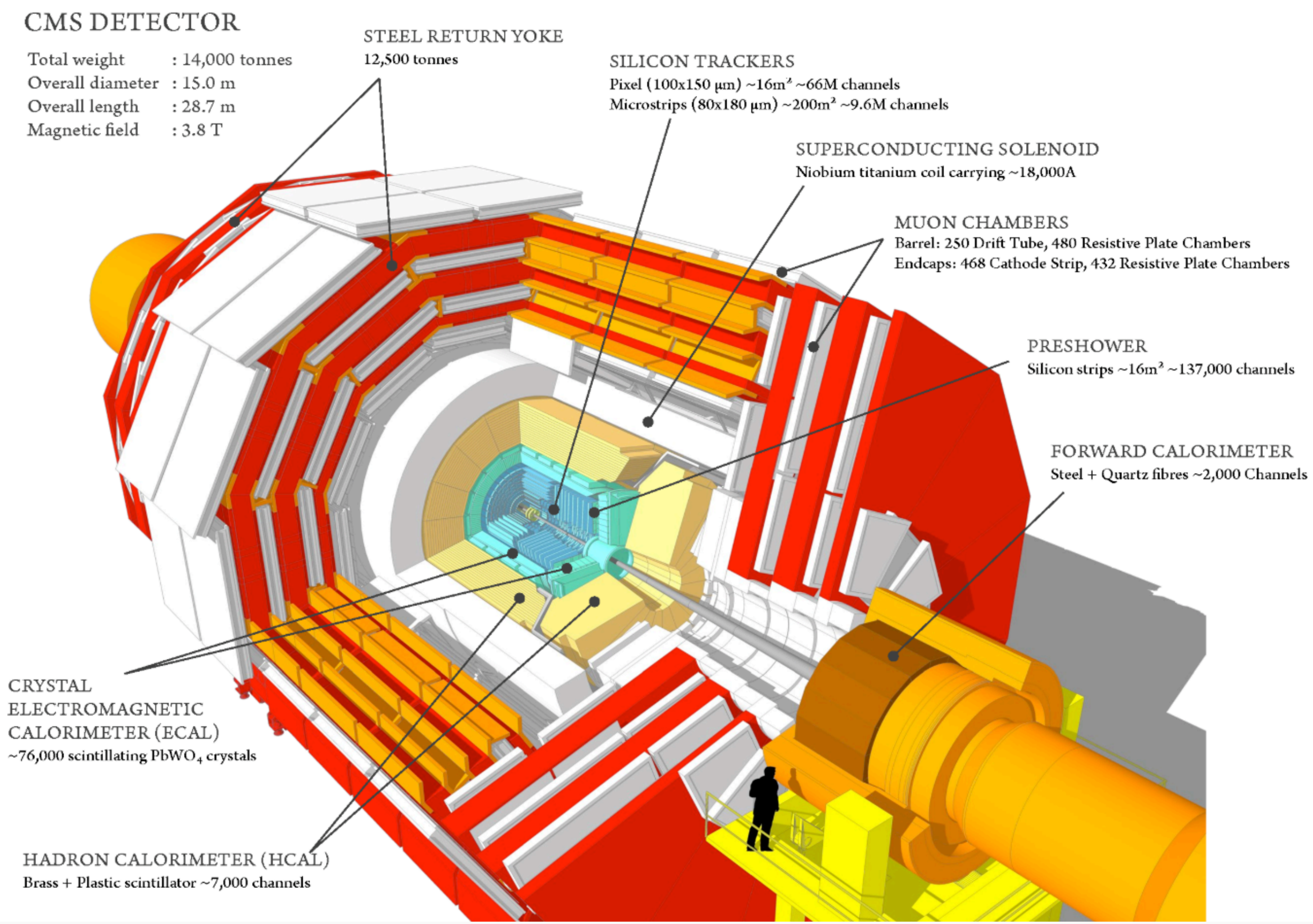
TEST BEAM DATA ANALYSIS WITH PANDAS

- Test beam data processed with CMS software (CMSSW), and then stored in “flat” ROOT TTrees (based on C++):
    - A table of format: row = event , columns = variables
- Many modern frameworks exist, e.g. based on python
    - Numpy — numerical python data structures/arrays
        - Python “outside” wrapping fast C functions “inside”
    - Pandas — wrapper around numpy for easier use
- Several packages allow ROOT —> numpy conversion

- Today: demo of pandas analysis using HGCAL test beam data
    - https://github.com/artlbv/llr-hgcal-seminar

BACKUP

THE CMS DETECTOR



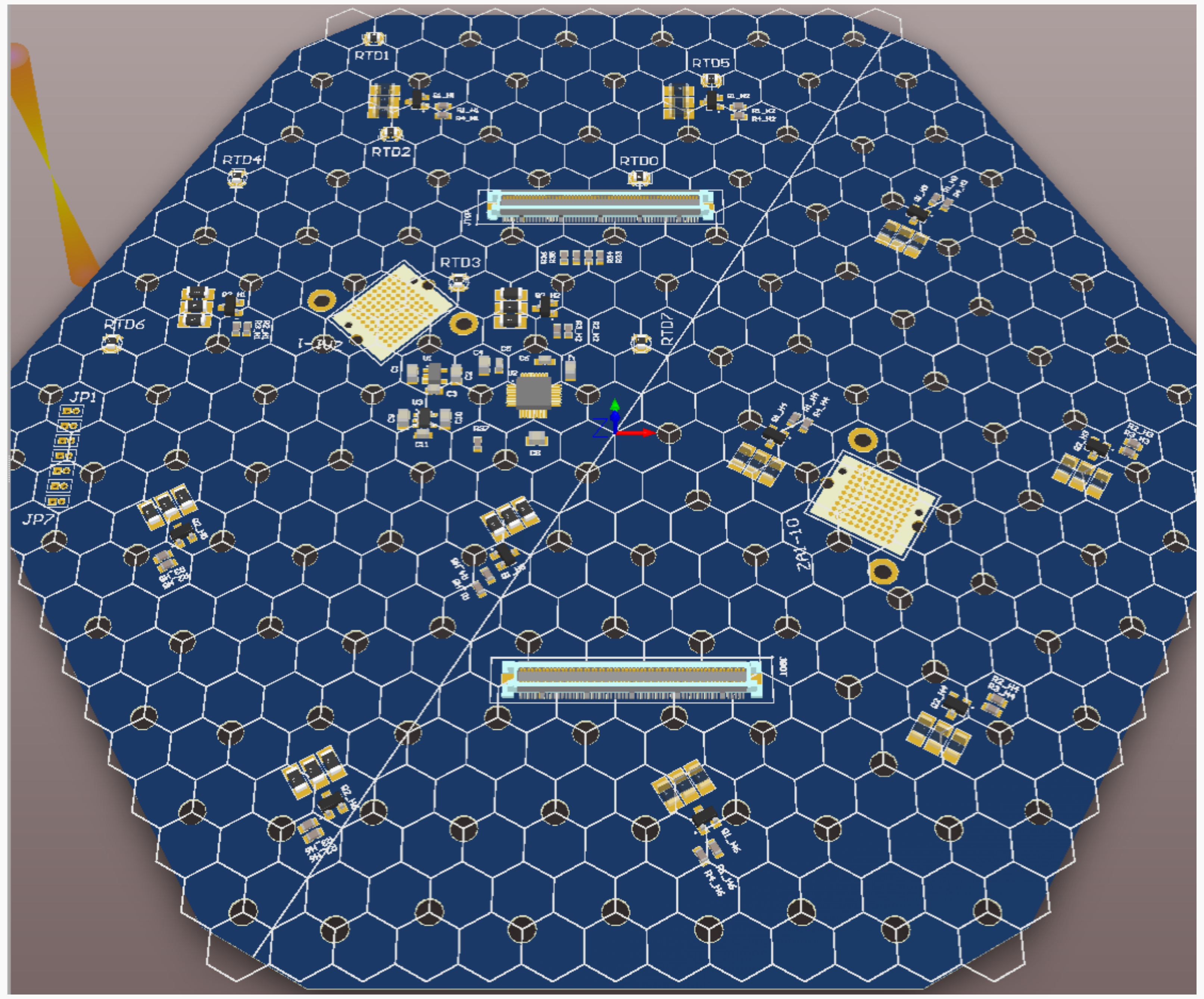
FRONT-END ELECTRONICS

- Detector modules with 2 PCBs <u>< 6mm thick</u>:

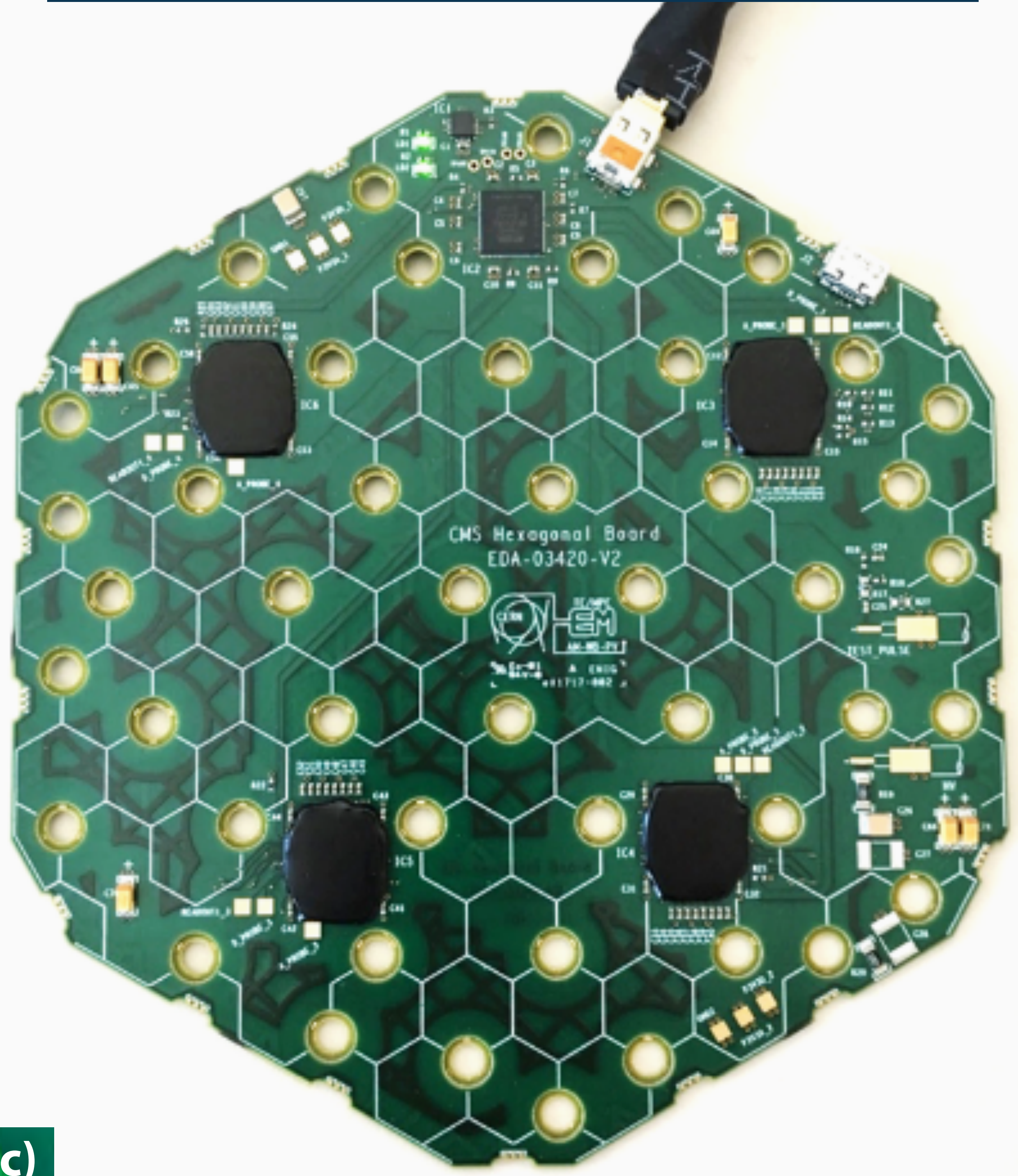
  1. PCB: "hexaboard" Wire-bonds to Si-sensor and very-FE ASICs
  2. PCB: Motherboard for powering, data concentration, trigger generation and bi-directional communication

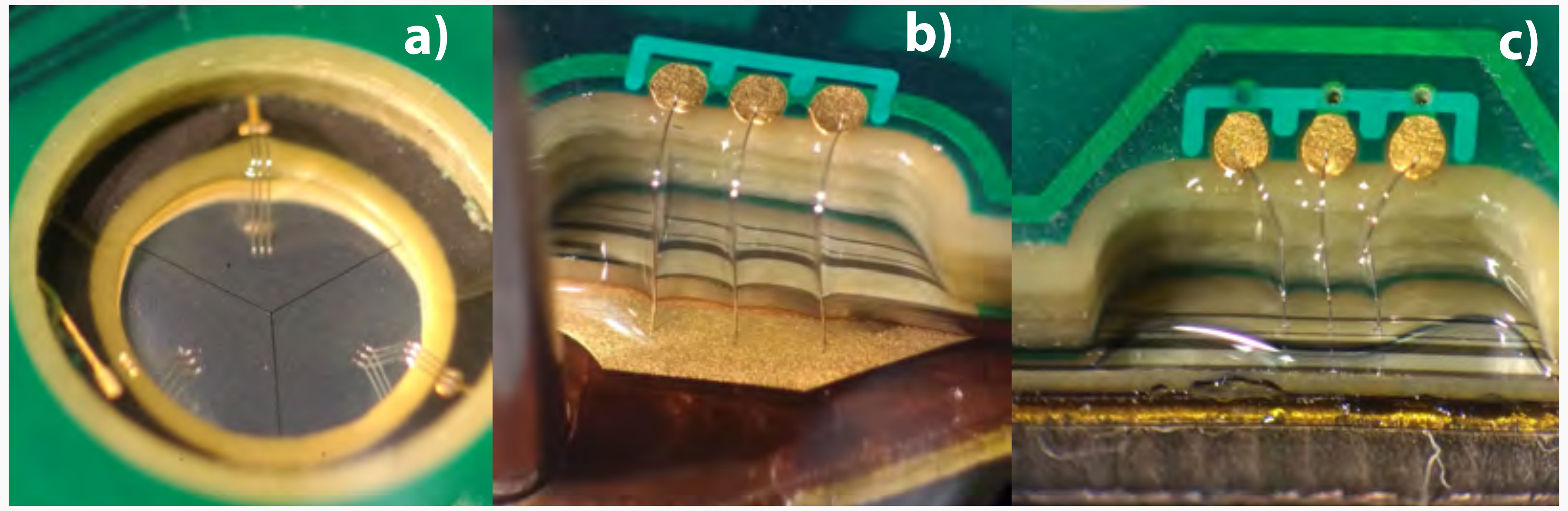
- Trigger/data transfer: low-power GBT links (lpGBT)

Hexaboard design for HGCROC



Hexaboard PCB for Test Beam

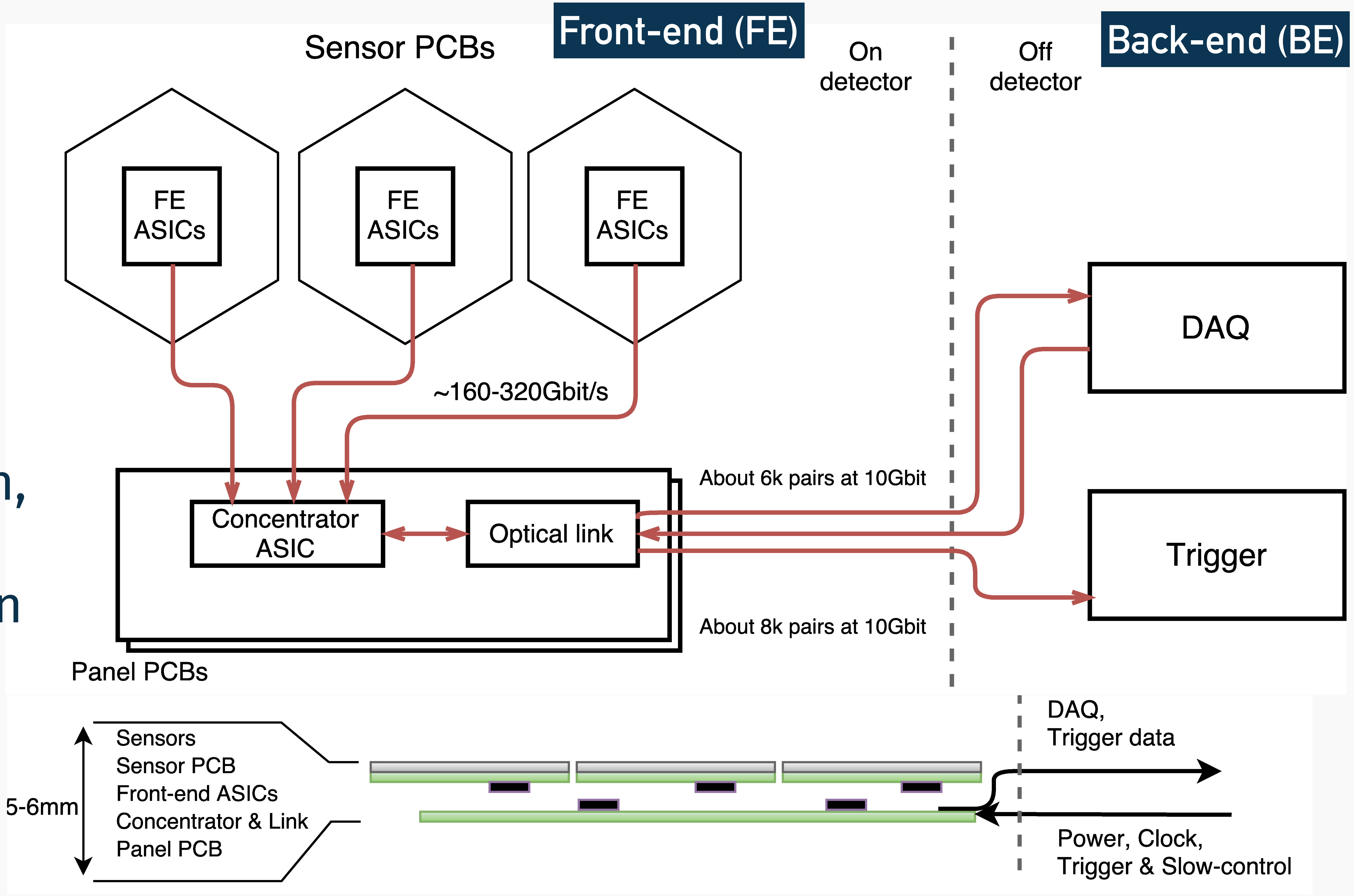




Wire-bonds from Silicon to 1. PCB

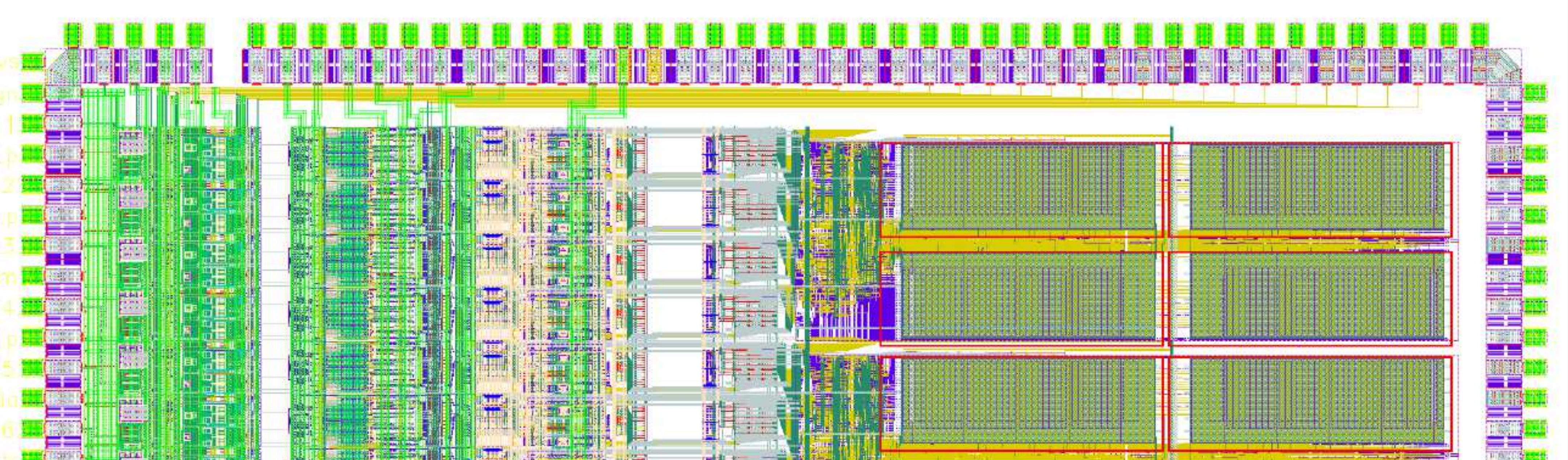
FRONT-END ELECTRONICS

- Detector modules with 2 PCBs <u>< 6mm thick</u>:
    1. PCB: "hexaboard"
       Wire-bonds to Si-sensor and very-FE ASICs
    2. PCB: Motherboard for powering, data concentration, trigger generation and bi-directional communication
- Trigger/data transfer: low-power GBT links (lpGBT)



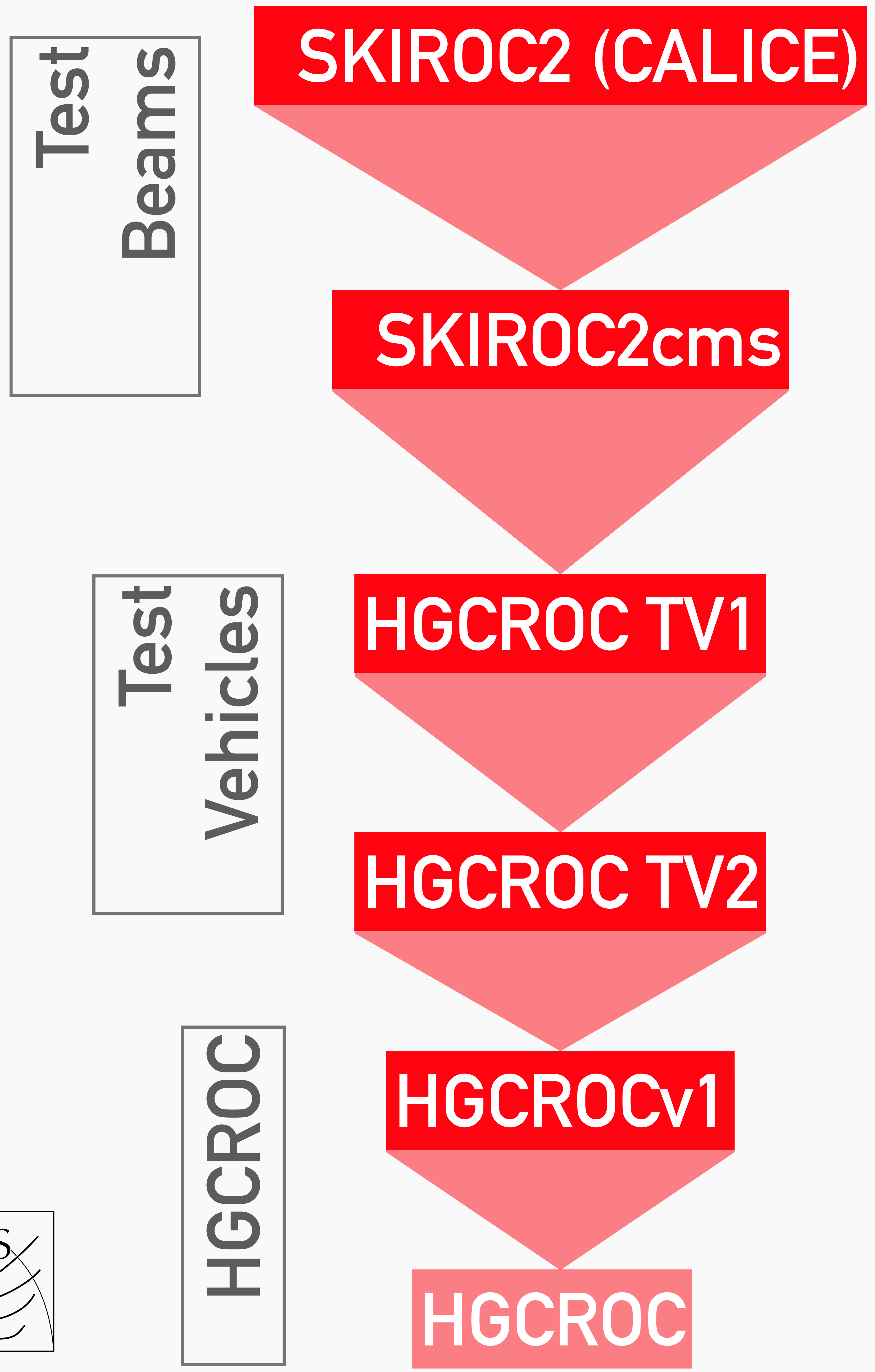
VERY FRONT-END ASIC

- At the heart of the detector electronics is the front-end readout ASIC
- The design and environment of the HGCAL pose several requirements
  - System on chip: charge, time, digitization, data and trigger processing, ZS …
  - Low power: < 15 W/channel
  - Low noise: < 2000 e^-
  - High radiation: 10^{16} n_{eq} (1MeV eq.)/cm^2
  - High speed readout: > 1 Gb/s
  - Same ROC for Si&SiPM



- Signal: high dynamic range: 0–10 pC
  - Charge: 0–100 fC [11 bits]
  - Time over Threshold: 0.1–10 pC [12 bits]
- Timing information: Time of Arrival with 25 ps resolution > 50 fC [12 bits]

HGCAL ASIC EVOLUTION: FROM SKIROC TO HGCROC

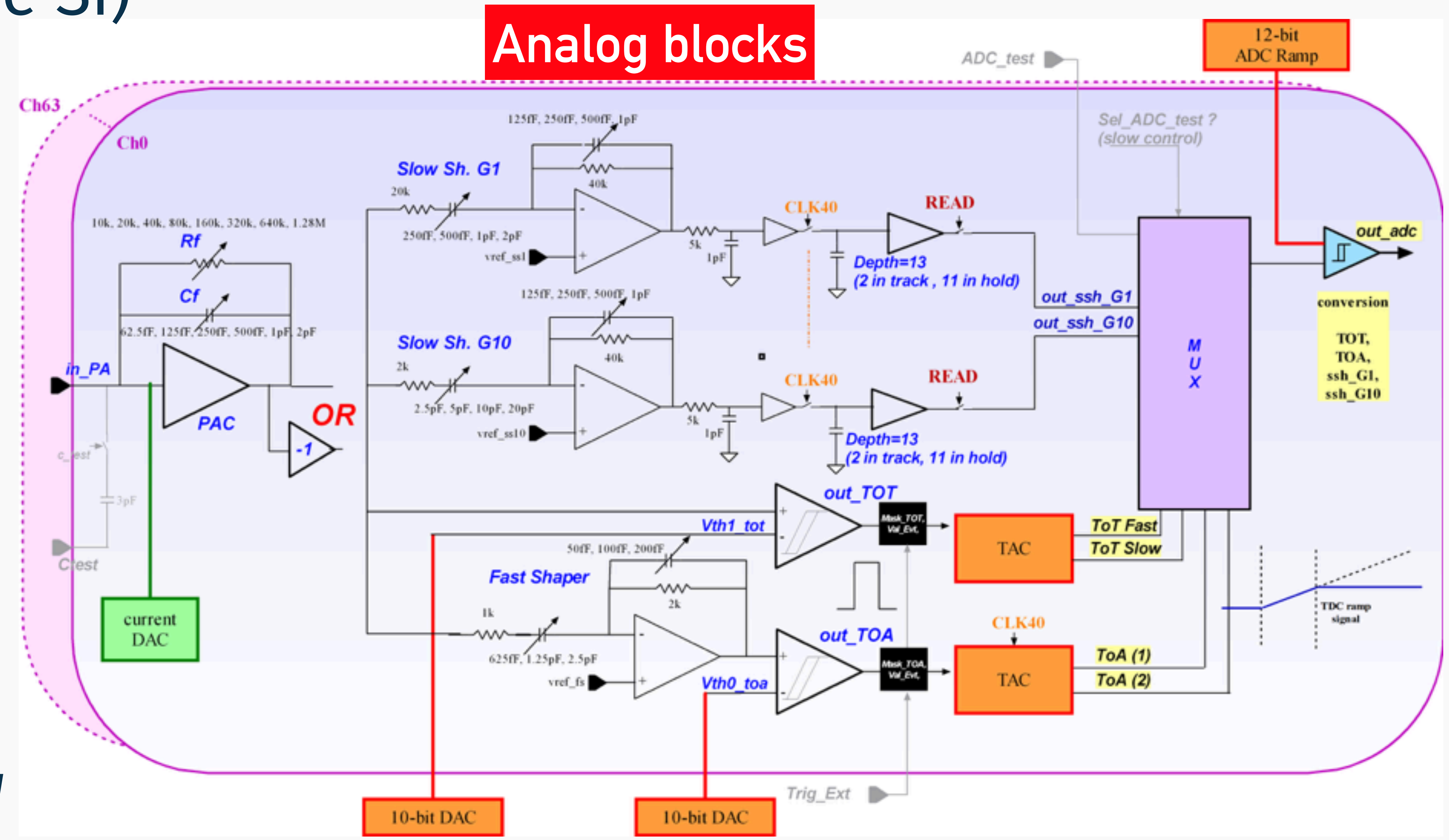


- SKIROC2:
  - ASIC used by CALICE in the SiW ECAL
  - Dedicated 64 channel Si-detector readout ASIC, SiGe 350 nm
- SKIROC2cms: *submitted and received in 1Q of 2016*
  - Modification for test beams with CMS-like running conditions
  - 40 MHz clock and sampling, Gain + ToA + ToT
- Test Vehicle 1: *submitted in May 2016, received in August 2016*
  - First HGCROC test vehicle in CMOS 130 nm architecture
  - Dedicated to preamplifier studies
- Test Vehicle 2: *submitted in December 2016, received in May 2017*
  - Dedicated to analog channel study for TDR
- HGCROCv1: *submitted in July 2017, expected in October 2017*
  - All analog and mixed blocks; many simplified digital blocks

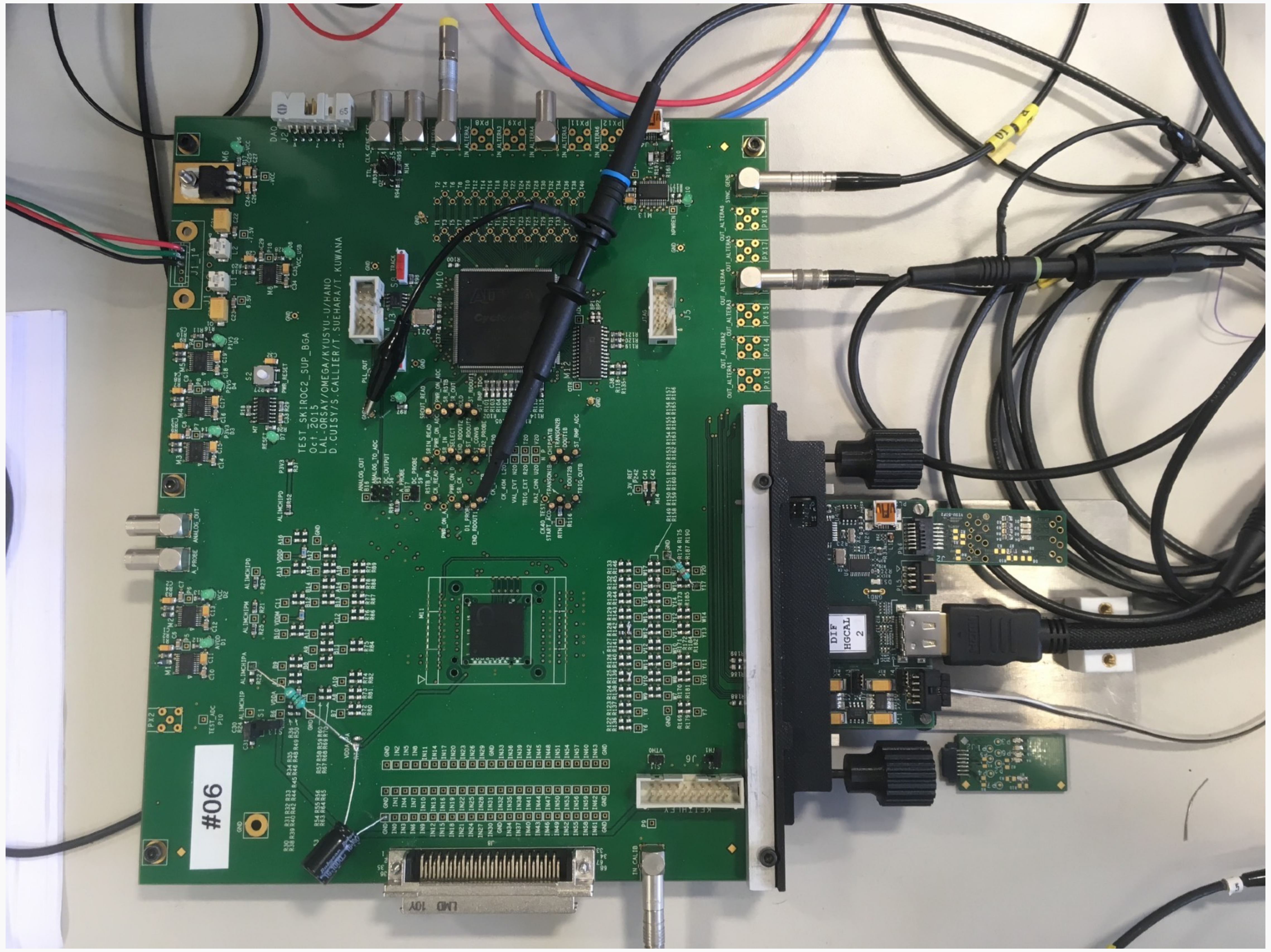
➡ **Final HGCROC submission by mid 2019!**

SKIROC2CMS: ASIC FOR BEAM TESTS [Q1 2016]

- Modified 64ch CALICE SKIROC2 specially for test beam use
- Dual polarity preamplifier (for p- or n-type Si)
- 40 MHz clock and 25 ns sampling
- ADC: low and high (x10) gain
  - Slow shaper with 40ns shaping time
  - 300ns in rolling analog memory
- Time-of-Arrival — *proof of principle!*
  - Fast shaper (5 ns)
- Time-over-Threshold — *proof of principle!*
  - For large signals directly from the preamplifier
- TDC (TAC) for TOA & TOT (~20 ps binning, ~50ps jitter)



SKIROC2CMS: ASIC FOR BEAM TESTS

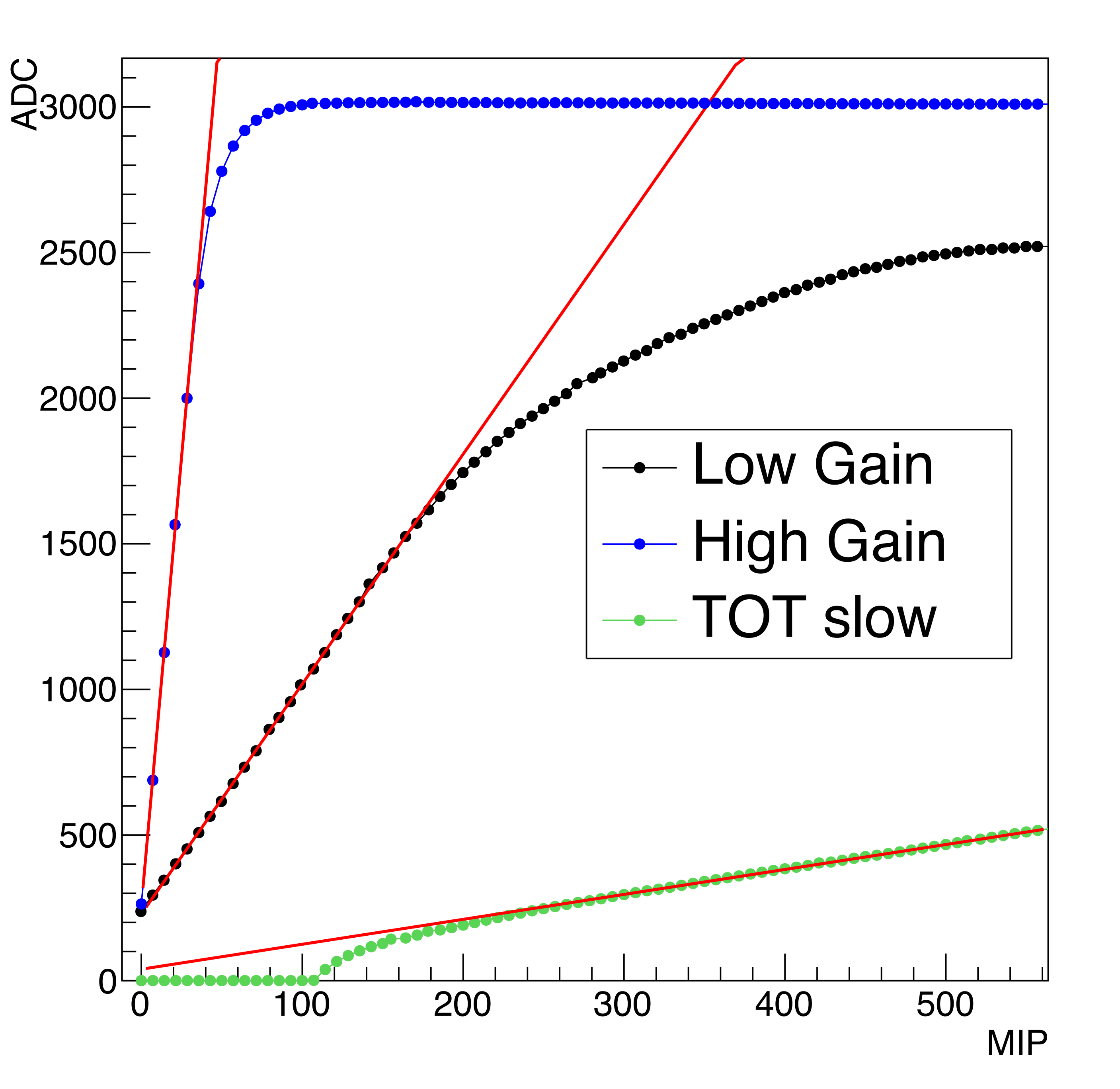


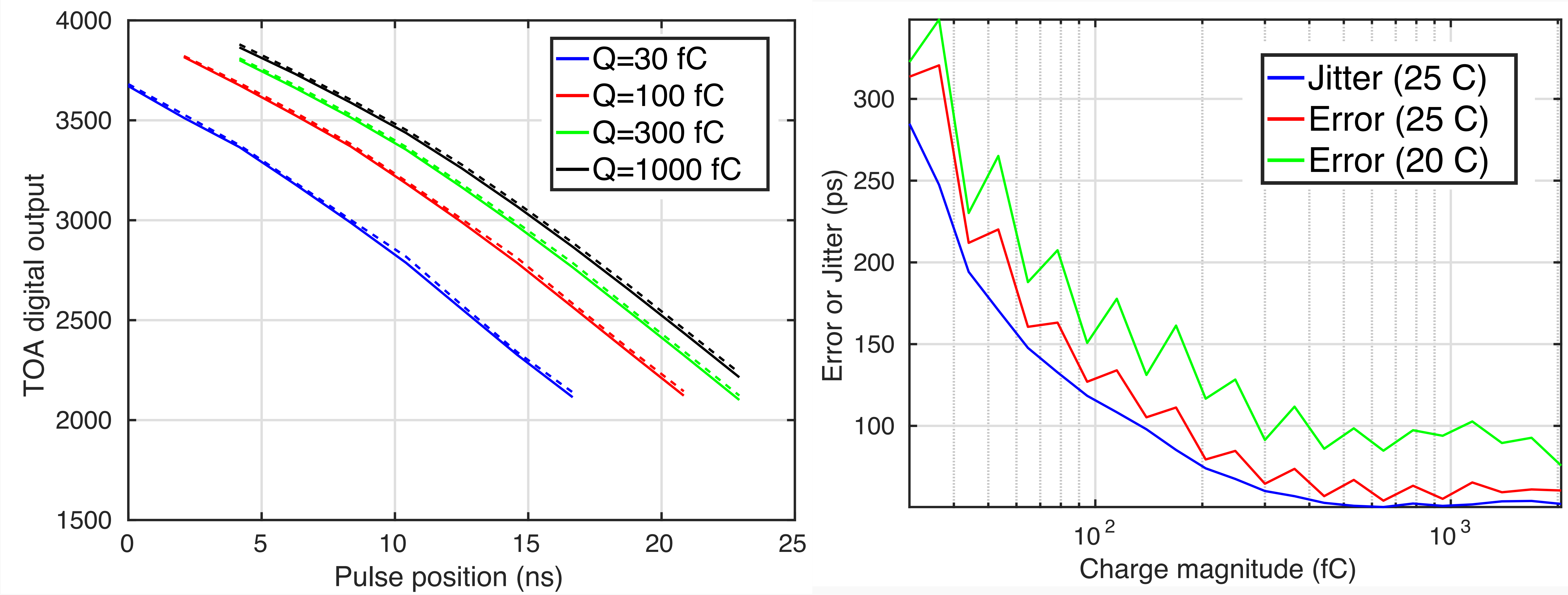
ASIC test board

- Extensive tests of the SKIROC2cms ASIC have been performed
  - Gain and TOT linearity, noise, pedestals
  - TOA transfer characteristics, efficiency, time-walk, jitter
  - Temperature stability
- On single-ASIC test board and hexaboard
- More details about the TB performance in tomorrow's talk by Thorben Quast

SKIROC2CMS: ASIC FOR BEAM TESTS

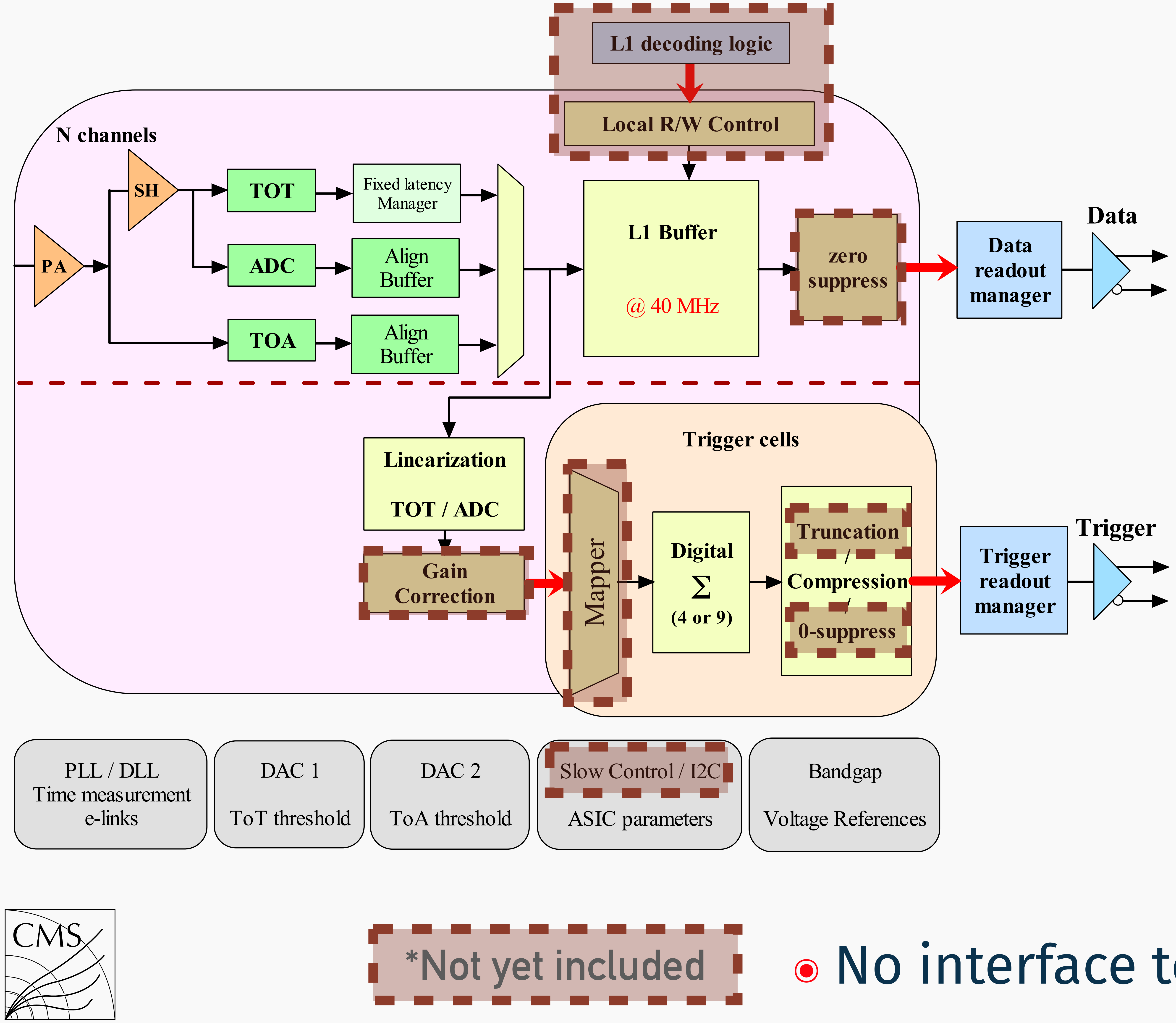
- ADC and TOT linearity:
  - HG/LG linear until 500 fC
  - TOT linear for 500fC — 10pC
- Noise for gain: ~ 3500 e⁻
- TOA performance:
  - Off-line correction for time-walk possible
  - Constant term: 50 ps
  - Noise term: 10ns/Q(fC) [expected ~4ns/Q]





* Jagged shape is due to imperfect interpolation between characterisation measurements.

HGCROCv1 [Q3 2017]



- 32 channels for development/cost
- Dual polarity (for p- or n-type silicon)
- TOA, TOT with 2 variants: low power or DLL
- 11-bit SAR ADC @ 40MHz
- Simplified Trigger path: no ZS, only 4 sums
- Data readout @ 320MHz
- Slow Control with triple voting (shift register like SK2-CMS)
- Digital blocks with simplified architecture
- Services: bandgap, PLL, 10b DAC
- No interface to GBT/concentrator yet

HGCAL TRIGGER FLOW

Front-end

- **HGCROC** — Resolution and granularity reduction, formation of trigger cells (TC)
- ~300 Tb/s
- **Concentrator** — Selects fraction of trigger cells (threshold or fixed number of highest energy TC)
- ~40 Tb/s

Back-end Trigger primitive generator

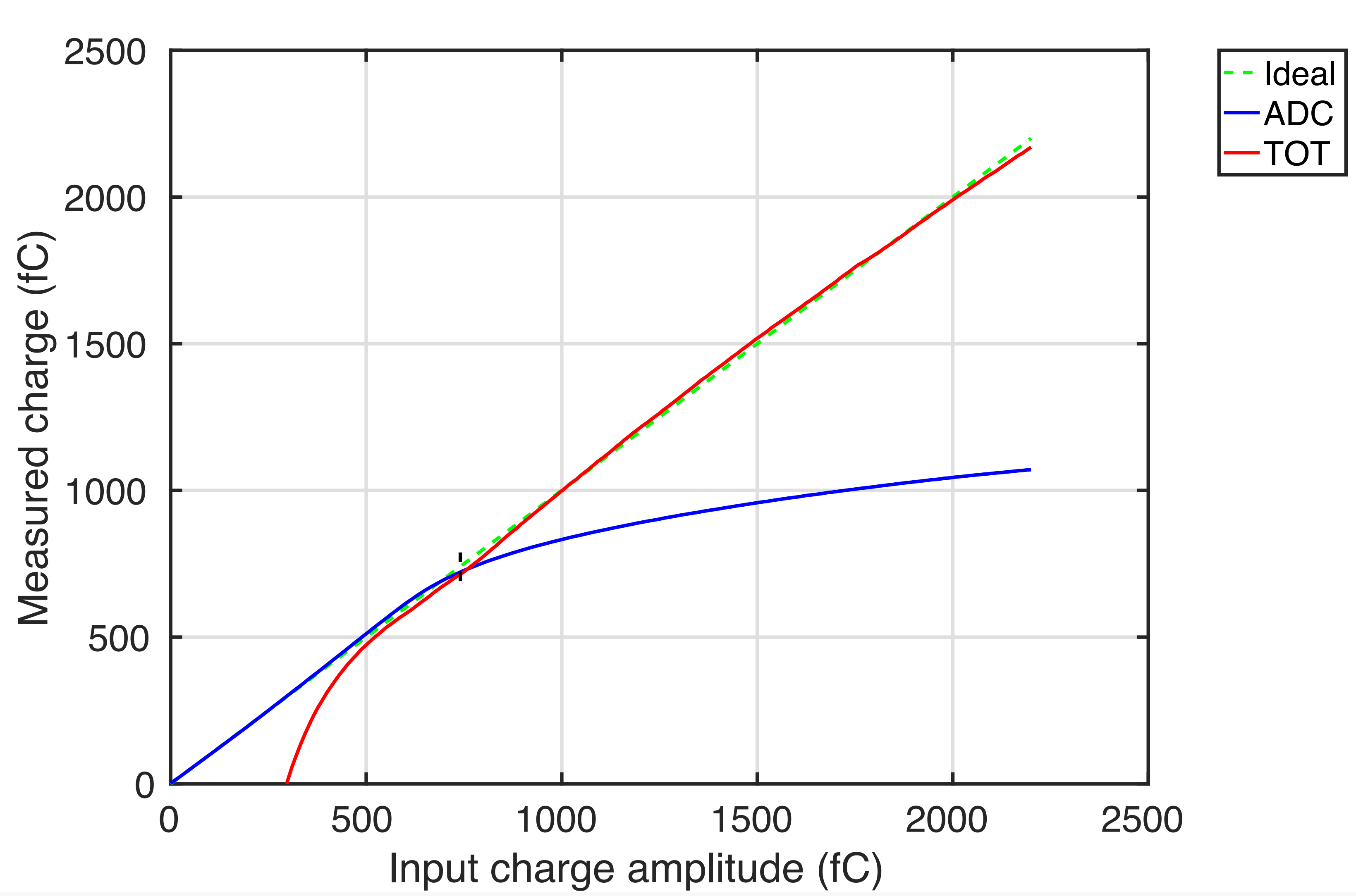
- **TPG Stage 1** — Dynamical 2D clustering of trigger cells per layer
- ~20 Tb/s
- **TPG Stage 2** — Formation of 3D clusters — trigger primitives (TP)
- ~2 Tb/s

CMS Trigger

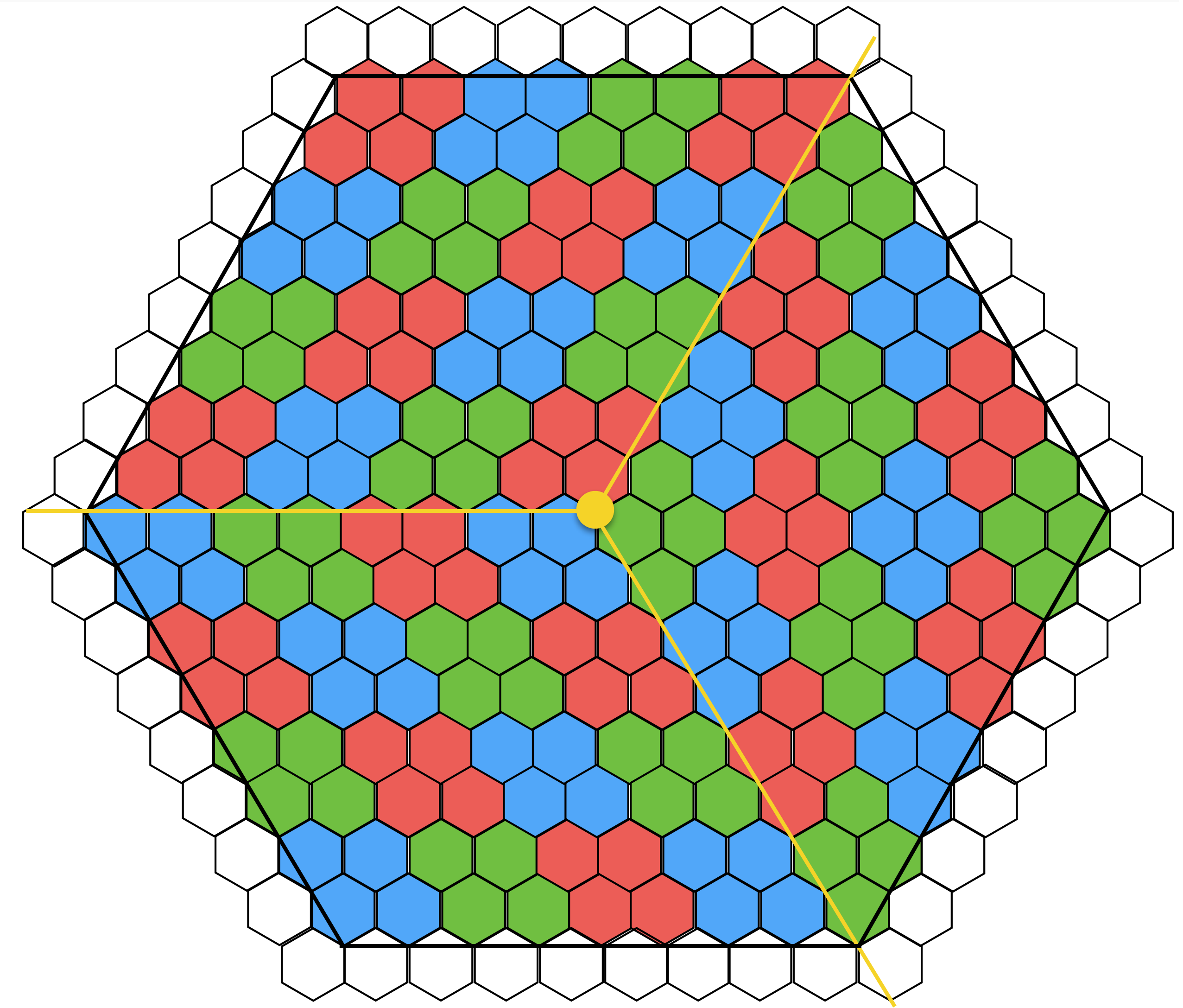
- **Correlator** — L1 trigger correlator with input from track trigger
- **Global trigger** — Central CMS L1 trigger

TRIGGER: HGCROCv1

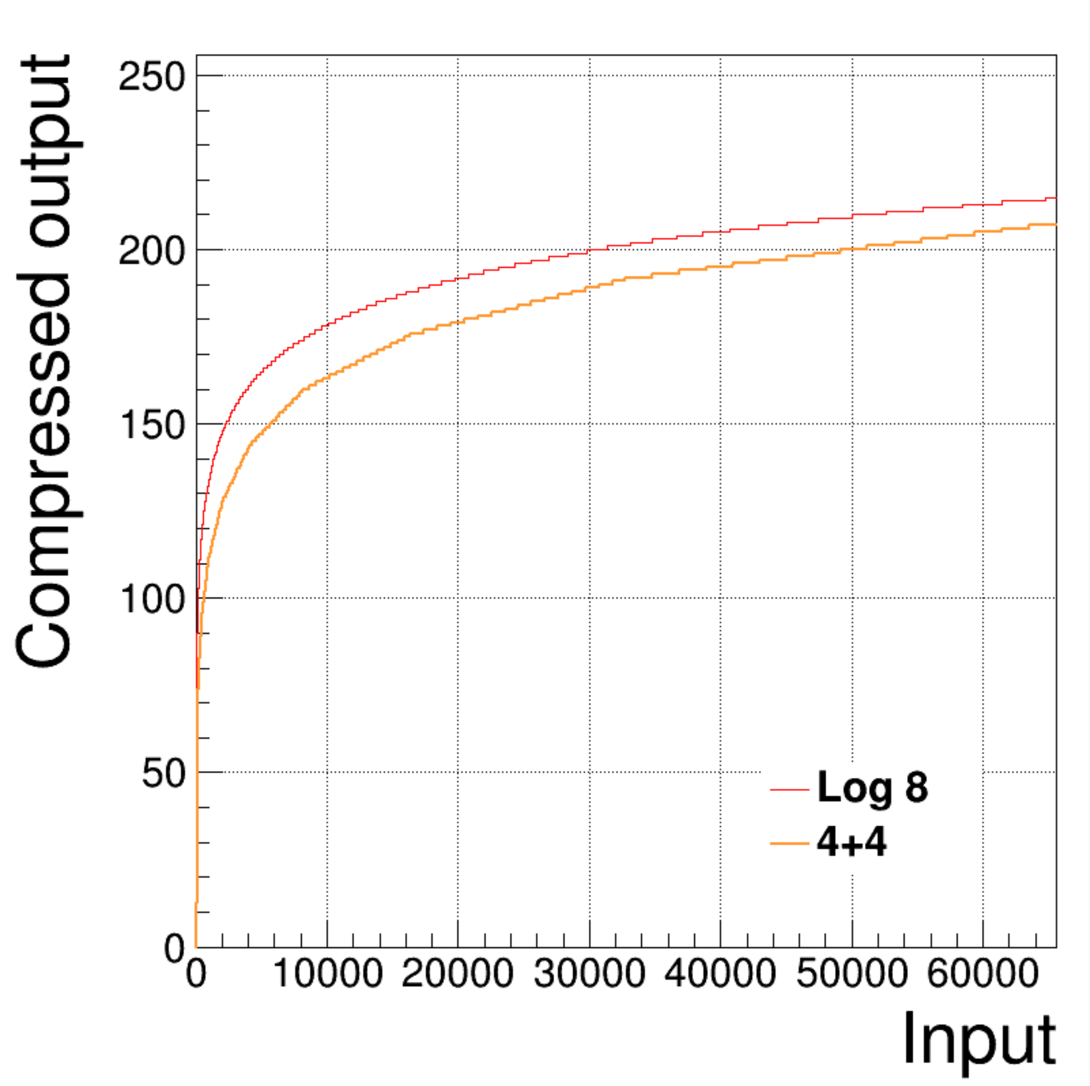
- Reduced energy resolution:
  - ADC/TOT linearization: automatic switching
  - Digitized charge data:
    - Gain: 11-bit ADC ➔ LSB @ 0.1 fC
    - TOT: 12-bit TDC ➔ LSB @ 2.5 fC
  - Compensate LSB ratio (~25) ➔ 17 bits
- Reduced granularity:
  - 4 (9) cells per Trigger Cell (48 per wafer)
  - Sum of 4 channels ➔ 17+2 bits
- Compression:
  - 4+4 encoding ➔ 8 bits



ADC/TOT linearisation



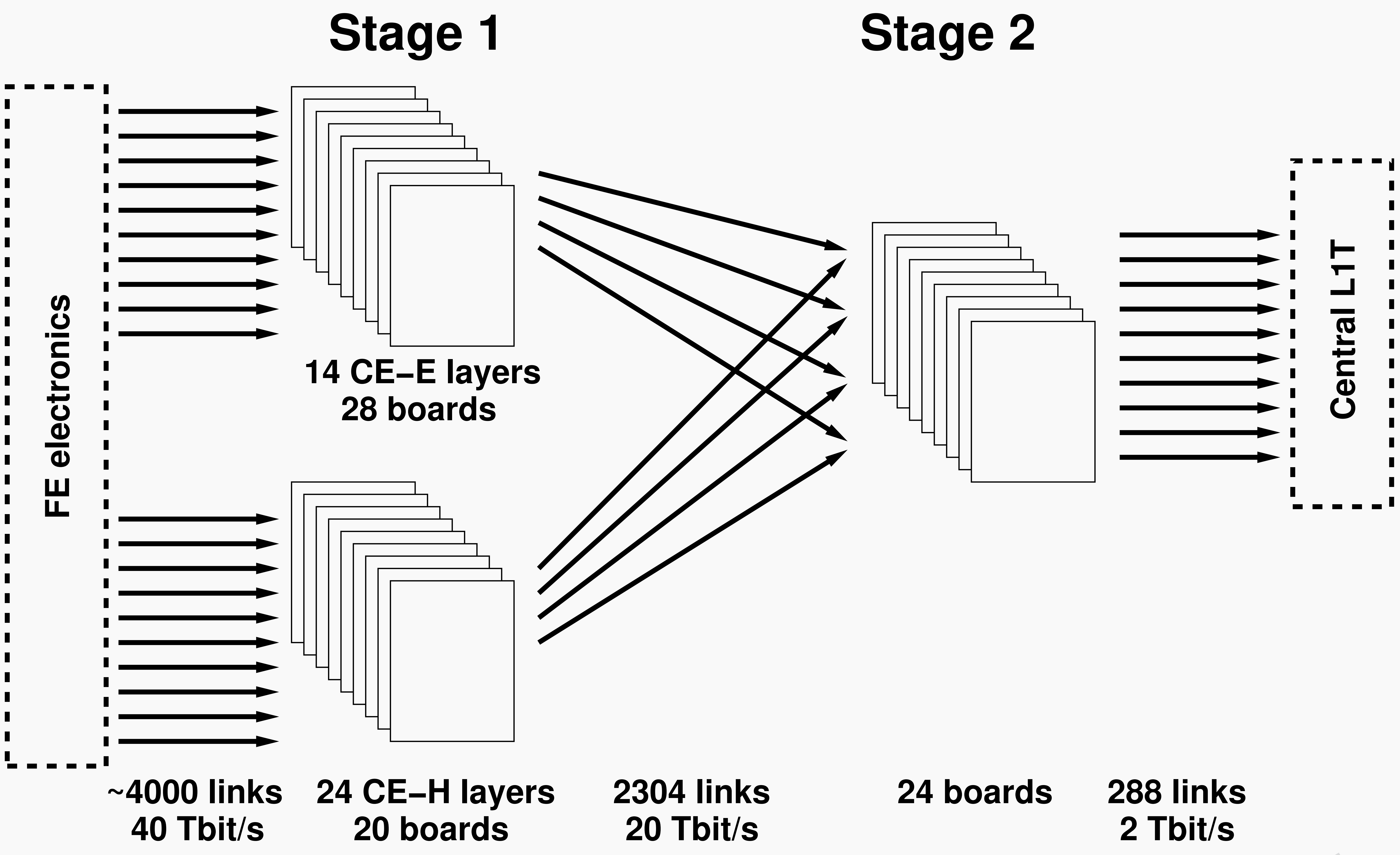
Trigger Cells



Data compression

BACK-END: TRIGGER PRIMITIVE GENERATOR

- Stage 1:
  - Dynamical clustering based on the Nearest Neighbour TCs
    generates **2D clusters** in each trigger layer
- Stage 2:
  - Creation of **3D-clusters** exploiting the longitudinal development of the shower using the projected position of each 2D cluster to identify its direction

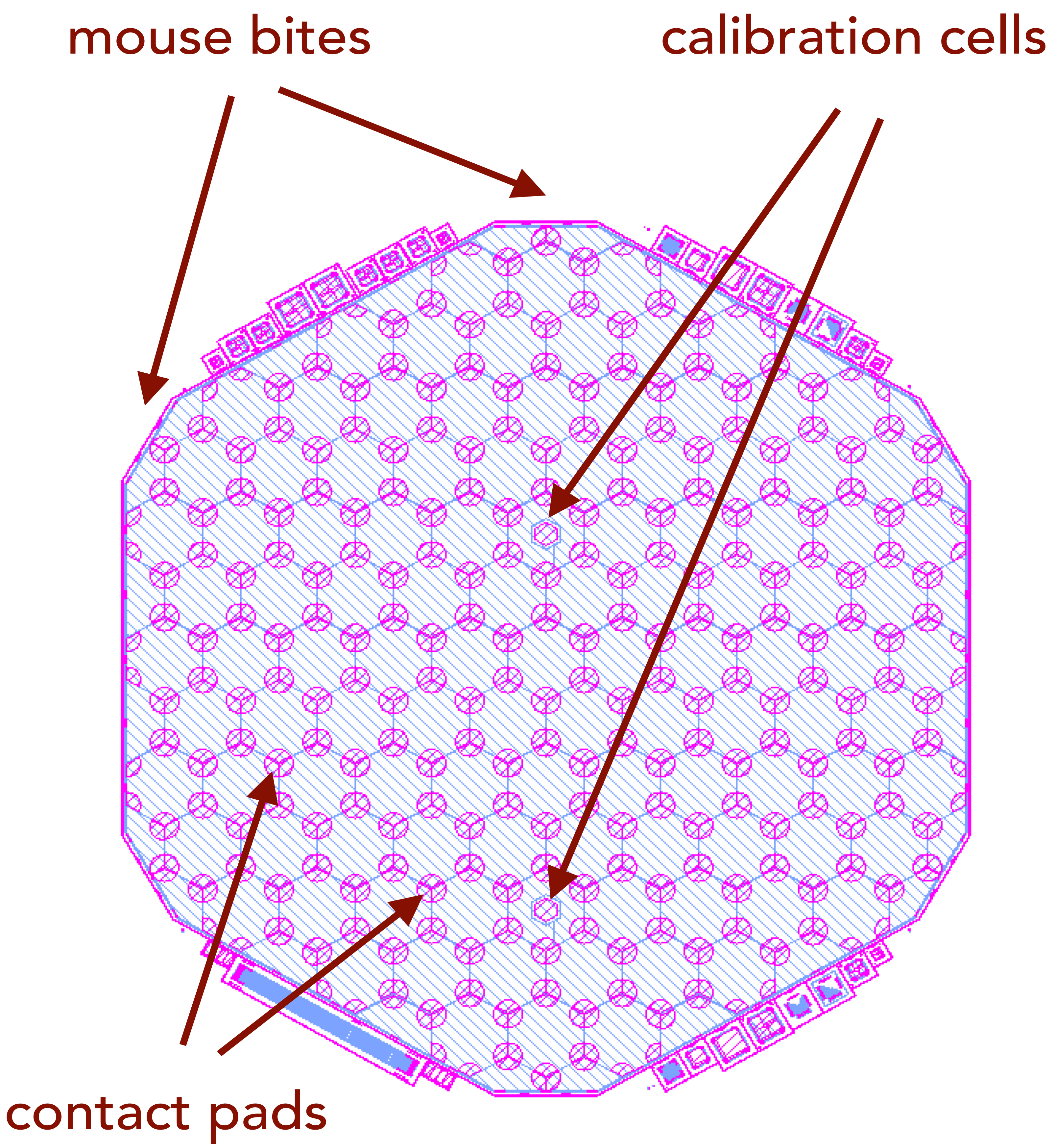


- The Stage 1 –> Stage 2 data transmission is **x24 time-multiplexed** in order for all data from one endcap to be processed by one single FPGA

HGCAL SI-SENSOR AND WAFERS

- **Hexagonal geometry** as largest tile-able polygon
  - **6” and 8”** sensors considered
  - Cell sizes of **~0.5 cm^2 and ~1 cm^2**
  - Cell capacitance of **~50 pF**
  - Will most likely need n-on-p for inner layers
- Some design goals
  - **1kV sustainability** to mitigate radiation damage
  - **Four quadrants** to study inter-cell gap distance and its influence on V_{bd}, C_{int} and CCE
- A few more details about those sensors
  - Active thickness by **deep diffusion or thinning**
  - Inner **guard ring is grounded**, outer guard ring is floating
  - Truncated tips, so called **mouse bites,** for module mounting
  - **Calibration cells** of smaller size for single MIP sensitivity at end of life

From TIPP-2017



Hamamatsu 6” 128ch design