The TIMESPOT project
A System Approach to 4D tracking

Adriano Lai
INFN – Sezione di Cagliari – Italy

Istituto Nazionale di Fisica Nucleare

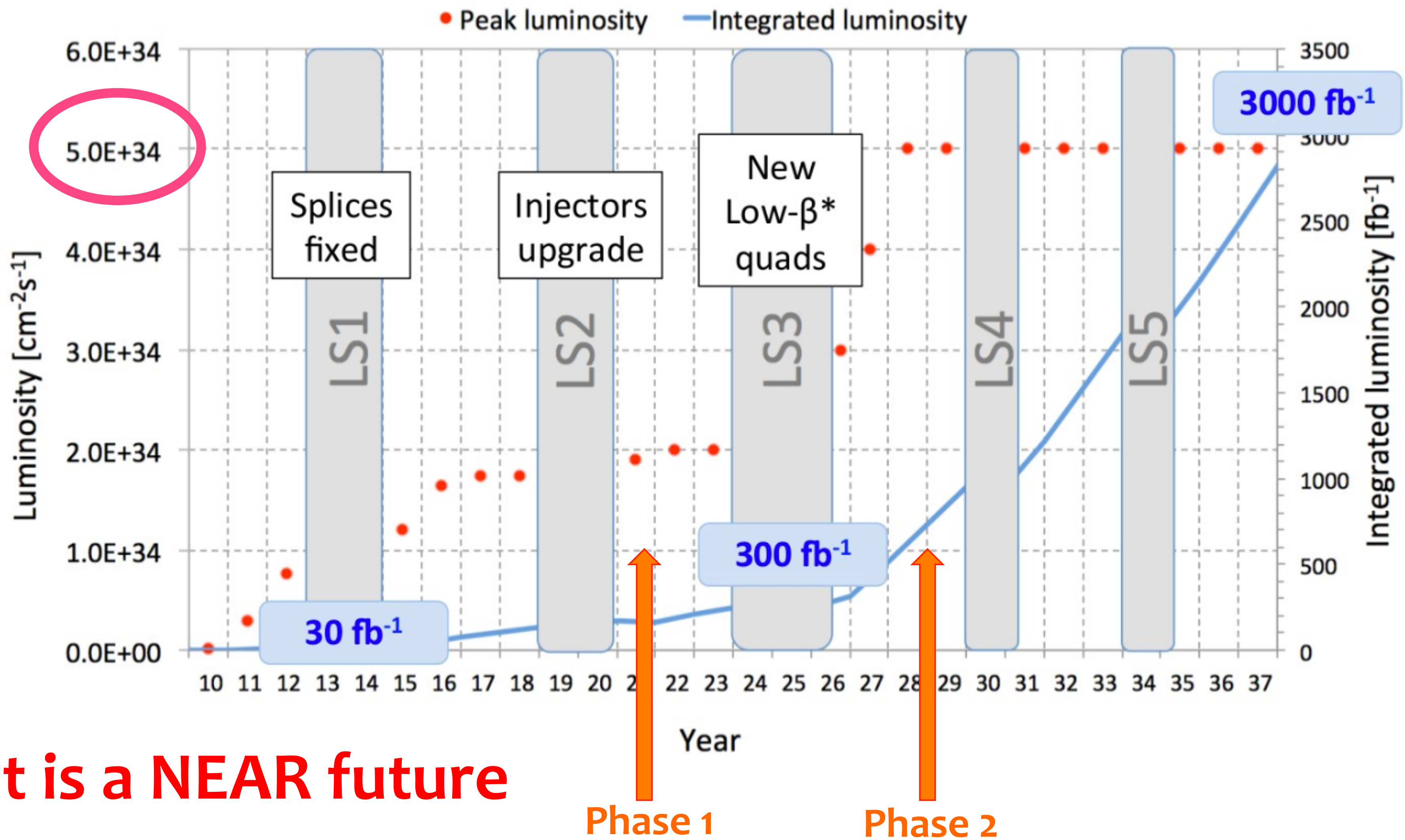
TimeSPOT
TIME and SPace real-time Operating Tracker

Outline

1. Why 4D ? Why timing?
2. Aim and Structure of the project: organization in Work Packages
3. Why 3D sensors ?
4. 2018 activity and first results
   a. Progress on sensor developments
   b. Progress on front-end electronics
   c. Progress on algorithms for real-time tracking
4. Perspective
5. Conclusion

The problem of tracking at HI-LUMI colliders and posed requirements

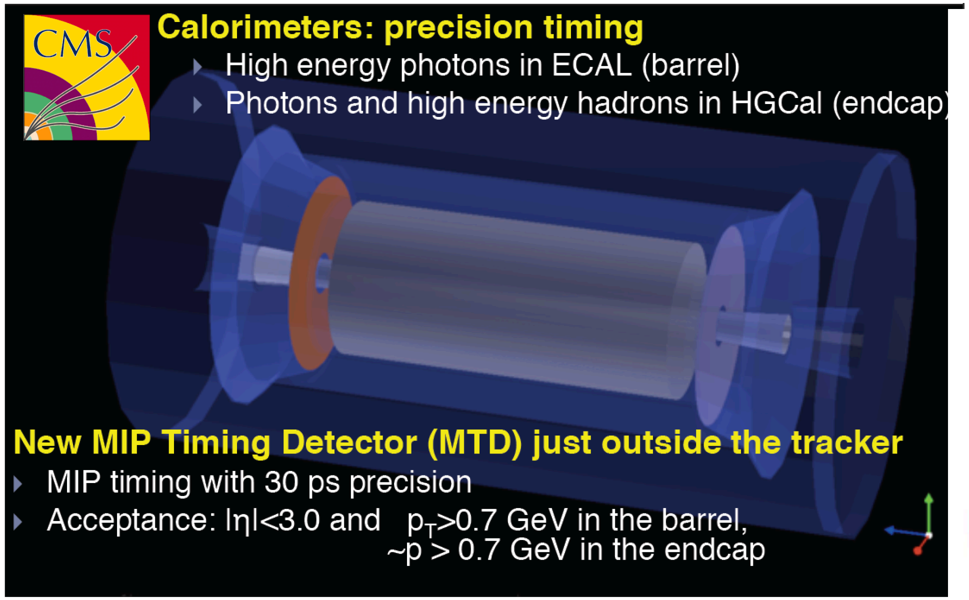
LHC upgrade program

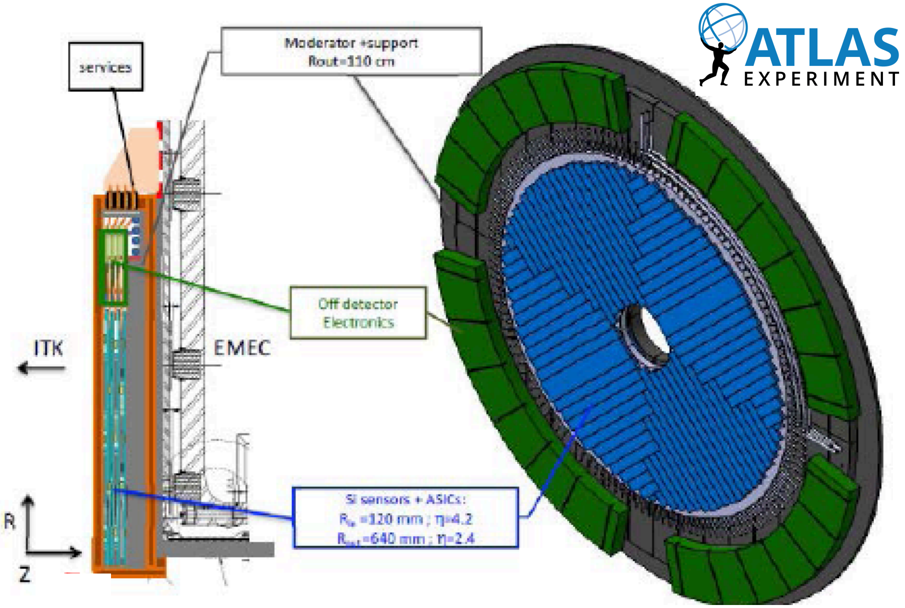


It is a NEAR future

CMS and ATLAS Phase2: Timing Layers.

Both experiments are aiming at an upgrade in Inner Tracking systems , but high pile-up (O(100)) merges vertices even after upgrades, causing important inefficiencies in Primary Vertex (PV) identification (around 15%)



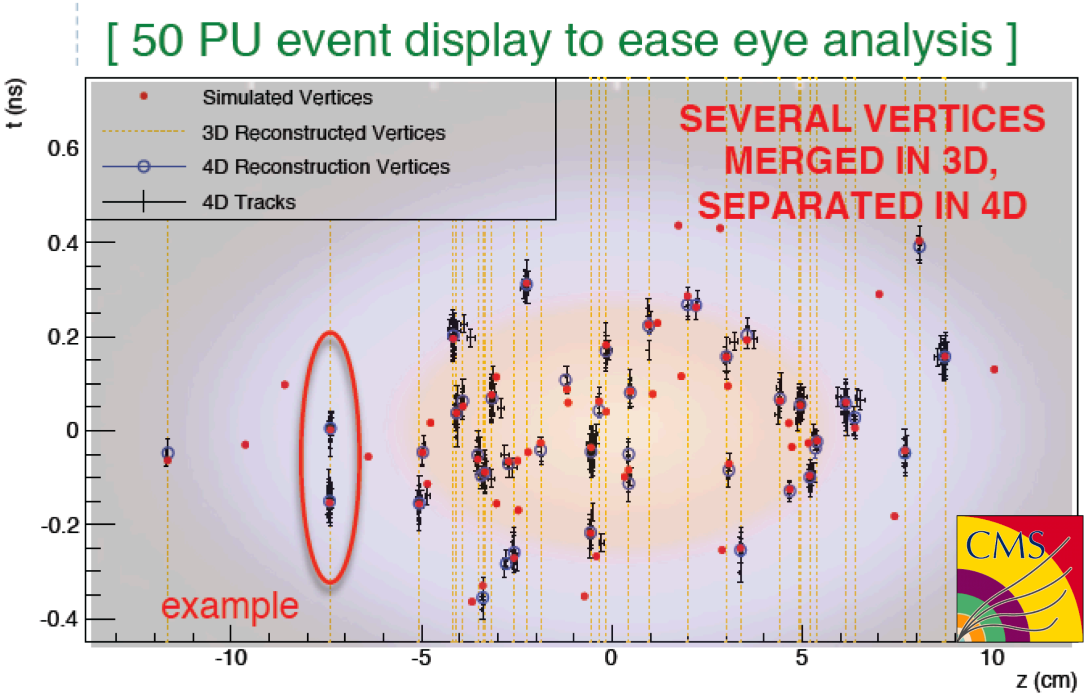


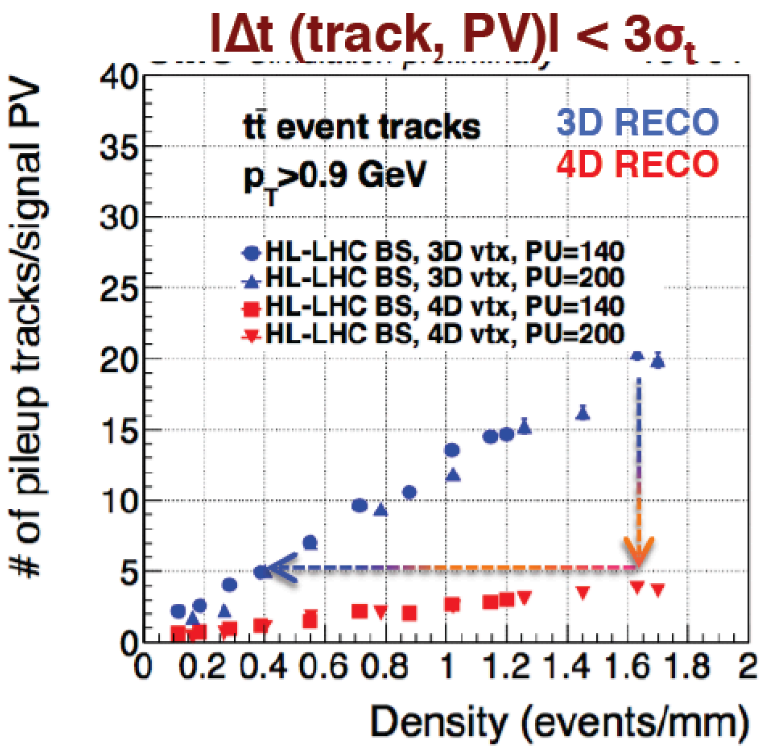
- **Coarser space resolution w.r.t. trackers (power and number of channels saving)**
- **Use measurement of track path length and momentum to determine time-at-vertex for the track**
- **Pick timing layer hits by means of tracking, integrating timing layer hits into 3D Kalman**
- **Filter**
- **Back propagate smoothly to tracker, using a higher-dimensions KF with timing information**

→ Timing used at trigger and/or analysis level

CMS and ATLAS Phase2: Timing Layers.

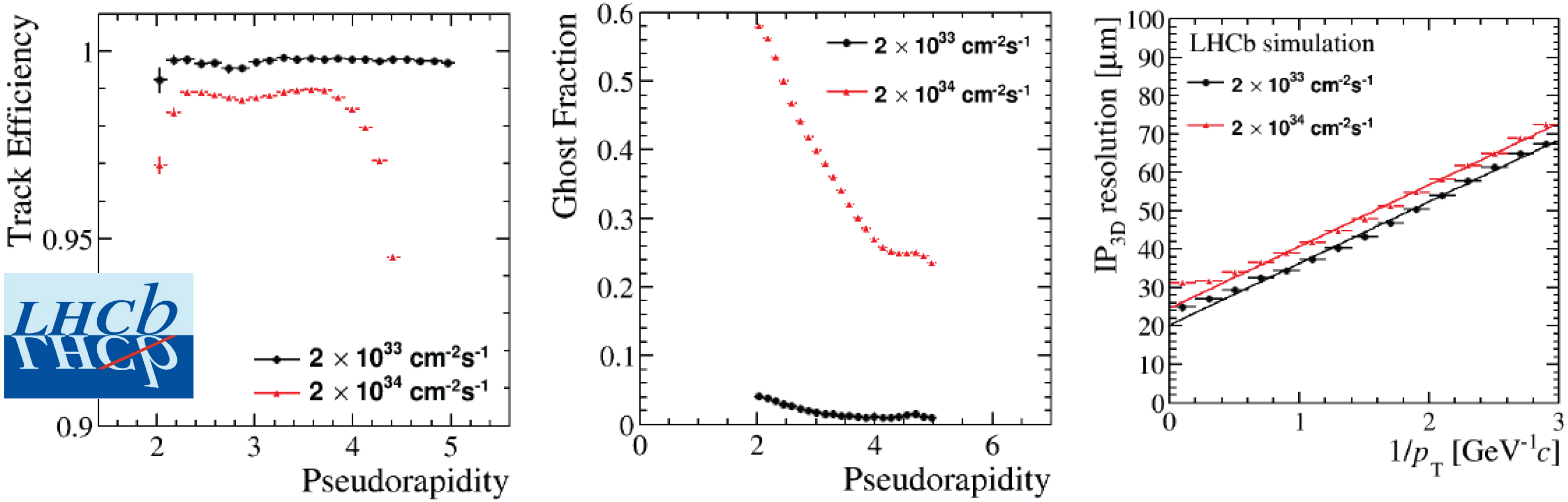
Both experiments are aiming at an upgrade in Inner Tracking systems , but high pile-up (O(100)) merges vertices even after upgrades, causing important inefficiencies in Primary Vertex (PV) identification (around 15%)





Timing layers should take back inefficiencies to the level of Phase1 (1-2%)

Timing Layers, are they sufficient?

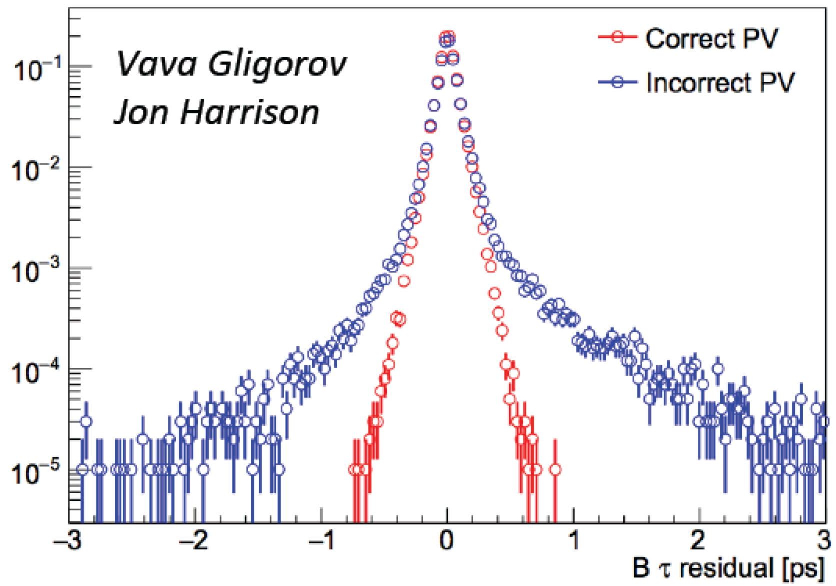


The LHCb experiment has a slightly different time-scale for the upgrade. It will reach 2 x 10^{34} in luminosity after LS4 (year 2030)

Studies on physics perormance using a non-upgraded detector show a dramatic drop in performance, which can be (only partially) recuperated increasing (x4) the granularity of the vertex detector (or adding time information to pixels)

Moreover, LHCb requirements in radiation hardness, are ≈ x10 those of ATLAS/CMS Phase2

Timing Layers, are they sufficient?

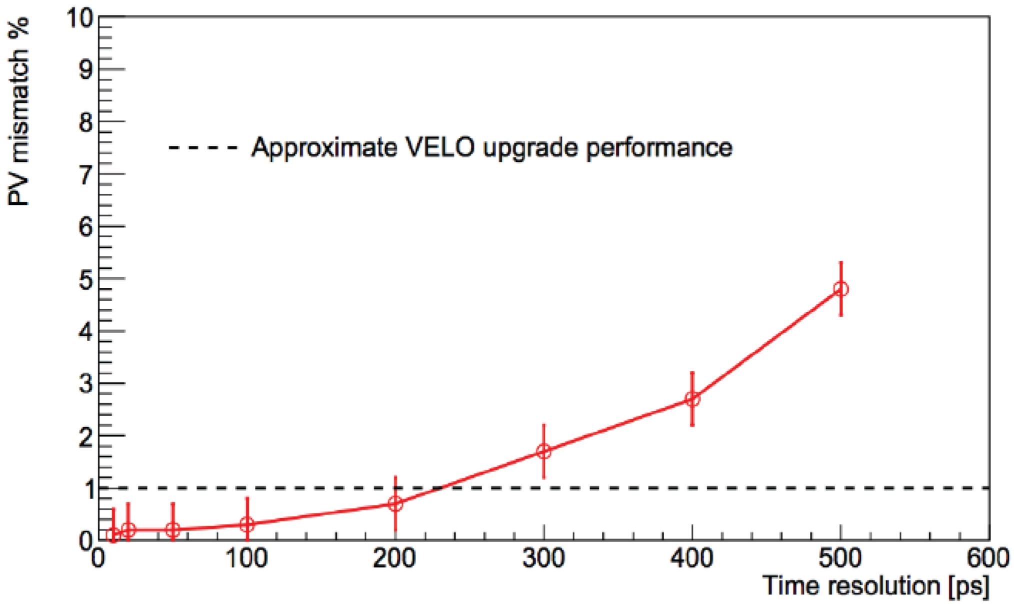


To keep the PV reconstruction performance at the due level about 6 ps time resolution per track must be kept

Correspondingly, at least 200 ps per pixel are required: timing INSIDE the tracker

An important channel of activity in the LHCb physics program requires an accurate measurement of lifetime in B and C meson decays

Incorrect PV identification dramatically spoils the lifetime measurement



Beyond LHC Hi-Lumi?

	LHC ALICE ITS	CLIC	HL LHC Outer pixel	HL LHC Inner pixel	FCC pp
NIEL (n_{eq}/cm^2)	10^{13}	$< 10^{12}$	10^{15}	10^{16}	10^{15} - 10^{17}
TID	< 3 Mrad	< 1 Mrad	80 Mrad	1 Grad	40 Grad
Hit rate (MHz/cm2)	10	< 0.3	100-200	2000	200-20000

General specifications for a vertex detector of the next generation (Hi-Lumi and beyond)

- Space resolution: ≈ 10 μm (pixel pitch ≈ 50 μm)
- Radiation hardness: 10^{16} to 10^{17} 1 MeV n_{eq}/ cm^2 (sensors) and > 1 Grad (electronics)
- Time resolution: 100 ps per pixel or better (< 10 ps per vertex)
- Data rates of the order of n x Tb/s to be handled (real-time?)

TIME & SPace real-time Operating Tracker

Structure, organization and objectives of the project

INFN
Istituto Nazionale di Fisica Nucleare

TimeSPOT
TIME and SPace real-time Operating Tracker

Main target:

Develop and realize a demonstrator consisting of a complete and simplified tracking system, integrating about 100-1000 read-out channels (pixels), satisfying the following characteristics:

- Space resolution: O (10 μm)
- Radiation hardness: > 10^{16} 1 MeV n_{eq}/ cm^2 (sensors) and > 1 Grad (electronics)
- Time resolution: < 100 ps per pixel (target ≈ 30 ps)
- Real time track reconstruction algorithms and fast read-out (data throughput > 1 TB/s)

Activities are organized in 6 work packages: P.I. : A. Lai, Cagliari

2018 (items 1–3)

1. 3D silicon sensors: development and characterization (GF. Dalla Betta Trento)
2. 3D diamond sensors: development and characterization (S. Sciortino Perugia)
3. Design and test of pixel front-end (V. Liberali Milano)
4. Design and implementation of real-time tracking algorithms (N. Neri Milano)
5. Design and implementation of high speed readout boards (A. Gabrielli Bologna)
6. System integration and tests (A. Cardini Cagliari)

Sezioni INFN: Bologna, Cagliari, Genova, Ferrara, Firenze, Milano (+Bergamo), Padova, Perugia, Torino, TIFPA.

≈ 60 heads, ~ 20 FTE. People from LHCb, ATLAS, CMS + others

Outline

1. Why 4D ? Why timing?
2. Aim and Structure of the project: organization in Work Packages
3. **Why 3D sensors ?**
4. 2018 activity and first results
   a. Progress on sensor developments
   b. Progress on front-end electronics
   c. Progress on algorithms for real-time tracking
4. Perspective
5. Conclusion

3D silicon sensors

PROS

- Un-matched radiation hardness(1)
- Already used technology(2) for vertex detectors
- Strong mitigation of Landau fluctuation by geometry
- Extremely fast signal: optimal potentiality for timing(3) (not yet exploited!) → <u>optimization by design</u>

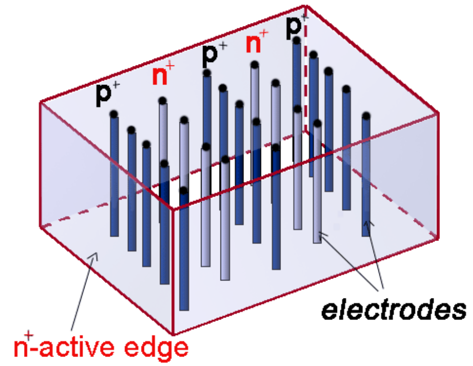
CONS

- Fabrication complexity and cost (w.r.t planar standard technology)
- Geometric inefficiency (~blind electrodes) → tilt(2) or stagger

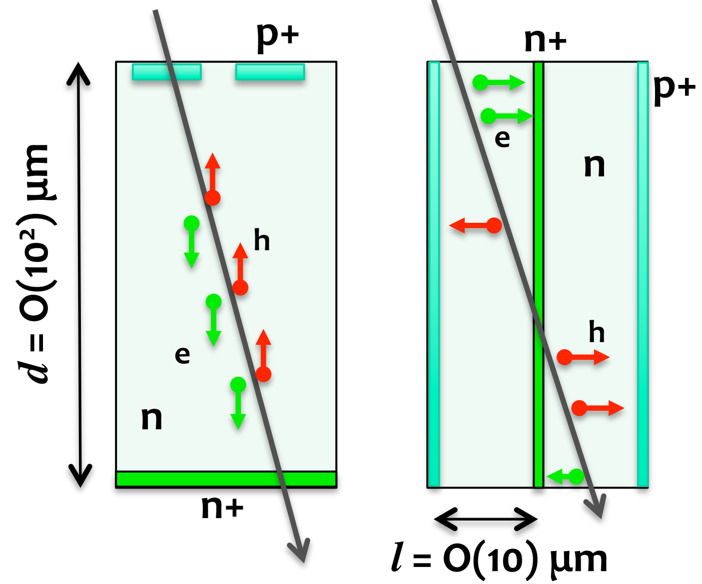
(1) J. Lange et al, *Radiation hardness of small-pitch 3D pixel sensors up to a fluence of 3x10^{16} n_{eq}/cm^2*, 2018 JINST 13, P09009.

(2) C. Da Via et al., *3D Silicon Sensors: Design, large area production and quality assurance for the ATLAS IBL pixel detector upgrade.* NIMA, vol 694 Dec. 2012.

(3) S. Parker et al., *Increased Speed: 3D silicon Sensors; Fast Current Amplifiers*, IEEE TRANSACTIONS ON NUCLEAR SCIENCE, VOL. 58, NO. 2, APRIL 2011.



planar sensor vs 3D sensor



Charge deposition distance is de-coupled from electrode distance

Conclusions

Simone Gennai*
on behalf of the ATLAS and CMS Tracker Groups

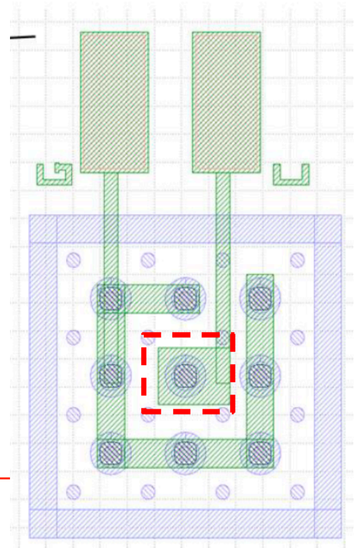
- Several test beams have been made in 2018
  - large effort of a small crew!
- Collected a large set of data
  - 3D and planar sensors
    - 50x50, 25x100
  - before / after irradiation
- Irradiation dose very near 1e16 n_{eq}/cm^2
  - FNAL test beam analysis revealed that we should not be far from the center of the beam in the LIN FE area.
- Efficiency after irradiation are compatible with those before irradiation already at moderate voltage even at high irradiation dose
  - everywhere **below 150 V**

	25x100 3D (0 deg)	**50x50 3D (0 deg)**
July (before irradiation)	97,3	98,6
October (after irradiation)	96,6	97,5

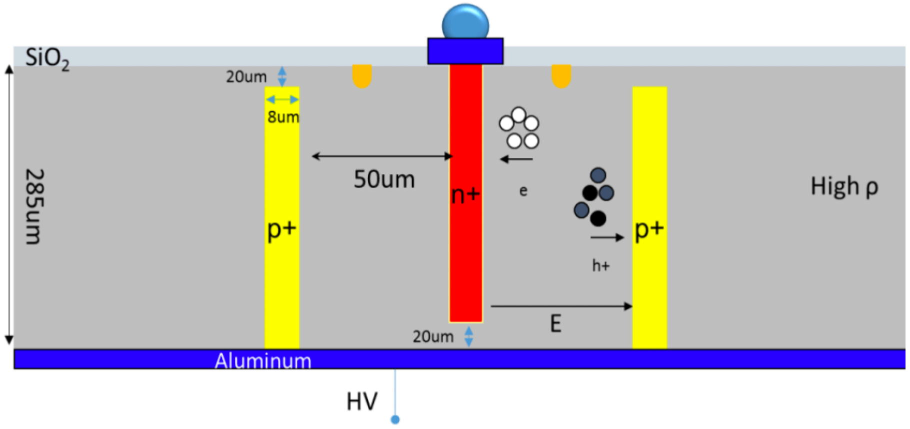
***TREDI 2019 – end of February**

Tests on CNM 3D columns (Ljubljana)

G. Kramberger *



50x50 μm²
ad-hoc test structure
Slightly different from FBK



***TREDI 2019 – February**

Conclusions

- Timing in small cell 50x50 μm² 3D detectors was measured and simulated.
- Very good agreement between simulated and measured results was found, within 10%, which validates simulation.
- Contribution to the timing resolution due to different hit positions (disuniformity) is found to be comparable to landau fluctuations in LGAD at high gain:
  - For multi-cell operation the resolution of 20 ps at -20°C temperature is predicted.
  - Single cell 50x50 μm² detector (1E) time resolution depends mainly on applied voltage – ~30 ps at >100 V and -20°C

3D silicon sensors
A “geometric” sensor

$$\sigma^2_t = \sigma^2_{Jitter} + \sigma^2_{Time\ Walk} + \sigma^2_{Landau\ Noise} + \sigma^2_{Disuniformity} + \sigma^2_{TDC}$$

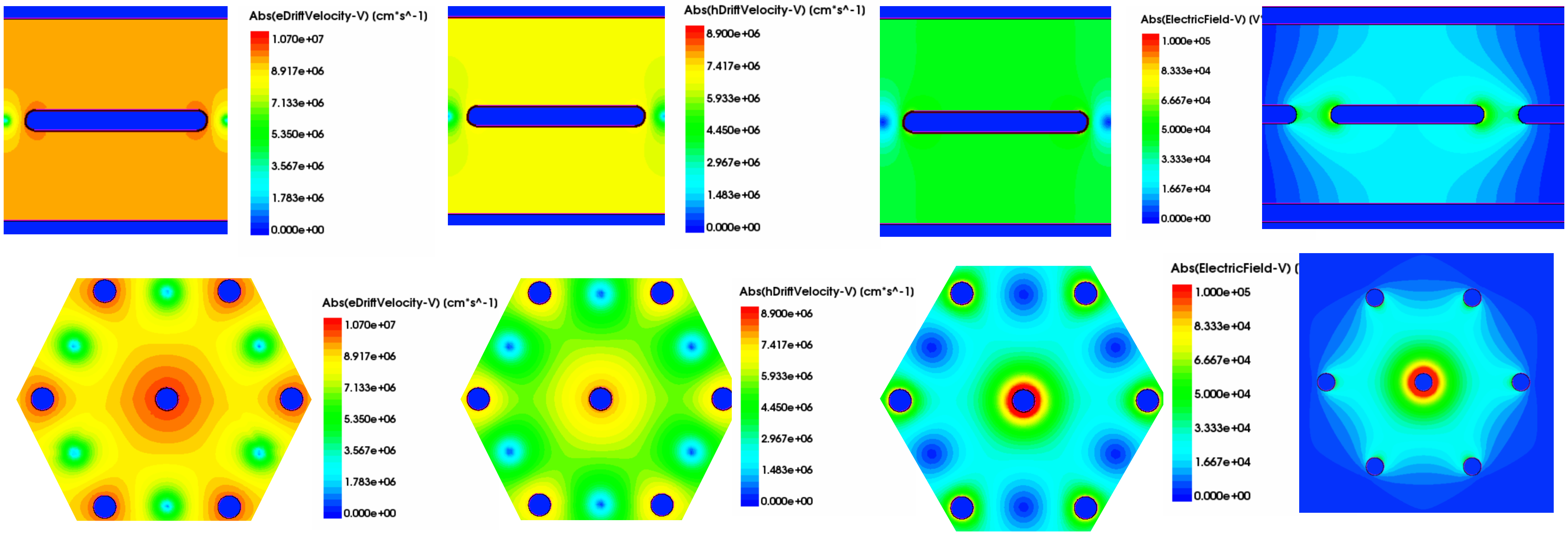
Sensor+electronics

$$\sigma_t = \frac{\sigma_n}{\left.\frac{dV}{dt}\right|_{V_T}}$$

Sensor.
3D has “in-time” δ-rays by geometry

Sensor layout: geometry

V_{bias} = 100 V



Electron drift velocity

Hole drift velocity

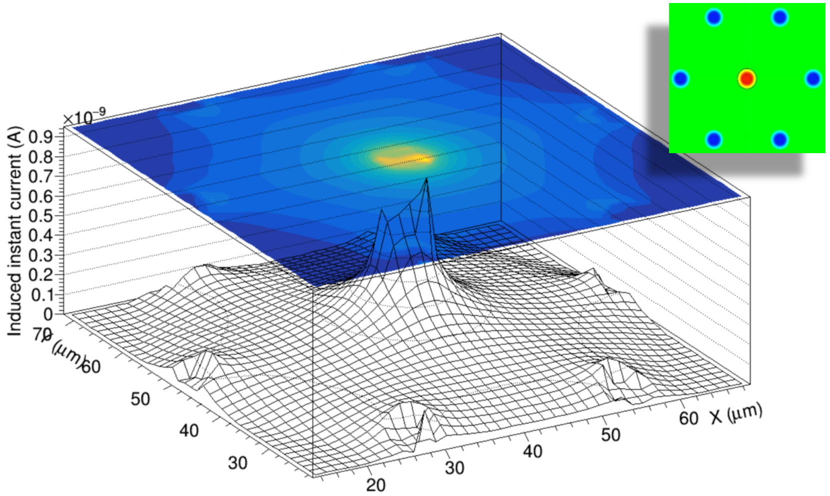
Electric field

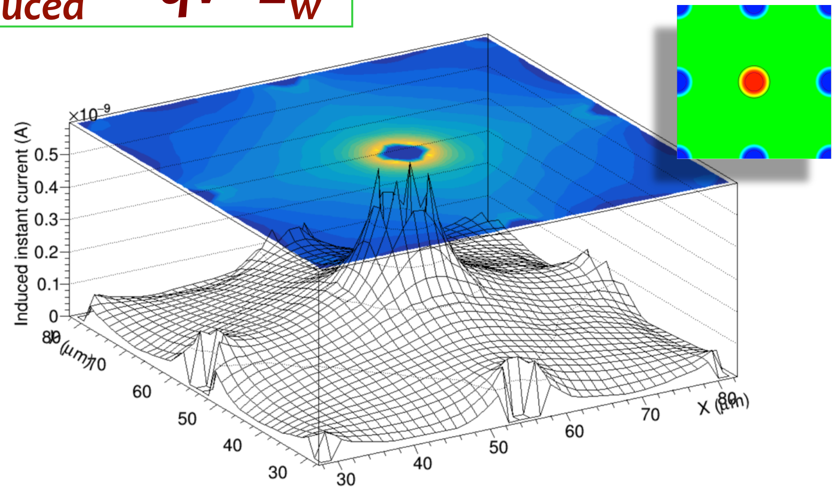
Weighting field

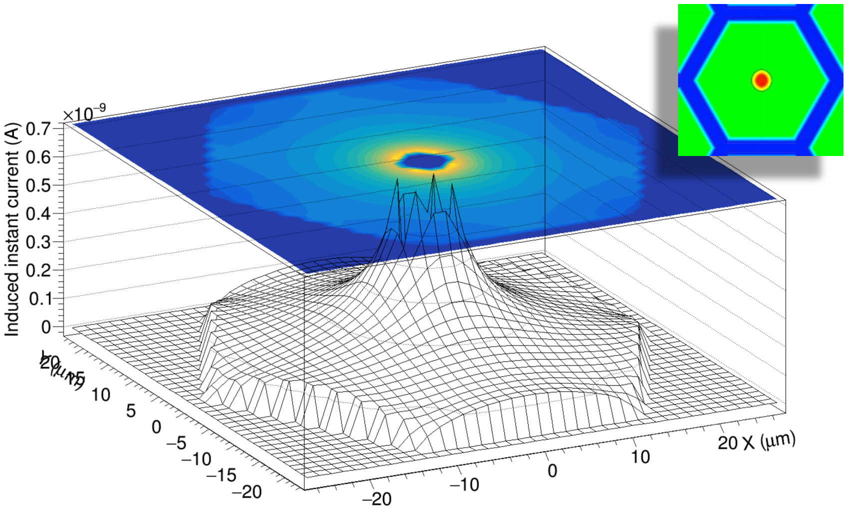
3D Sensor layout is a key for its performance

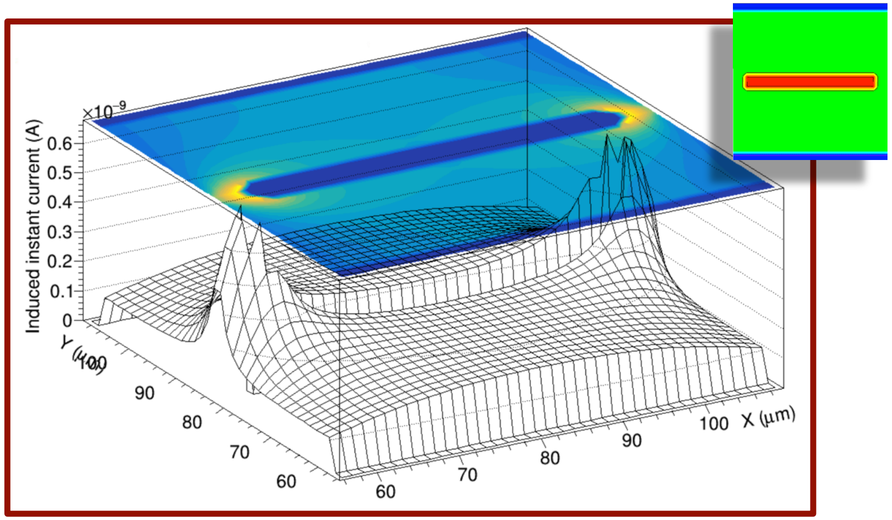
Simulations and sensor Design
2D-based “Ramo maps”

$$I_{induced} = qv \cdot E_w$$









Trench-shaped geometry

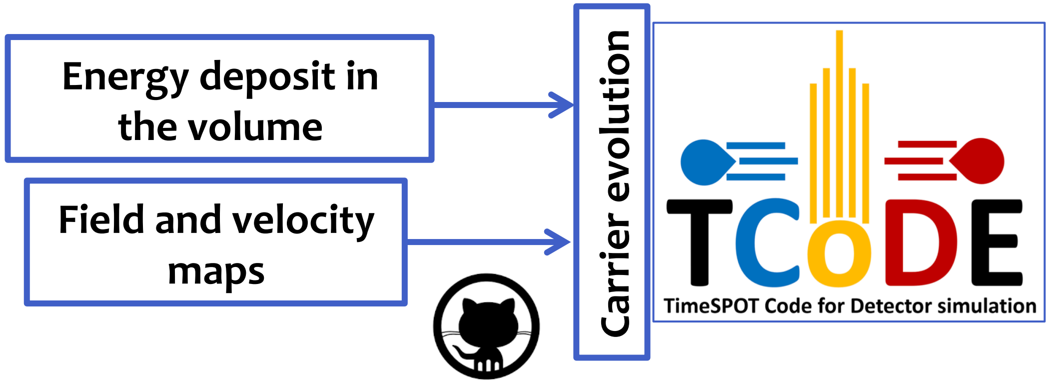
A. Loi – INFN Cagliari

Outline

1. Why 4D ? Why timing?
2. Aim and Structure of the project: organization in Work Packages
3. Why 3D sensors ?
4. 2018 activity and first results
   a. Progress on sensor developments
   b. Progress on front-end electronics
   c. Progress on algorithms for real-time tracking
4. Perspective
5. Conclusion

Trench geometry and Tools for full-3D simulation

- **Total charge deposit for MIP ≈ 2 fC**
- **Full depletion @ less than 100 V**
- **55x55 μm²: TIMEPIX family-compatible pitch**

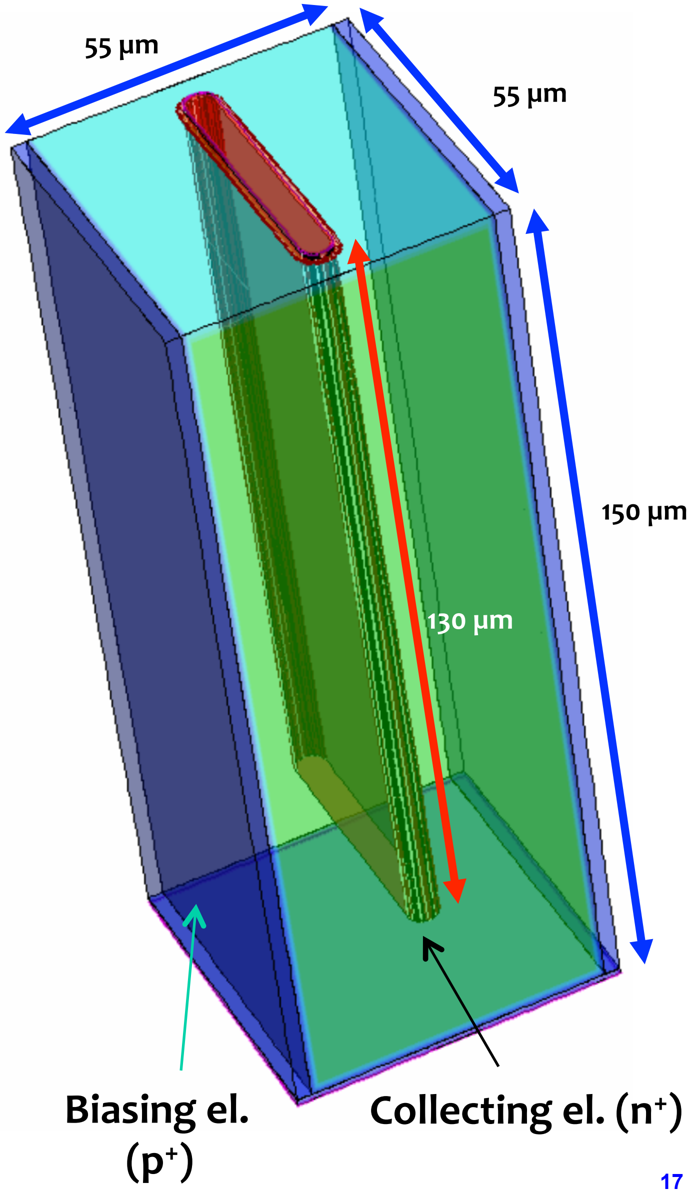


https://github.com/MultithreadCorner/Tcode

Induced current signal simulation:

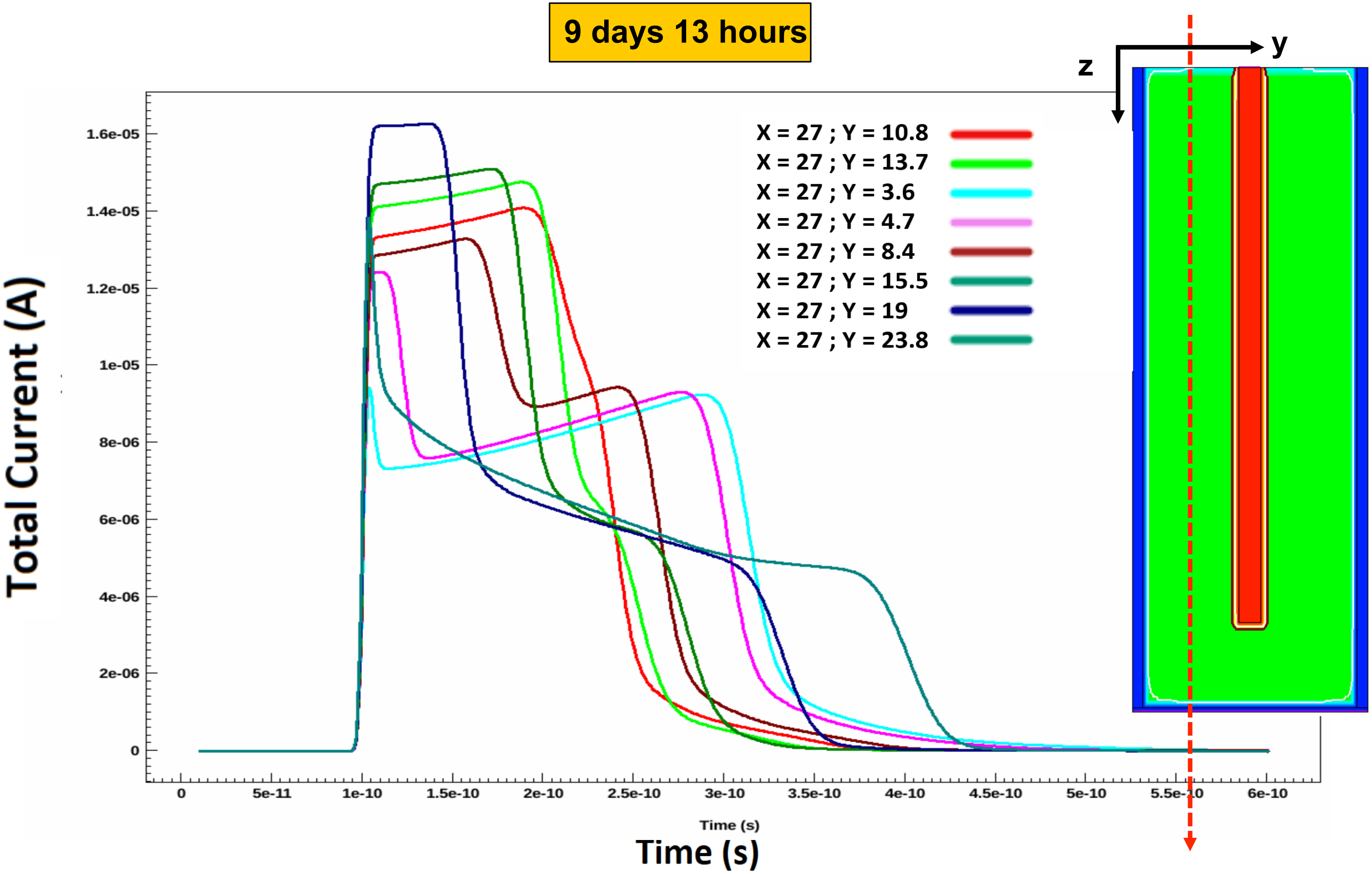
1. **dE/dx detailed physics for MIP (Geant4)**
2. **Detailed E field and mobility maps (e.g. TCAD)**
3. **Induced signal evolution (carrier transport):**
   - **Sentaurus TCAD: > 30 h* for 1 signal and no secondary particles on a 24-cores machine.**
   - **(Custom) TCODe: < 1 min for full simulation.**

**with very accurate and clever meshing*

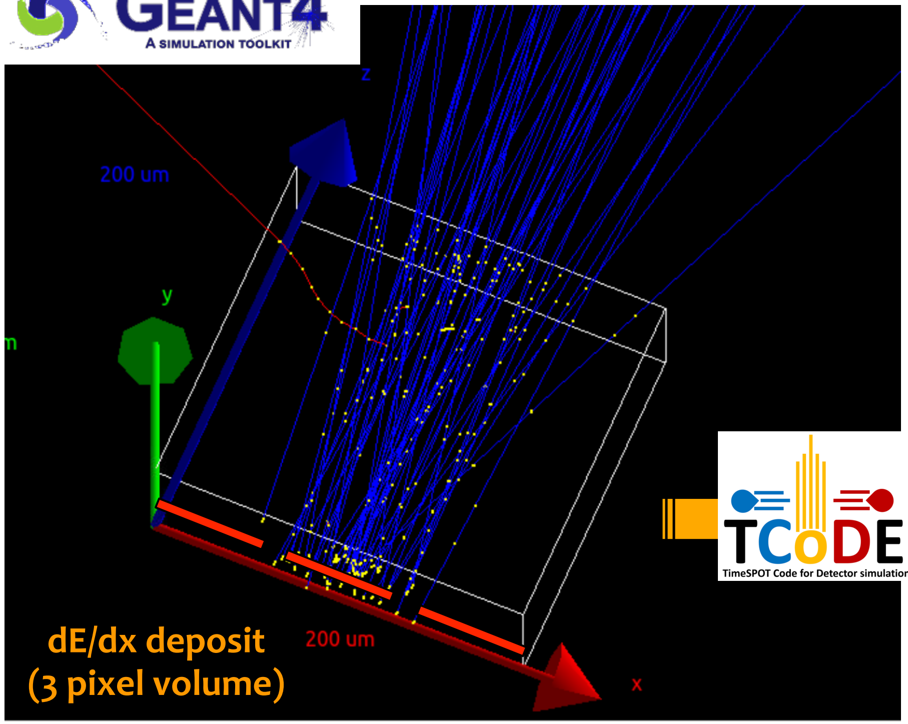


Signals: 2D on yz cut (TCAD)
(simplification for processing-time reasons)

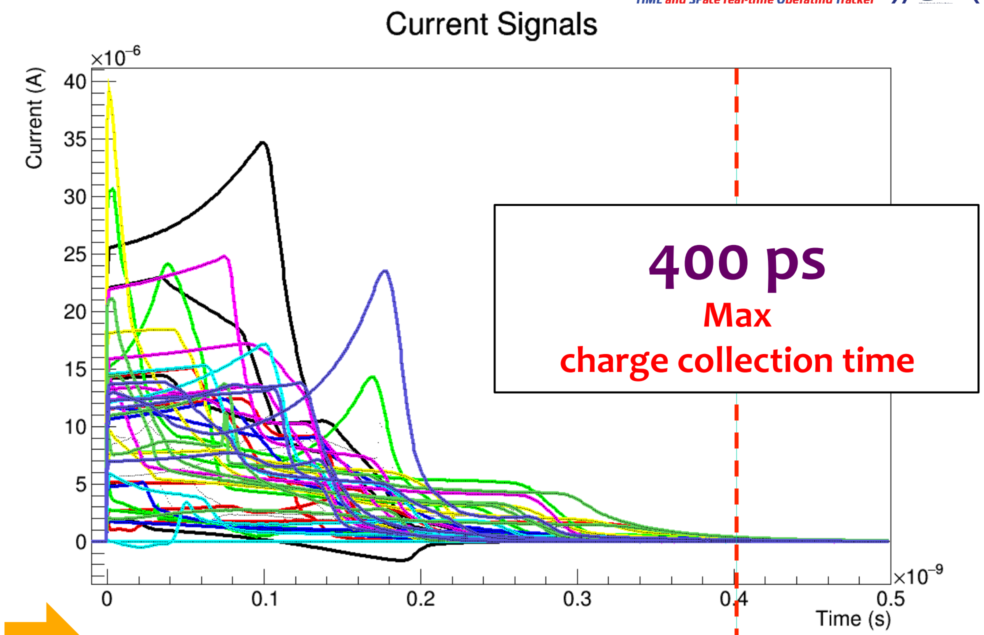
9 days 13 hours

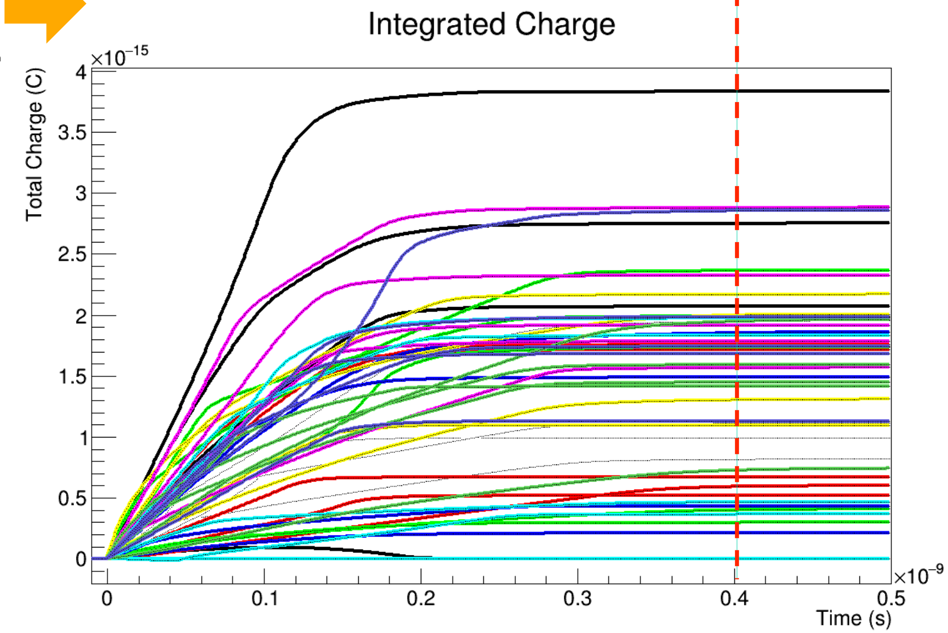


Signals: full-3D model. “Statistics”



TimeSPOT Code for Detector simulation

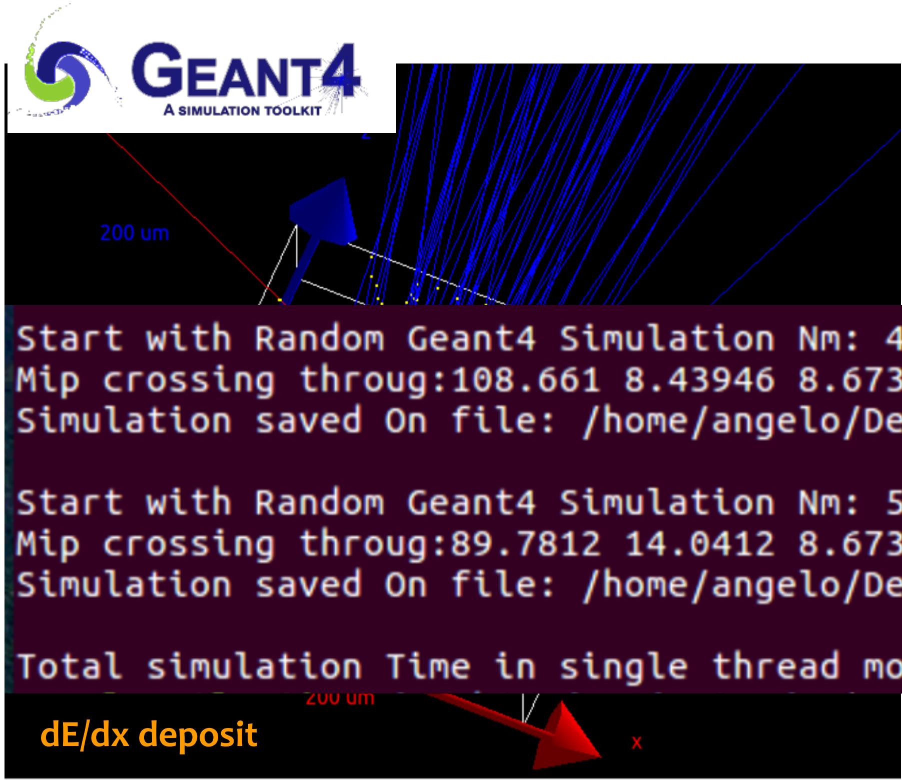




50 tracks.
Induced current signals calculated by TCODE.
(Input to F/E Electronics model)

A. Contu, A. Loi – INFN Cagliari

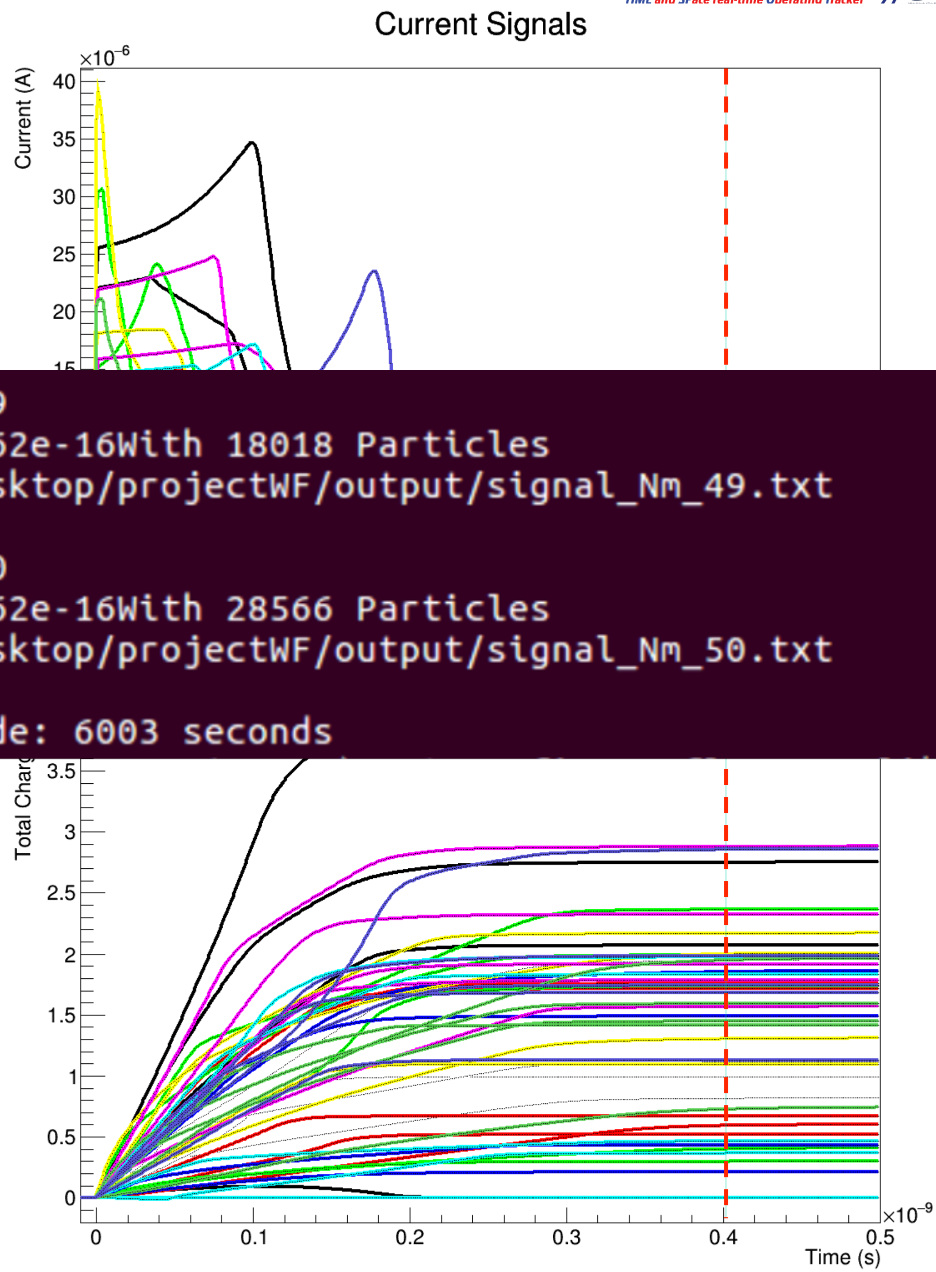
Signals: full-3D model. "Statistics"




```
Start with Random Geant4 Simulation Nm: 49
Mip crossing throug:108.661 8.43946 8.67362e-16With 18018 Particles
Simulation saved On file: /home/angelo/Desktop/projectWF/output/signal_Nm_49.txt

Start with Random Geant4 Simulation Nm: 50
Mip crossing throug:89.7812 14.0412 8.67362e-16With 28566 Particles
Simulation saved On file: /home/angelo/Desktop/projectWF/output/signal_Nm_50.txt

Total simulation Time in single thread mode: 6003 seconds
```

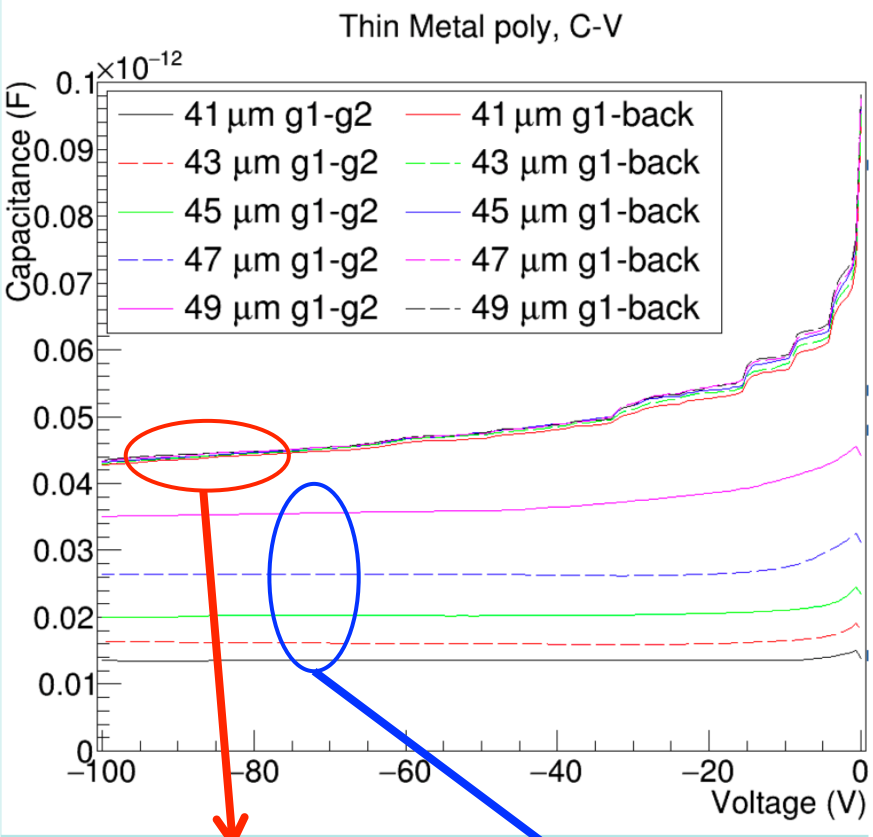


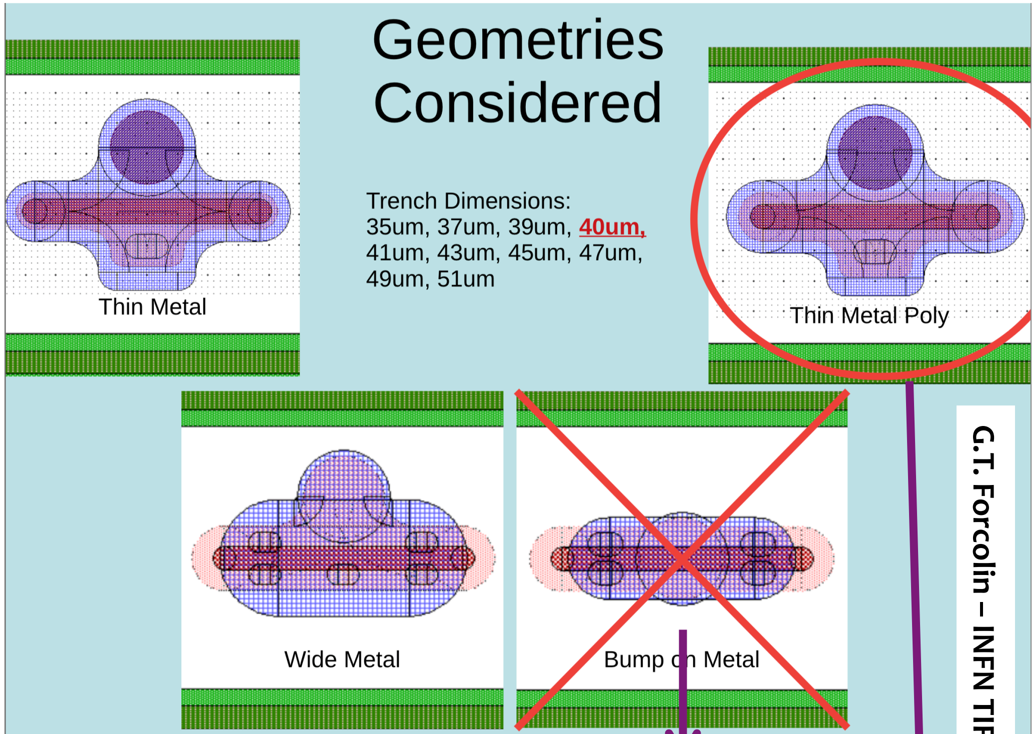
A. Contu, A. Loi – INFN Cagliari

50 tracks
Induced current signals calculated by TCODE
(input to F/E electronics model)

1h40' in ST (Intel®Xeon®CPU X5450 – 10 GB RAM)
1'40" on a gaming laptop in MT
2-3 months on TCAD (estimate)

WP1: 3D silicon sensors
Design rules and executive layout





G.T. Forcolin – INFN TIFPA

Opposite electrode capacitance

Inter-pixel capacitance

Discarded after technology tests

Choice for minimum capacitance (compatible with good E field uniformity and established design rules): 40 µm, 2 µm poly, thin metal poly

3D silicon sensors
Fabrication: Technology tests at FBK

3D trenched geometry is a new technology !!!

Some attempts on hexagonal trenches ad CNM (2013)*: ≈ Working, but very high leakage current → Tests @ FBK from July to December 2018.

"Simulation" of litho process

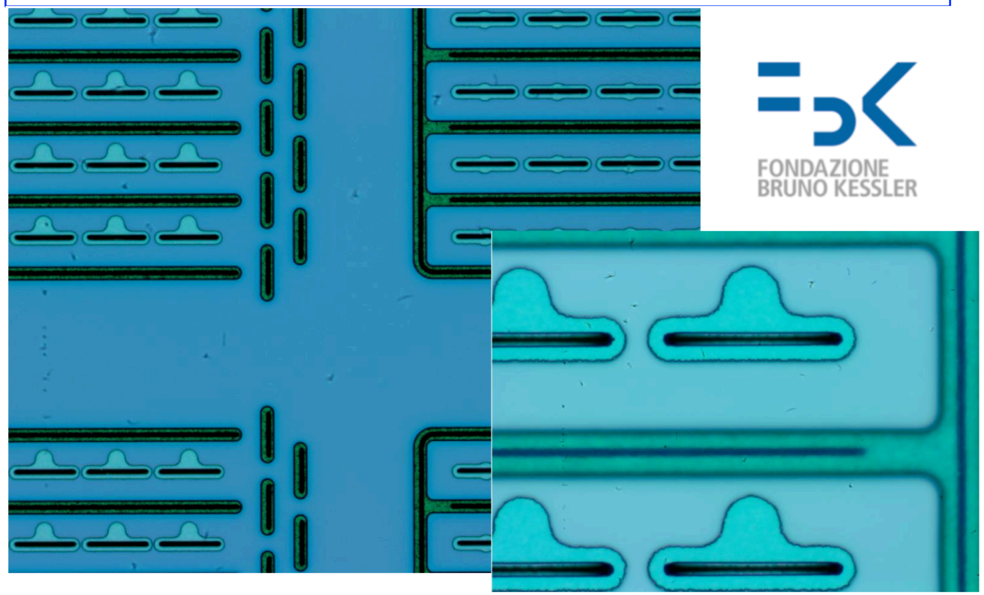
1. Oxidation
2. Definition and attack of ohmic trenches (Deep Reactive Ion Etching)
3. Deposition of poly-Si on ohmic trenches
4. Definition of poly-Si on ohmic trenches
5. Definition and attack of junction trenches (DRIE)
6. Deposition of poly-Si on junction trenches
7. Definition of poly-Si on junction trenches

8. TEOS deposition
9. Opening of contacts
10. Metal deposition and definition

Results

Litho trenches:
750 nm Oxide + 6 μm Vacuum bake Resist + DRIE:
→ yield 100%

Optimized recipe:
for DRIE: 160 μm (ohmic) and 135 μm (junction)
for poly: 3000 nm



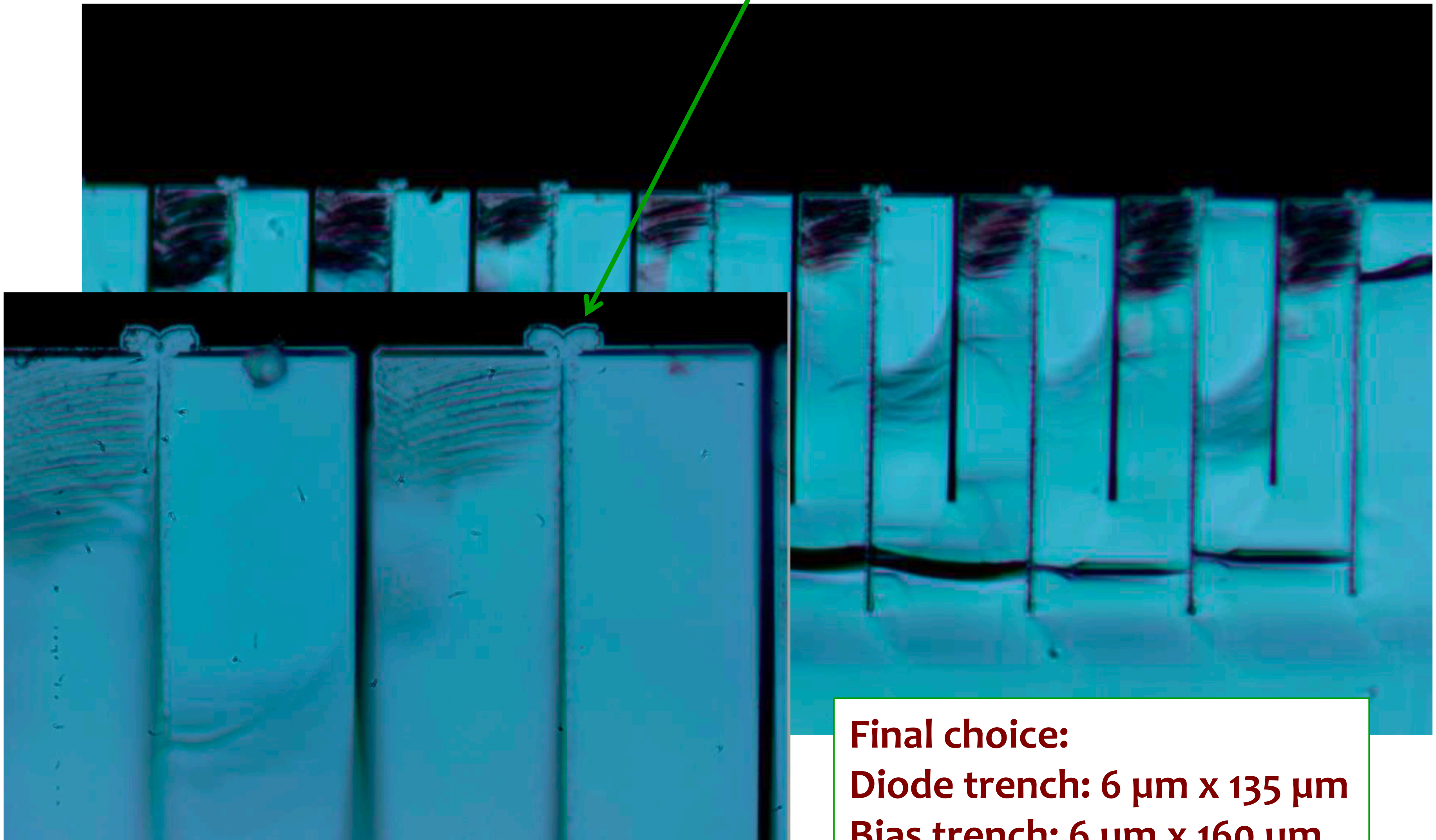
FONDAZIONE BRUNO KESSLER

A. Montalbano et al., NIMA 765 (2014), 23

Trenches

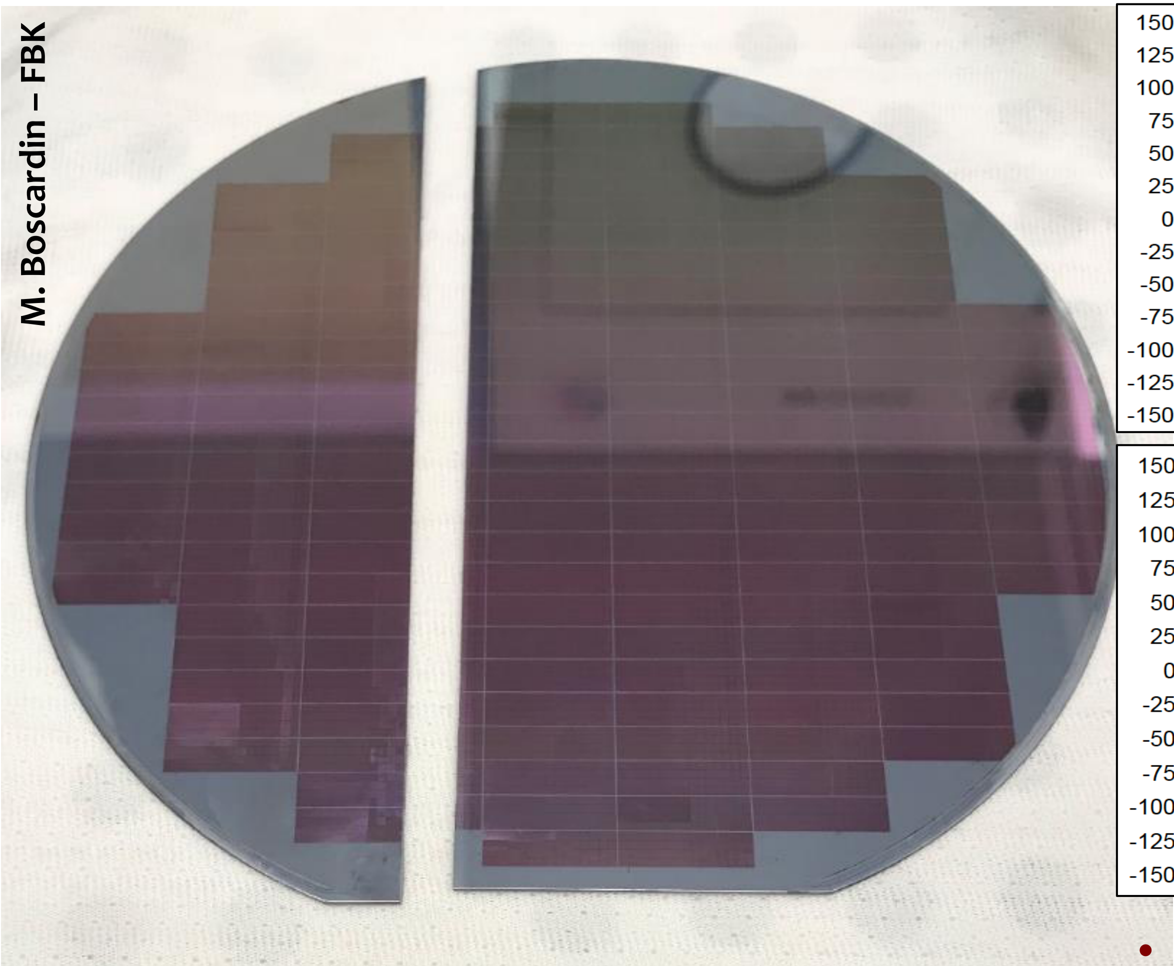
After poly dep (wrong attempt)

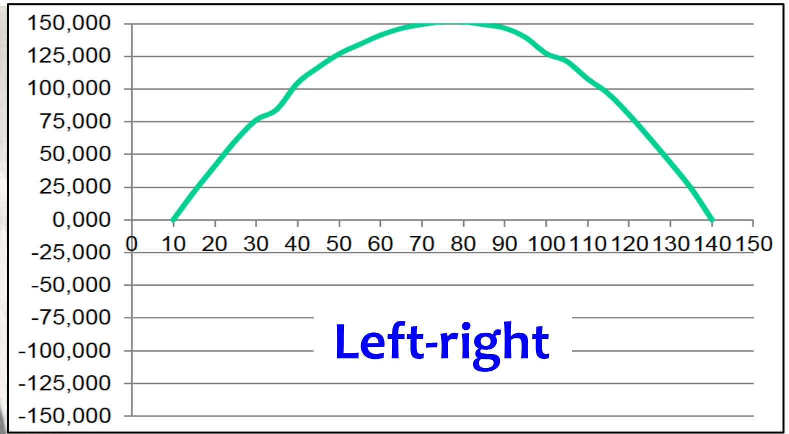
M. Boscardin – FBK

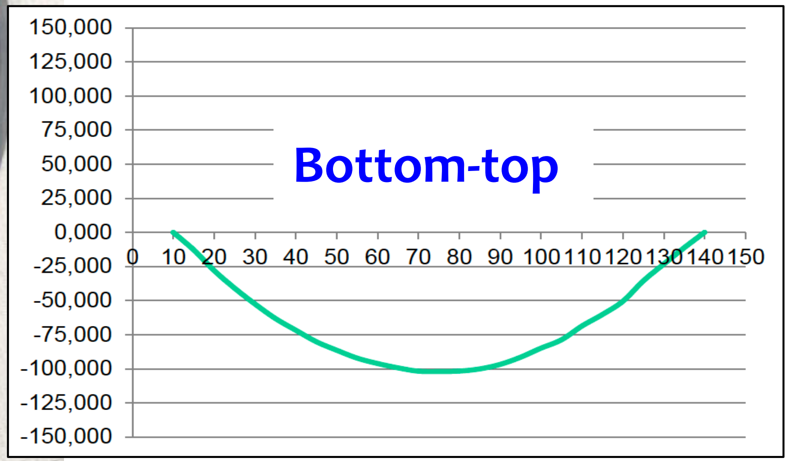


Final choice:
Diode trench: 6 µm x 135 µm
Bias trench: 6 µm x 160 µm

1st wafer prototypes and fabrication issues







- Mechanical stress.
- Wafer bowing
- Frequent breaking after attack and filling of ohmic trenches

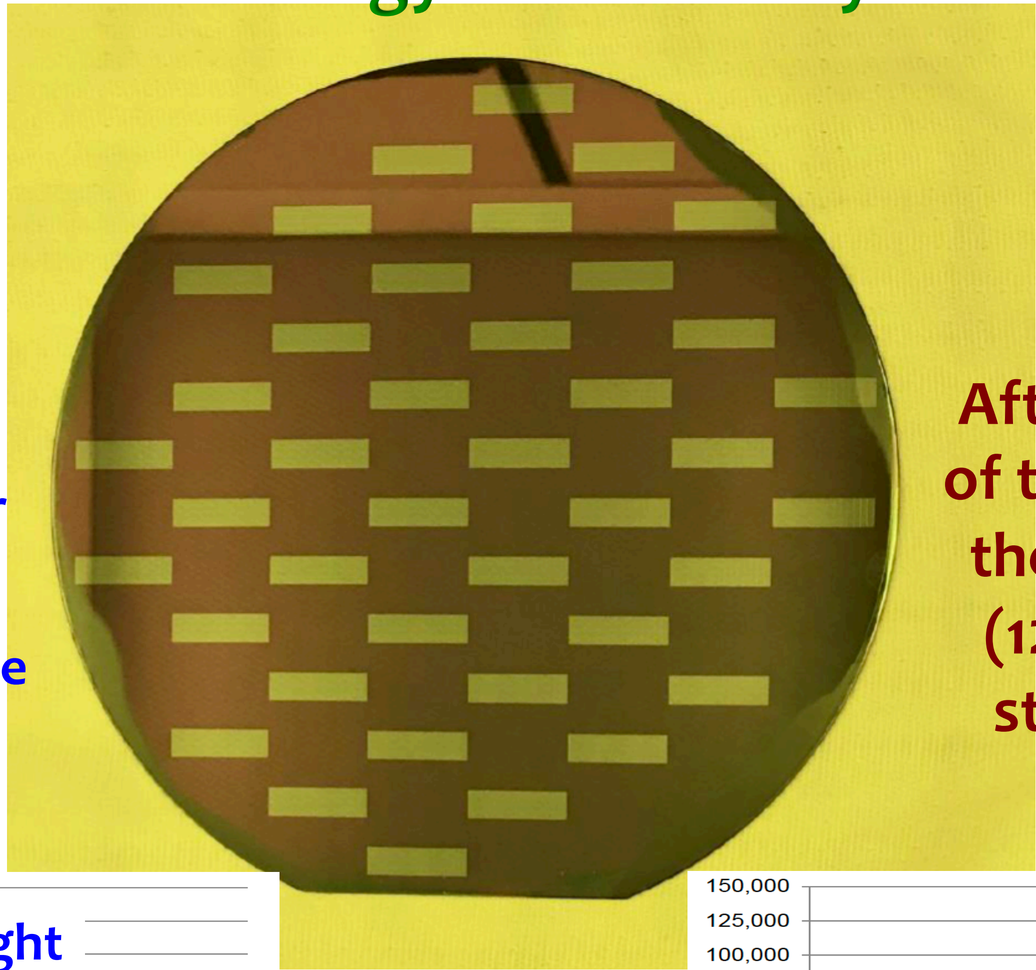
Low mechanical yield

Wafers tend to break !!

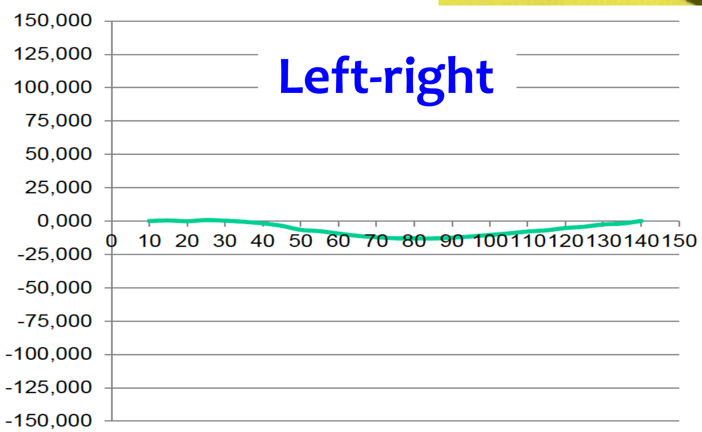
M. Boscardin – FBK

New strategy for wafer layout

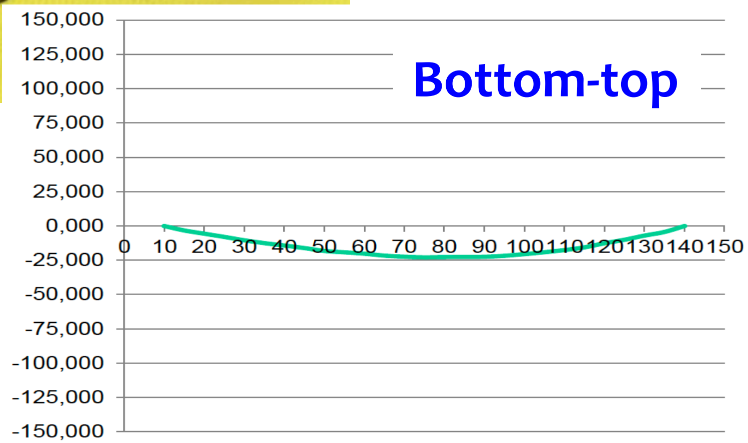
- Improved version (sparser modules)
- Not very suitable for mass production



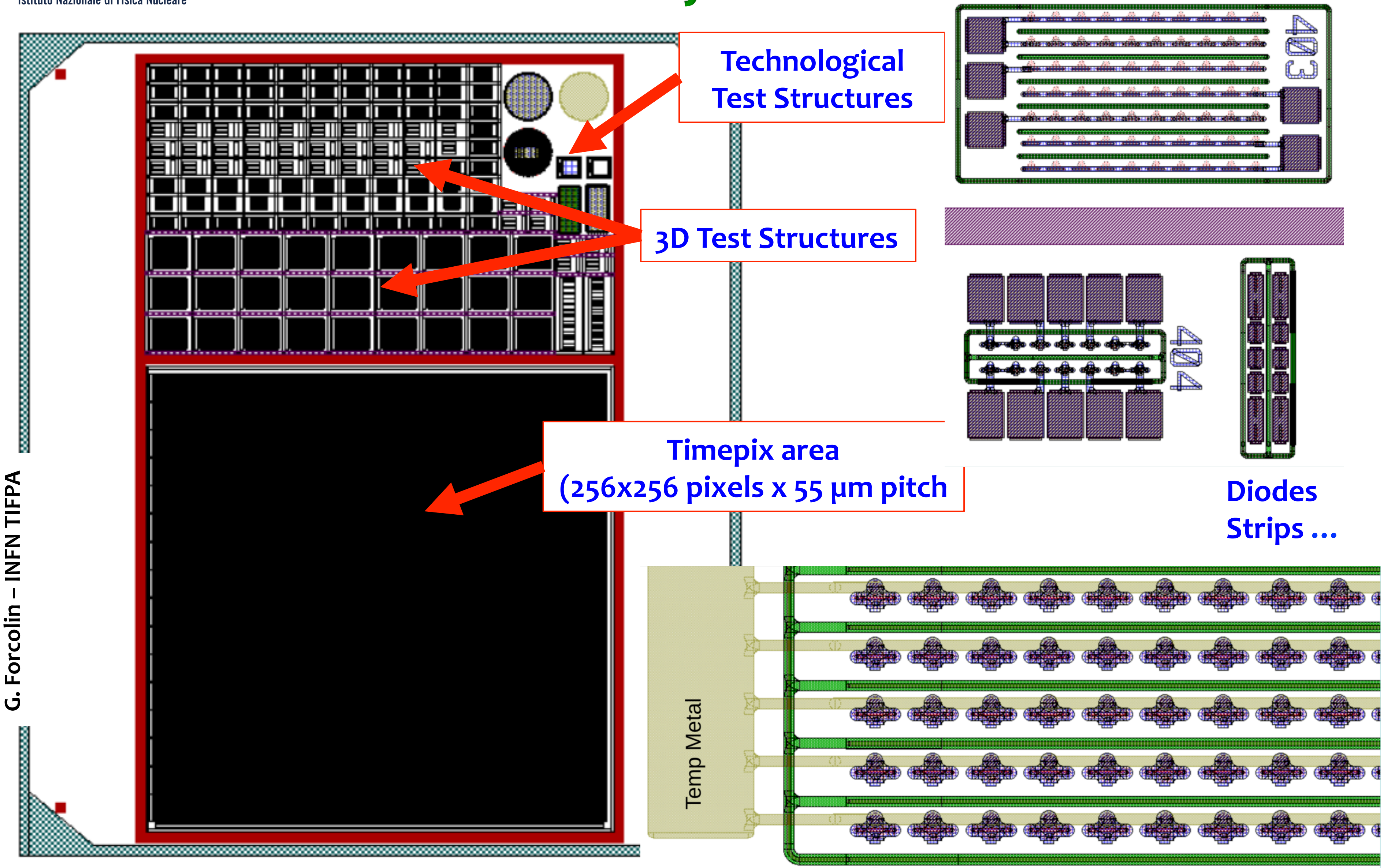
After fabrication of test structures, the 1st batch run (12 wafers) has started mid of January



Wafer bowing highly mitigated

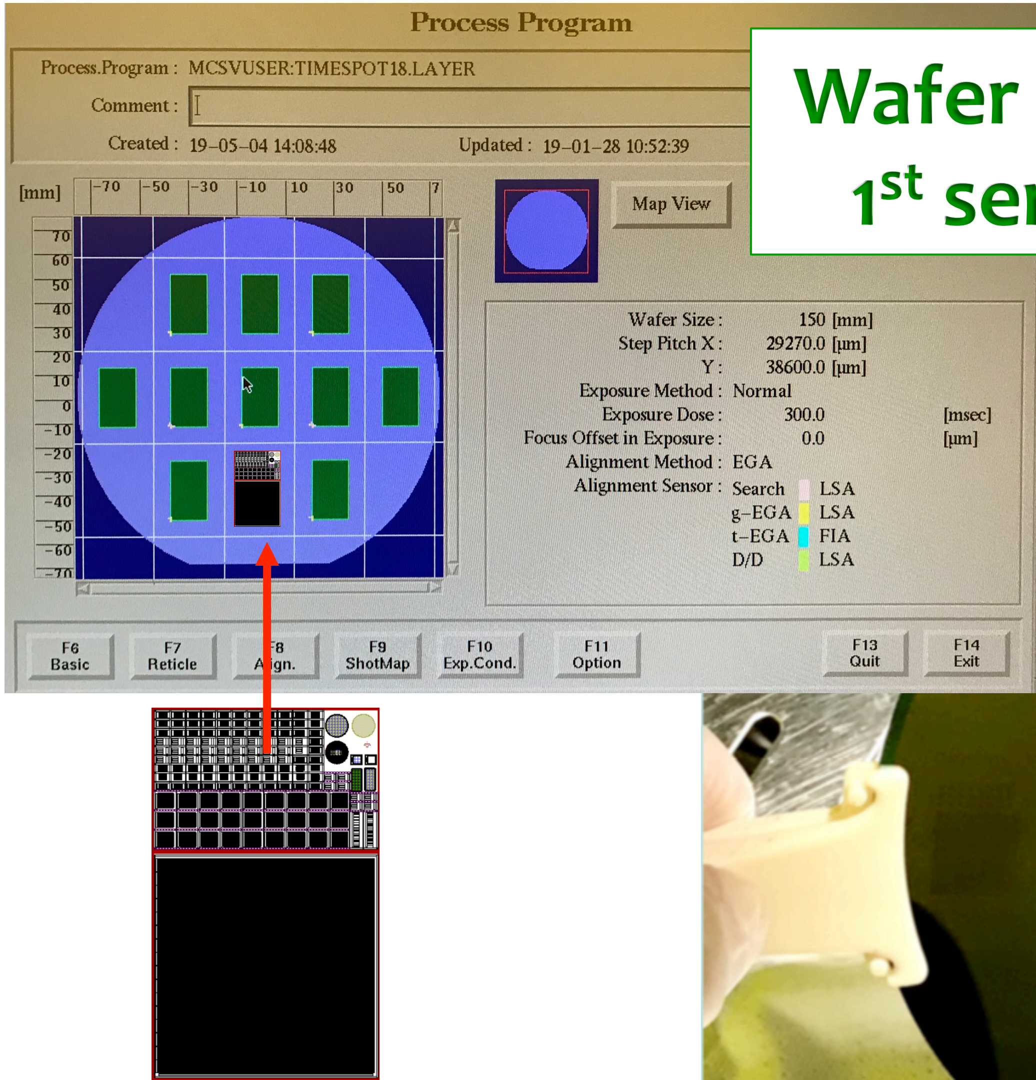


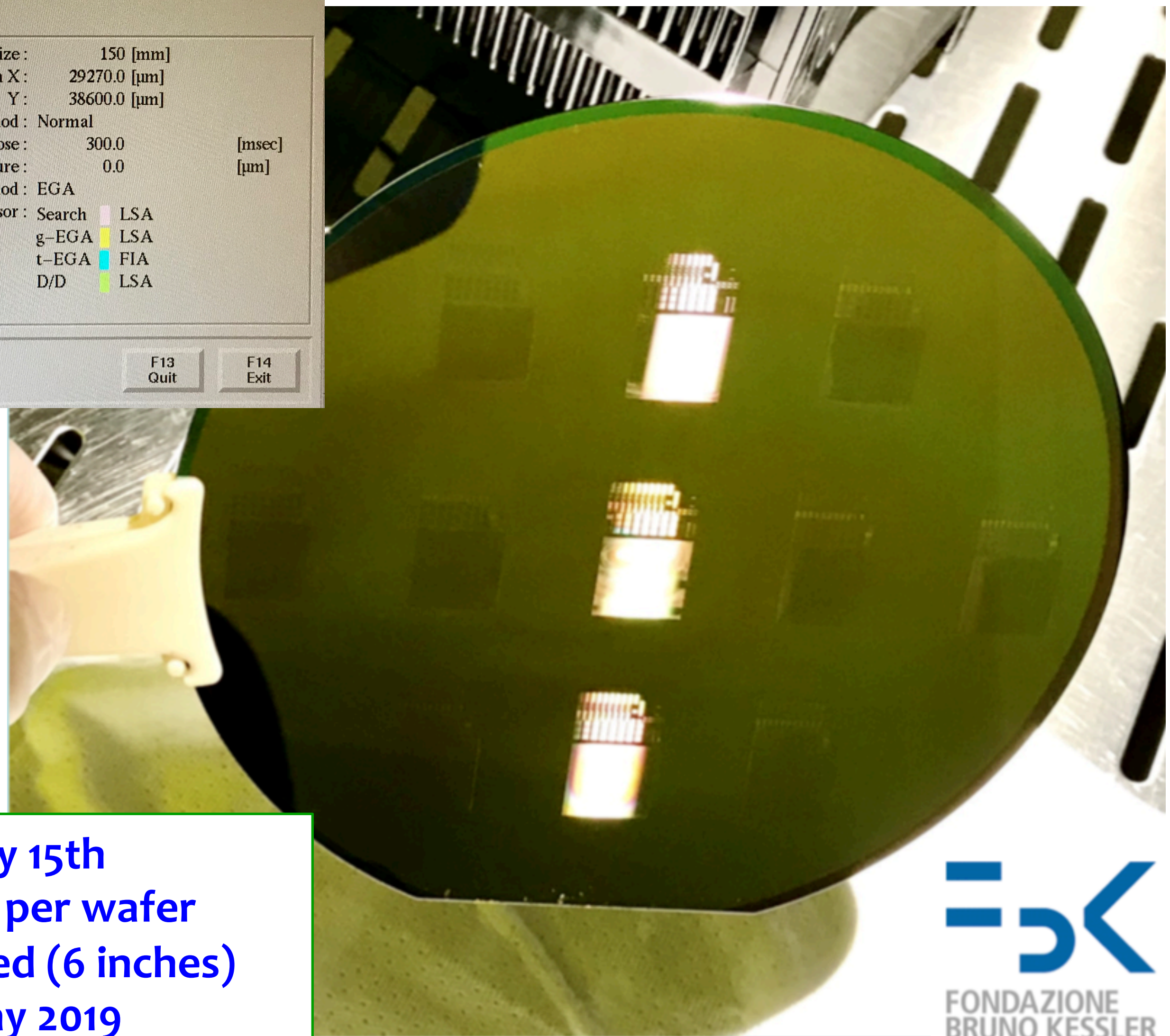
Production reticle for first production
Final layout



G. Forcolin – INFN TIFPA

Wafer production: 1st sensor batch





Started ~ January 15th
11 testable structures per wafer
12 wafers to be produced (6 inches)
Completion: ~ May 2019

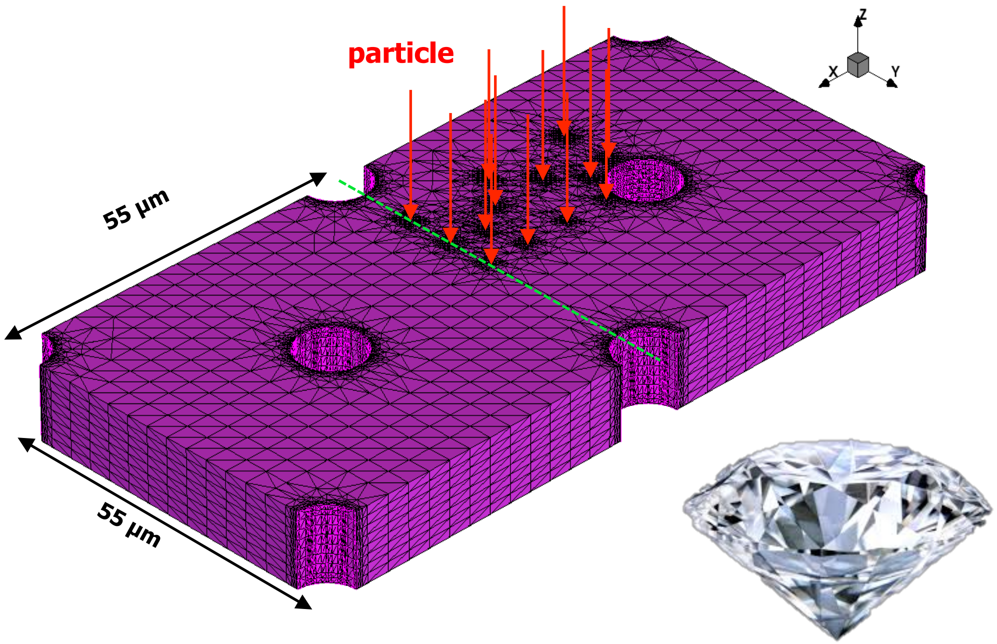
WP2: 3D diamond sensors

Firenze, Perugia

Silicon vs Diamond in radiation detection

	Silicon	Diamond	
Bandgap [eV]	1,12	5,47	Higher-Field operation
Breakdown Field [MV/cm]	0,4	20	
Intrinsic Resistivity@R.T. [Ω cm]	$2{,}3\times10^5$	$> 10^{11}$	lower leakage current
Intrinsic Carrier Density [cm^{-3}]	$1{,}5\times10^{10}$	10^{-27}	
Dielectric Constant	11,9	5,7	
Electron Mobility	1350	1900-3800	faster signal
Hole Mobility	480	2300-4500	
Saturation Velocity	1×10^7	$2{,}7\times10^7$	
Displacement Energy [eV/atom]	13-20	43	radiation hardness
Thermal Condutivity [W cm^{-1} K^{-1}]	1,5	20	heat dissipation
Energy to create e-h pair [eV]	3,62	11,6 - 16	
Radiation Length [cm]	9,36	12,2	
Energy Loss for MIPs [MeV/cm]	3,21	4,69	lower signal
Aver. Signal Created / 100 µm	8892	3602	

Already realized with success for dosimetric applications (3Dose – CSN5)



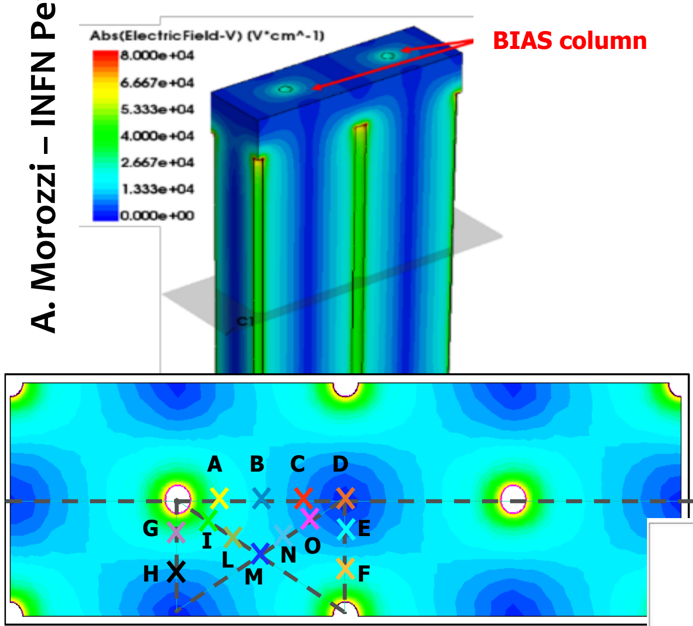
- Very promising characteristics for timing
- Lower signal can be partially compensated by larger thickness
- S/N ratio still favourable
- 3D structure decreases collection time and capture probability by defects

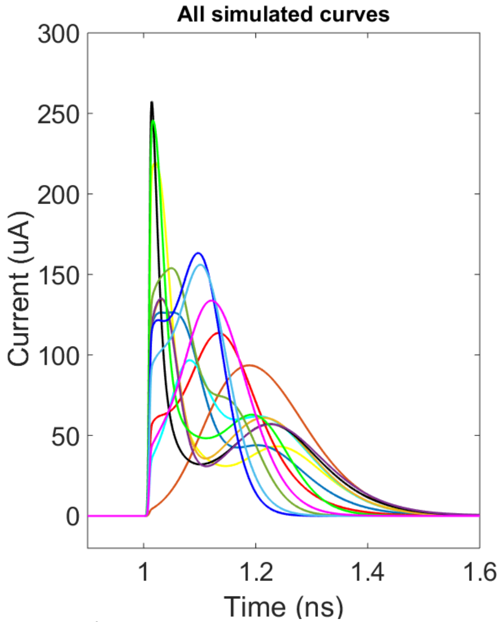
TIMESPOT plan:
Realize a silicon-geometry-compatible device and read-out it with the same pixel electronics, changing only the very first stage (programmable impedance and gain)

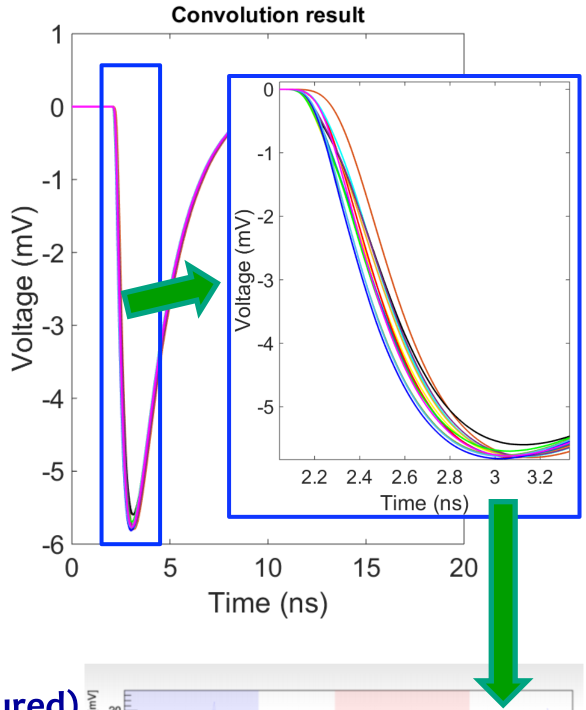
WP2: Simulation and optimization activities

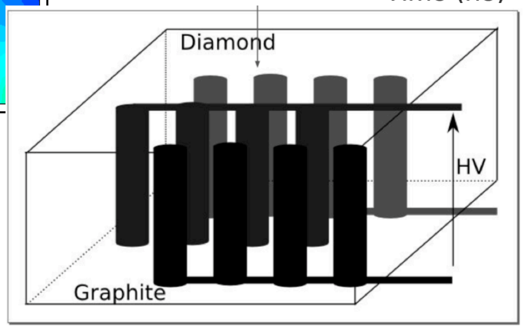
A. Morozzi – INFN Perugia

Experimental Set-up: ^{90}Sr source (≈ MIP generated charge)

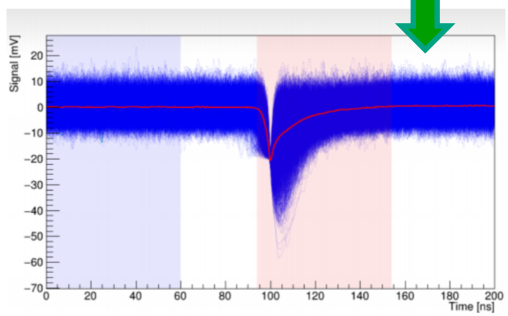








σ_t (measured) ≈ 240 ps (strips of columns: high C, high noise)



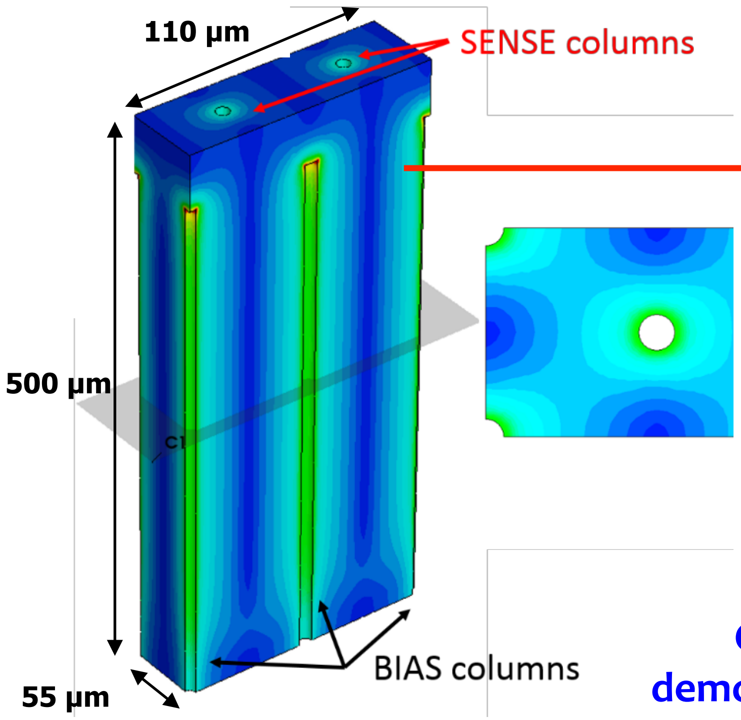
L. Anderlini – INFN Firenze

Moreover:

- Optimization of column distribution (field uniformity and CCE)
- Optimization of column aspect ratio (R vs C trade-off)
- Optimization of sensor geometry (idea to realize trenches: post-poned to results on columns)
- Many inputs from Perugia to 3D Silicon modelization activities

WP2: 3D diamond sensors

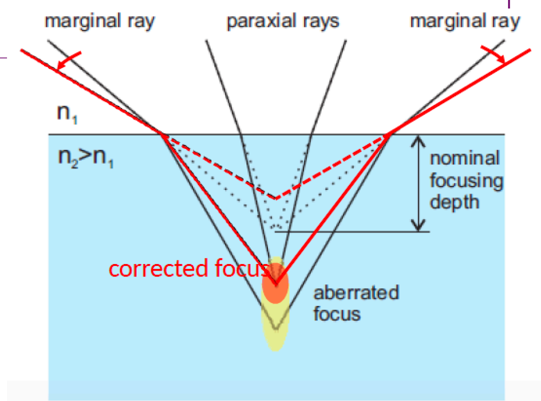
The key to success (or failure)



The problem is graphite(zation), not diamond

Typical column resistance ~ 100-10 kΩ

S. Lagomarsino et al., Diamond Relat. Mater., 43:23–28, 2014.



Other groups (Oxford* 2014) demostrated that electrode resistivity can be considerably lowered from some Ω cm to 0,022 Ω cm by removing optical aberrations in laser focusing during the graphitization process.

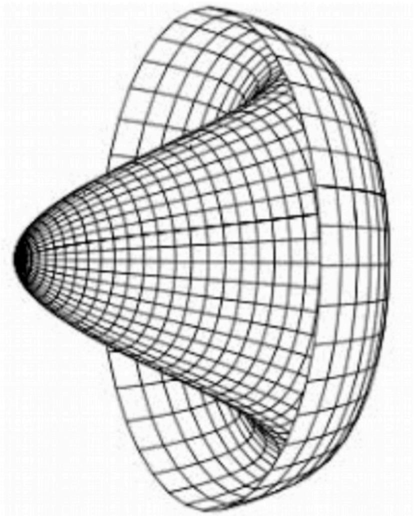
***Oxford, Manchester, Ohio Universities – the world best in this field – use a setup costing as much as the complete TIMESPOT budget ;-))**

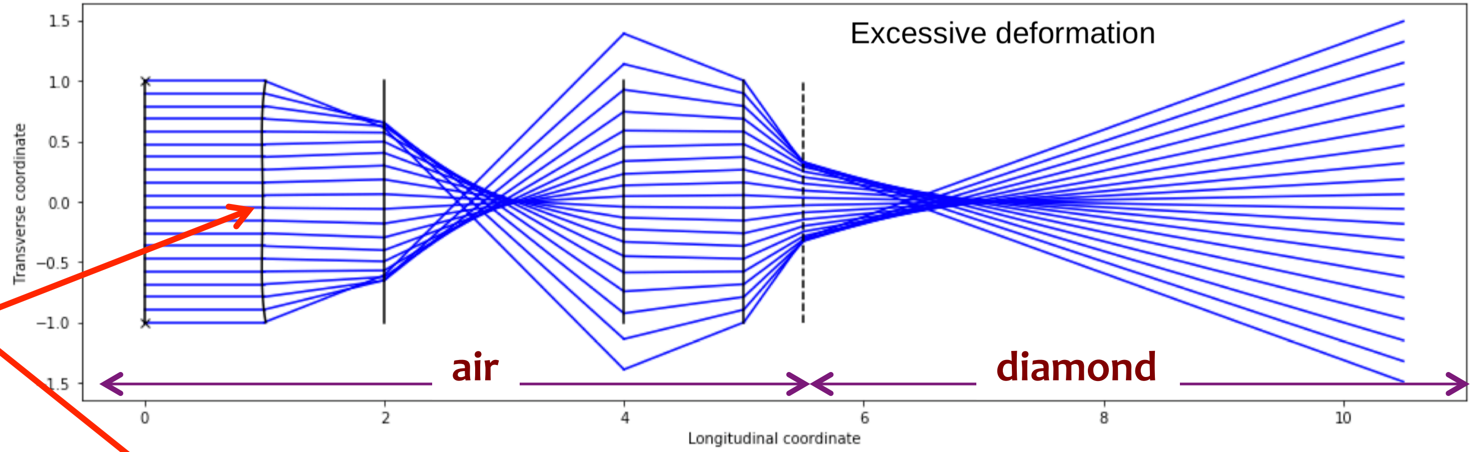
TIMESPOT proposes an alternative technique for correcting aberrations at a much lower cost than the real-time adaptive wave-front control

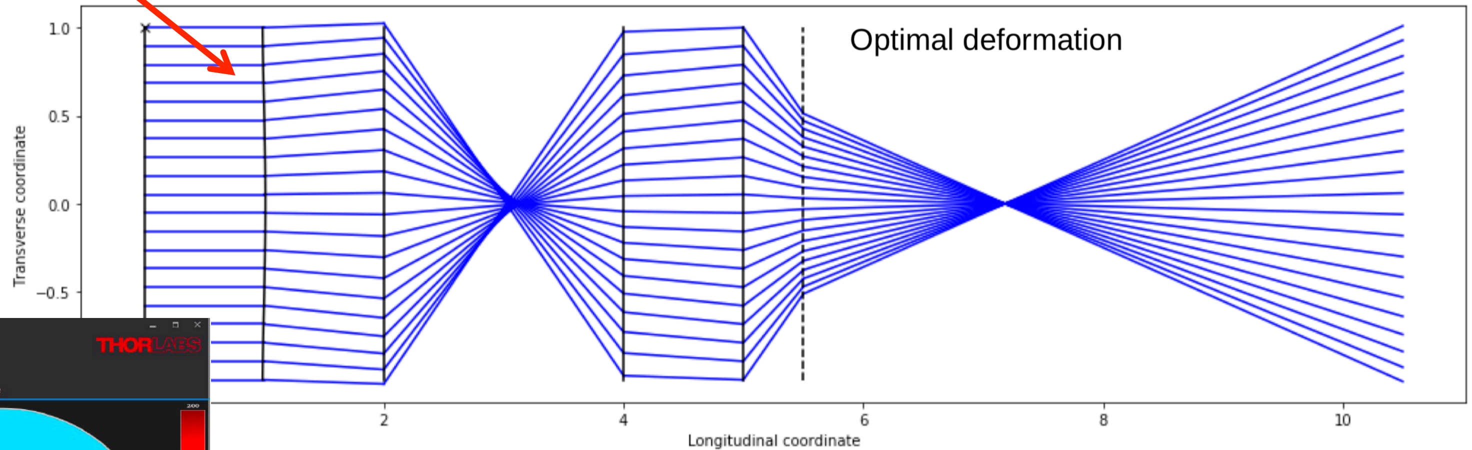
TIMESPOT starting point (April 2018): R = 53 kΩ, ρ = 2.35 Ωcm

WP2: Spherical aberration

Istituto Nazionale di Fisica Nucleare

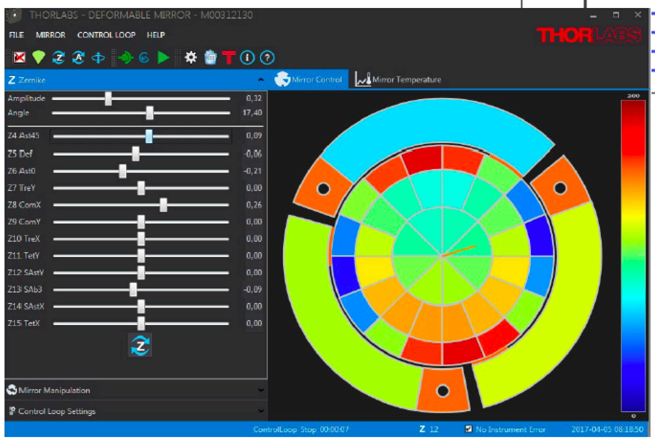






$$\sqrt{5}(6\rho^4 - 6\rho^2 + 1)$$

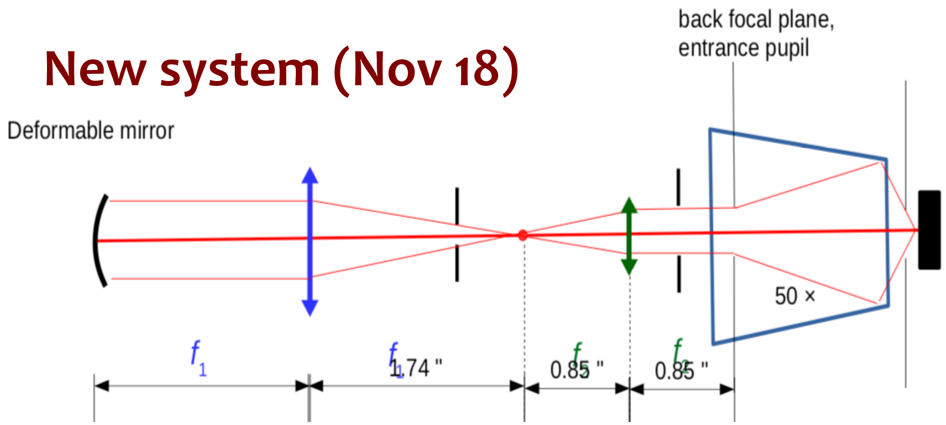
Zernike polinomials

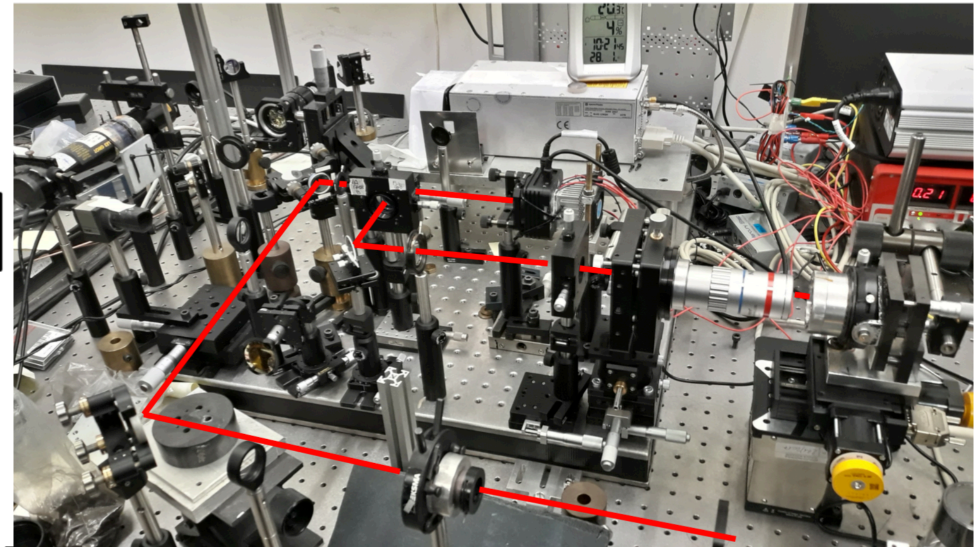


- A deformable mirror (mexican hat shape) can compensate for aberrations
- Theoretically the shape depends only on ρ
- Practically depends on many other critical (and nasty) parameters as alignment, tilting and temperature variations

WP2: Graphitization setup

New system (Nov 18)

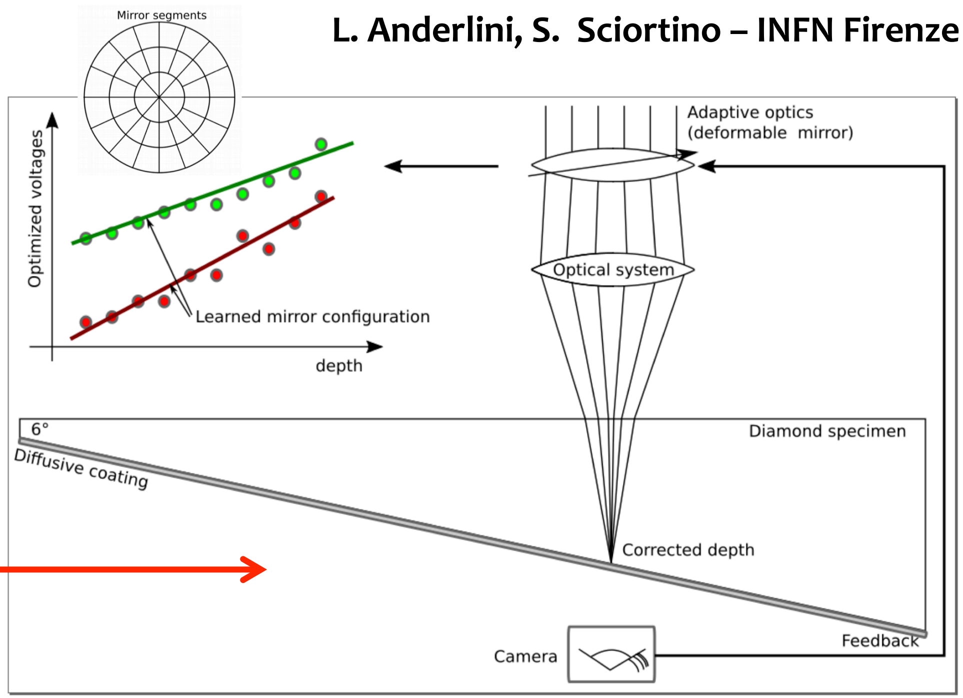




50× objective, large NA (0.67), 4*f* system, PI linear stages, He-Ne laser pointer

- stabilization in temperature of the deformable mirror
- optimization of the deformable mirror configuration
- timing measurement setup (new boards with aperture)
- columns at different energy per pulse and focus displacement velocity

L. Anderlini, S. Sciortino – INFN Firenze

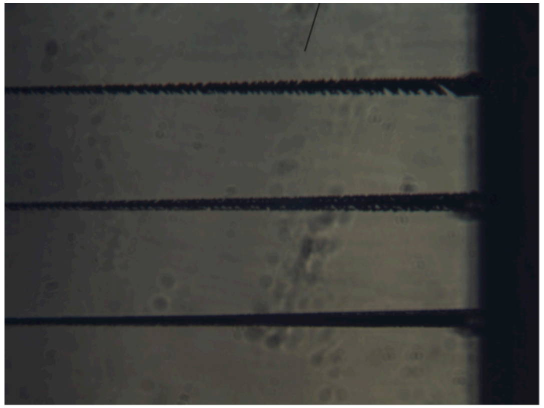


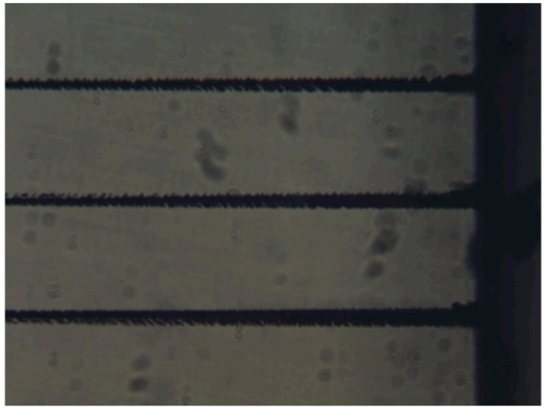
The optimal configuration of the mirror is "learned" on a diamond specimen of variable depth

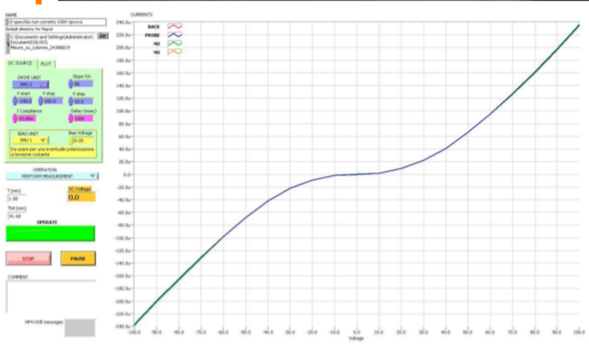
WP2: Results on column R

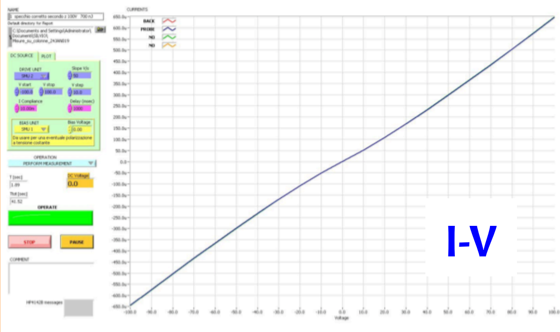
L. Anderlini,
S. Sciortino
INFN Firenze

Laser beam @ 0.7 μJ	without correction			with correction		
Growing speed (μm/s)	R (kΩ)	diam. (μm)	ρ (Ωcm)	R (kΩ)	diam. (μm)	ρ (Ωcm)
20	417	5.9	2.07	150	5.6	0.67
10	370	4.8	1.22	196	5.75	0.92
10	–	–	–	168	6.43	0.99









Results are very positive (a factor ~2 is gained in R, column quality has visibly improved)

Still far from the target (ρ ≈ 0.05 Ωcm)

Some gain margin with the present setup (additional factor 2-5?)

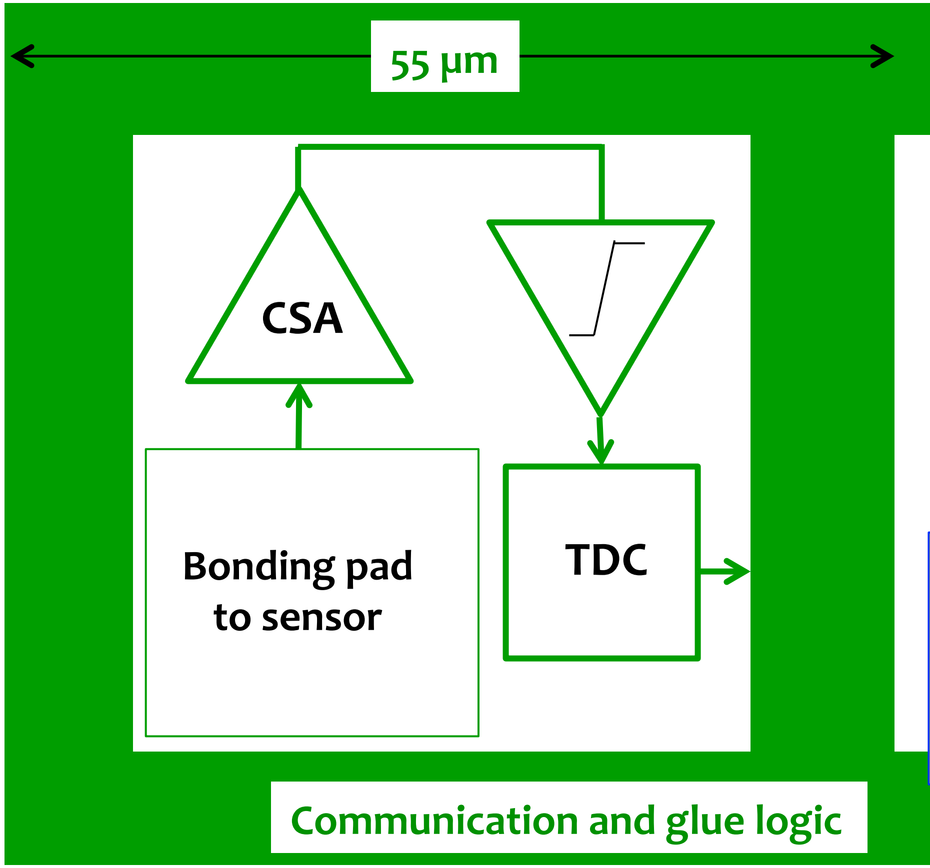
Is our low-cost setup basically inadequate?

Outline

1. Why 4D ? Why timing?
2. Aim and Structure of the project: organization in Work Packages
3. Why 3D sensors ?
4. 2018 activity and first results
    a. Progress on sensor developments
    b. Progress on front-end electronics
    c. Progress on algorithms for real-time tracking
4. Perspective
5. Conclusion

Pixel read-out electronics

- Pixel ROC for 4D tracking require a binary readout (with high resolution in time) and one TDC per pixel (or group of pixels)
- The first approach is to rescale a classic circuit (CMS RD53 style) to our purposes, adding a TDC per pixel



RD53 is a CMOS 65-nm: not enough !

→ CMOS 28-nm

F/E requirements:

- Keep the resolution below 100 ps rms or (better) as close as possible to sensor intrinsic performance (≈ 20 ps)

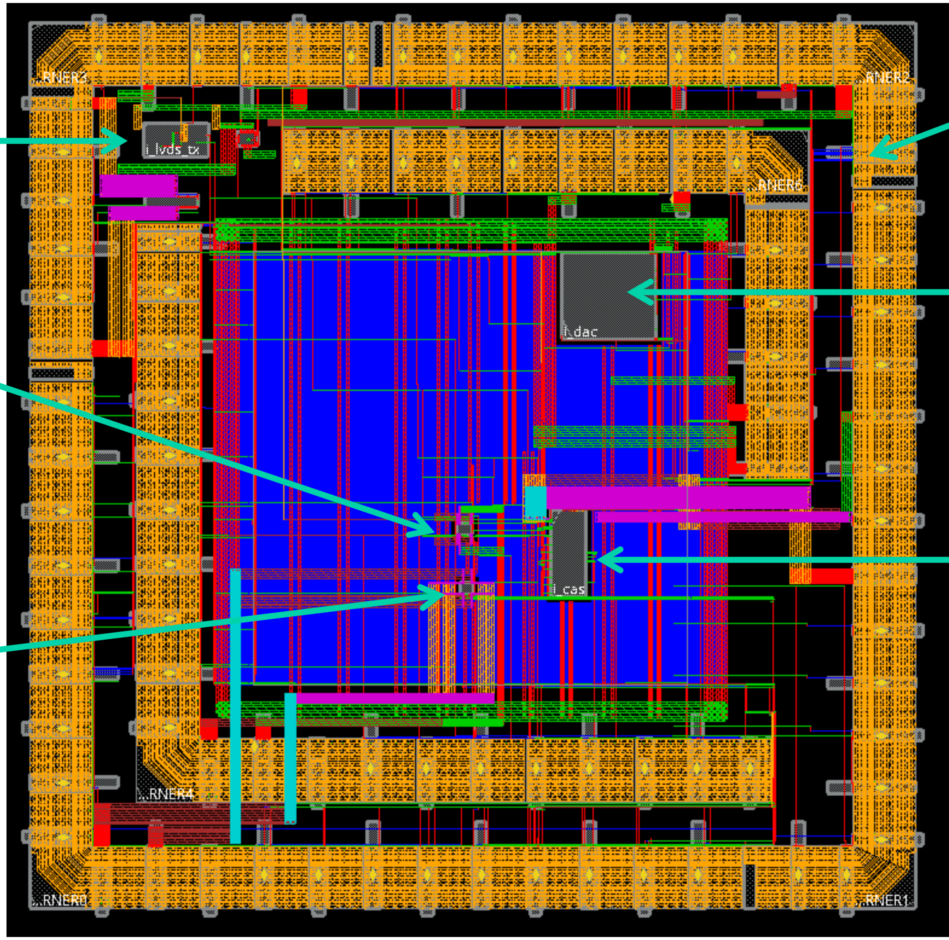
Present benchmark in pixel ROC with timing:
TiMEPIX4 200 ps time resolution (advanced stage of design)

1^{st} prototype chip

(submitted end of October, dies back ~ NOW)

- Main purpose: gain confidence on 28-nm CMOS and test technology performance.
- All cells are kept independent and directly accessible from external pins (with a few exceptions)

→ strongly pad-limited



LVDS Tx/Rx

OPAMP

6-bit DAC + SPI I/F

TDC1 (dithering)

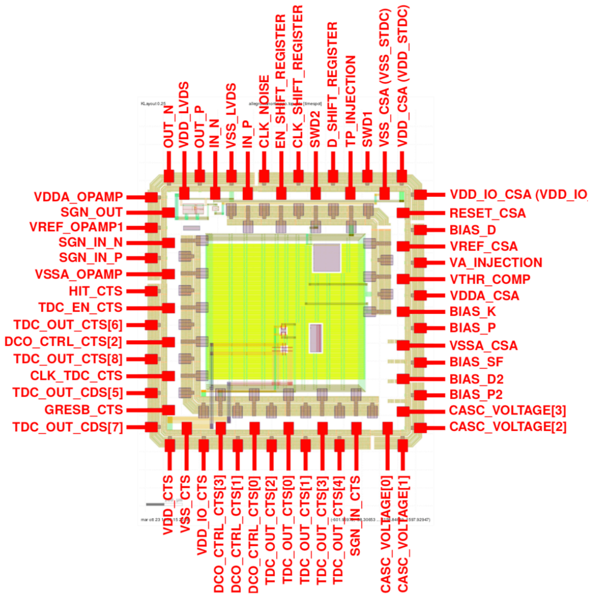
TDC2 (no-dithering)

8-channels CSA+Discriminator programmable power (and speed)

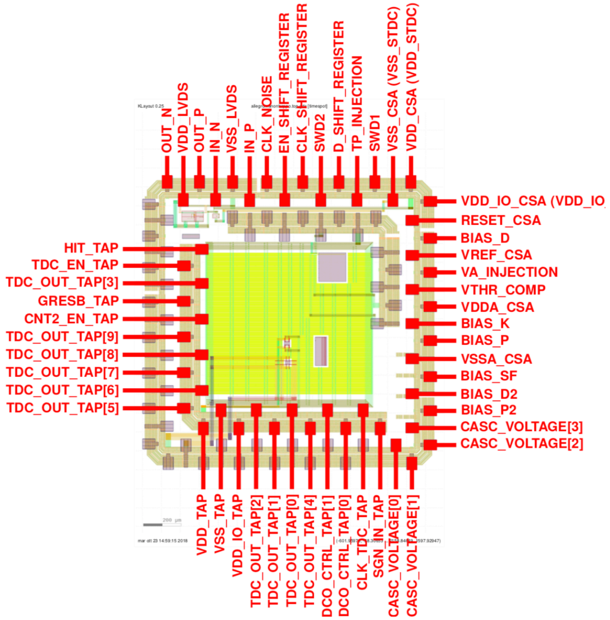
Total area 1.5x1.5 mm^2
mini@sic

In the next version/submission a ≈ 20x20 matrix of pixel ROC is possible

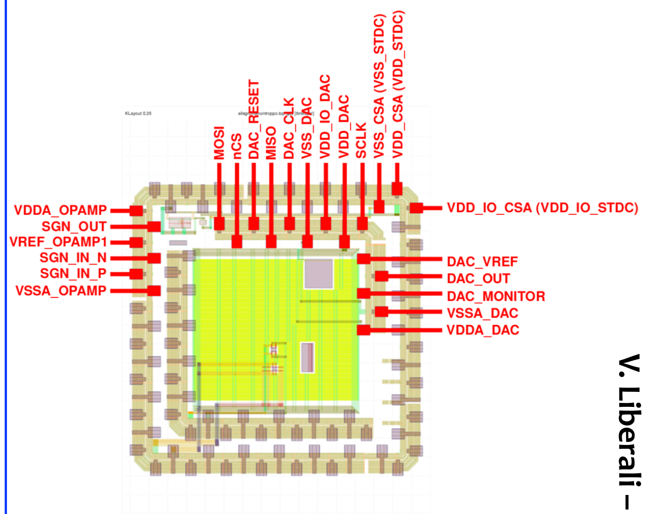
WP3: chip test preparation
1 PCB test, 3 bonding schemes



External frame:
- LVDS
- CSA + discriminator
- TDC CTS
- OPAMP

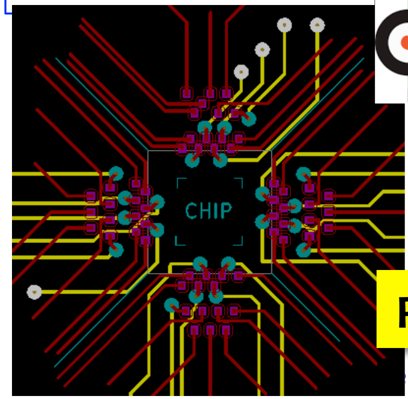


Internal frame (TDC side):
- LVDS
- CSA + discriminator
- TDC TAP



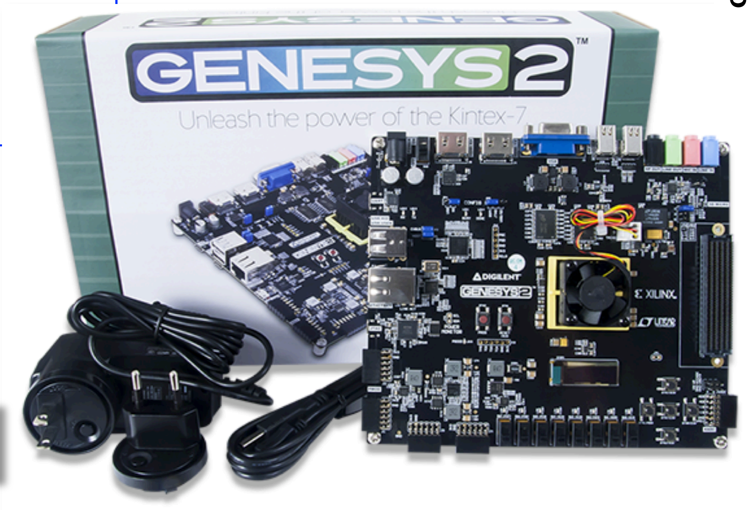
Internal frame (DAC side):
- DAC
- OPAMP

V. Liberali – INFN Milano



NCAB GROUP

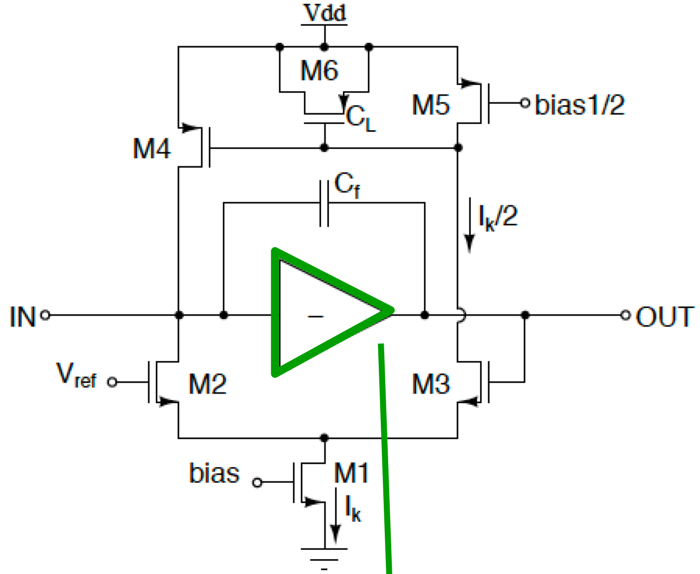
75 μm traces !!

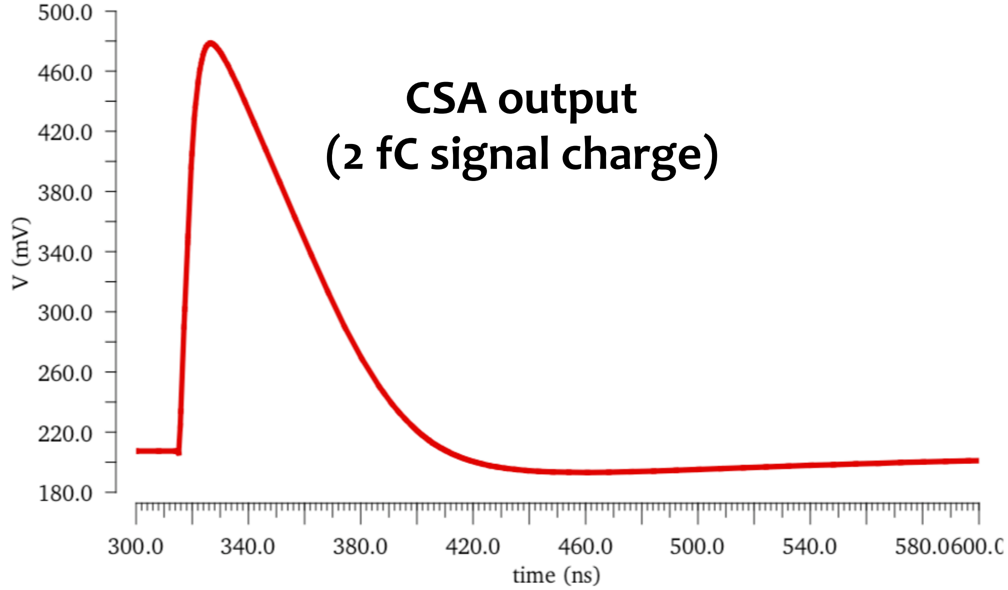


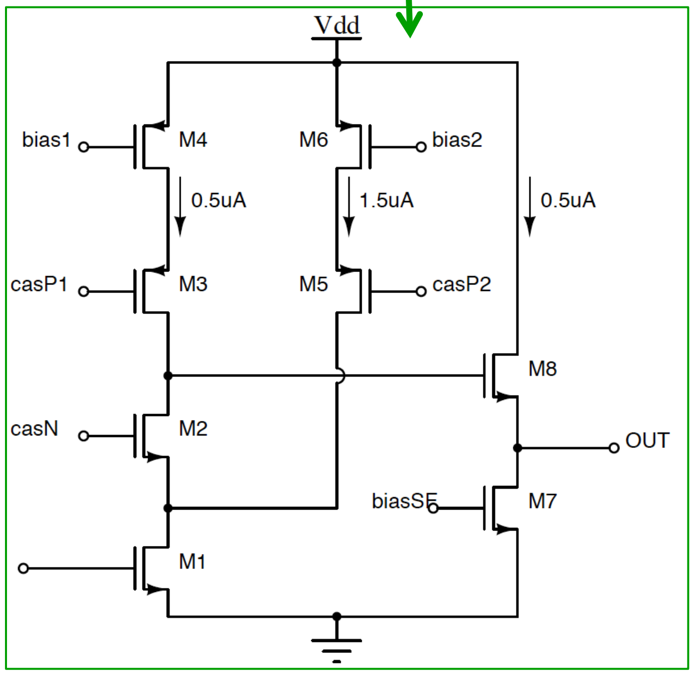
PCB & Bonding by Milano INFN lab

Input stage, CSA (1)

- Output voltage proportional to input charge
- Constant peaking and falling times for better timing (no CR-RC^n shaping)
- Low noise
- Krummenacher (active) filter: DC current compensation of input leakage current (critical?)
- Programmable input MOST current (this prototype)
- Cascodes can be switched on/off to improve S/N ratio (this prototype)

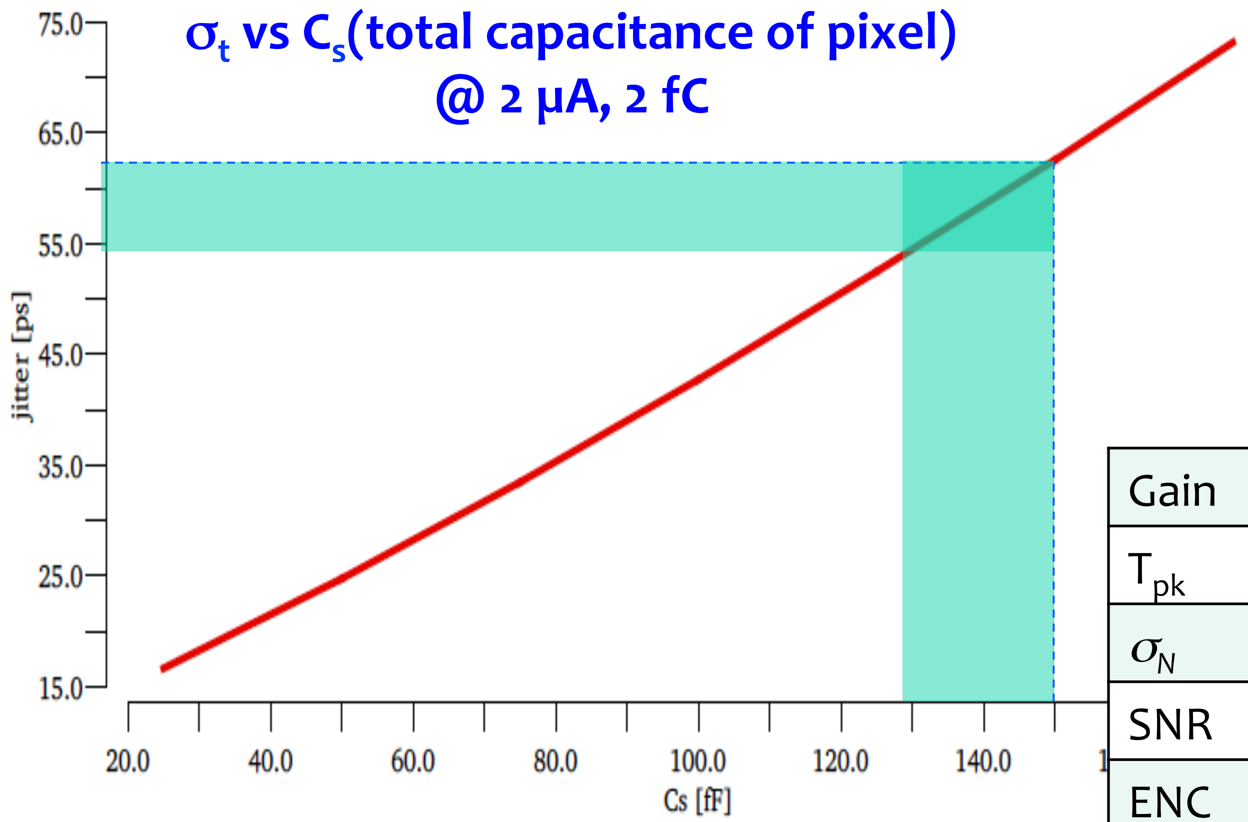






L. Piccolo – INFN Torino

Input stage, CSA (2)



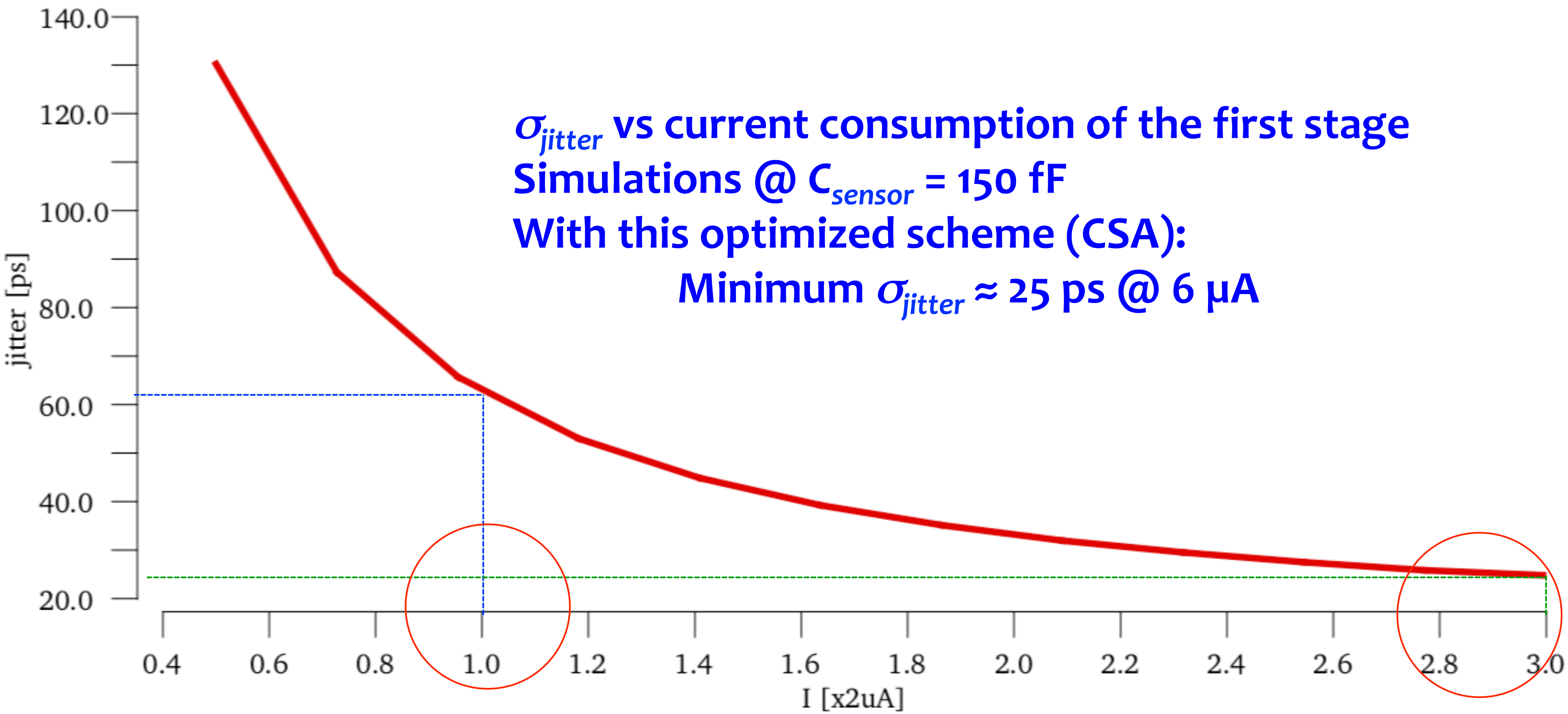
L. Piccolo – INFN Torino

table @ C_s = 150 fF

Gain	199.2	mV/fC
T_{pk}	11.86	ns
σ_N	2.63	mV
SNR	95	
ENC	82	e–
Jitter = σ_N/Vr	62*	ps
*Consumption	2	µA
Area (LE D. incl.)	37x14	µm²

Input stage, minimum σ_{jitter}

(circuit simulation output)

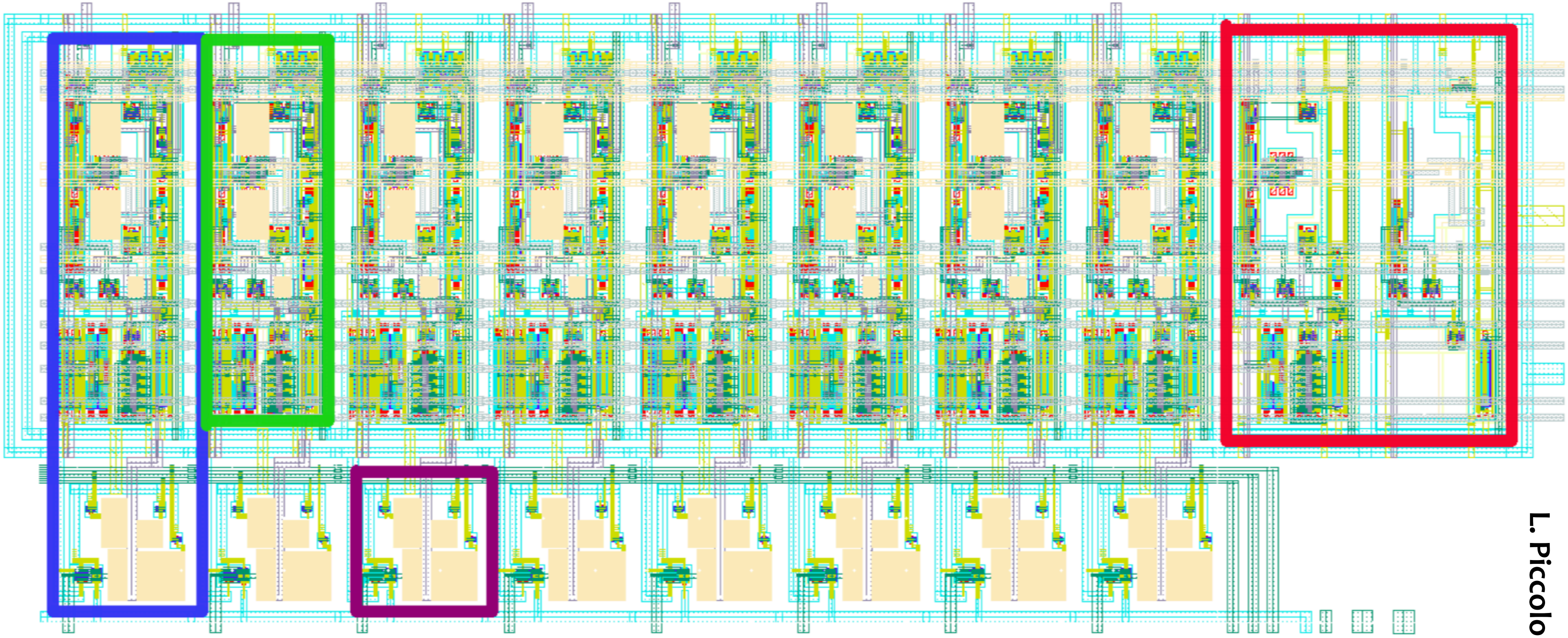


σ_{jitter} **vs current consumption of the first stage**
Simulations @ C_{sensor} = 150 fF
With this optimized scheme (CSA):
Minimum $\sigma_{jitter} \approx$ 25 ps @ 6 μA

L. Piccolo – INFN Torino

In view of the submission of the next version, we are already studying other readout schemes than the CSA (transimpedance or non linear input stages)

WP3: input stage layout



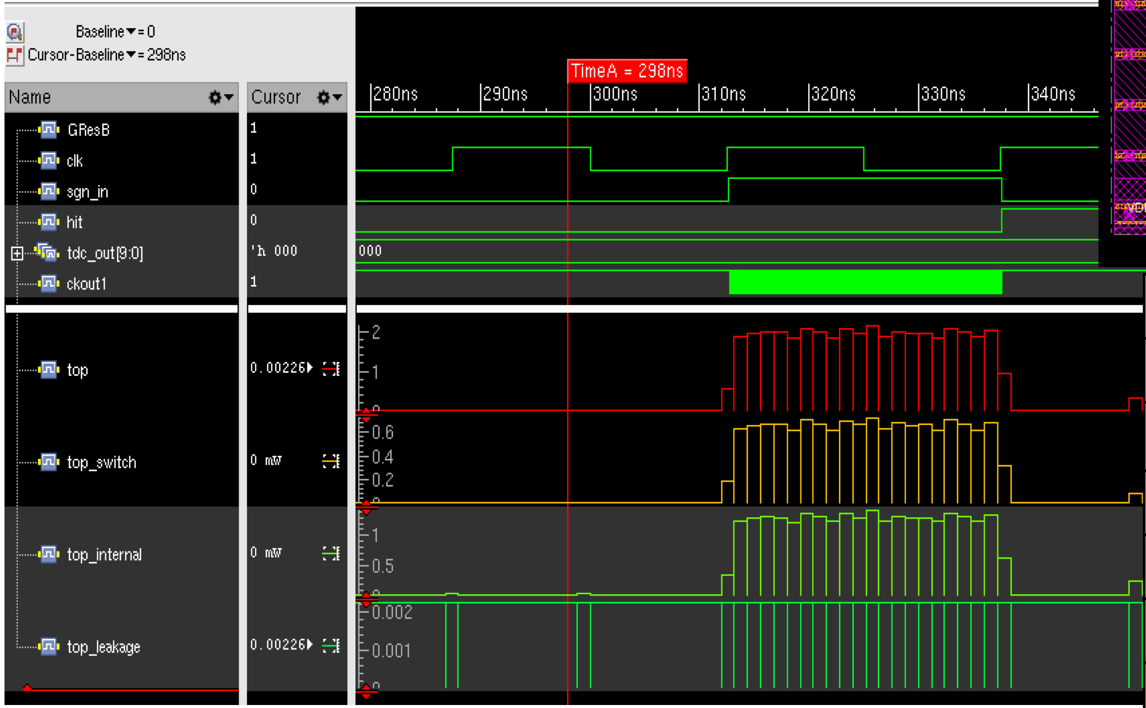
single channel core cell charge injection bias cell

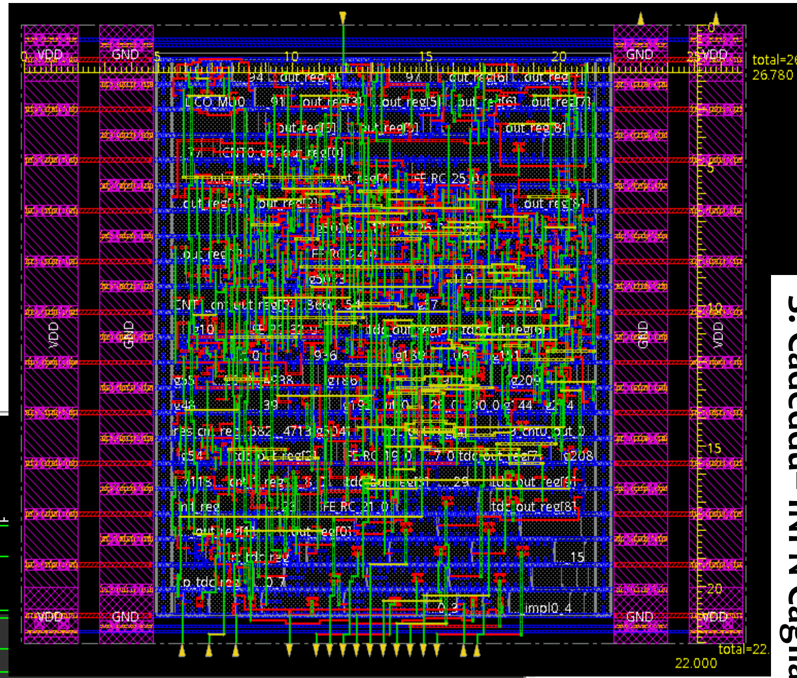
- 8 channels integrated
- Core channel consists in a CSA and a Leading Edge discriminator with offset compensation
- Whole cell sizes 60µm x 150µm (core cell area = 14 x 37 µm² without special care on area optimization)

L. Piccolo – INFN Torino

High-resolution TDC

- The (two) TDC designs are based on a "ALL digital fully-synthesizable design"*
- The DCO is standard-cell based
- DCO is enabled only on the occurrence of a hit for lower noise and consumption





S. Cadeddu– INFN Cagliari

Master Clk	40	MHz
Resolution (LSB)	50	ps
Resolution(rms)	15	ps
NOB	10	bits
Area	**20x15**	μm²
Power (conversion)	**1.9**	mW
Power (stand-by)	11	μW

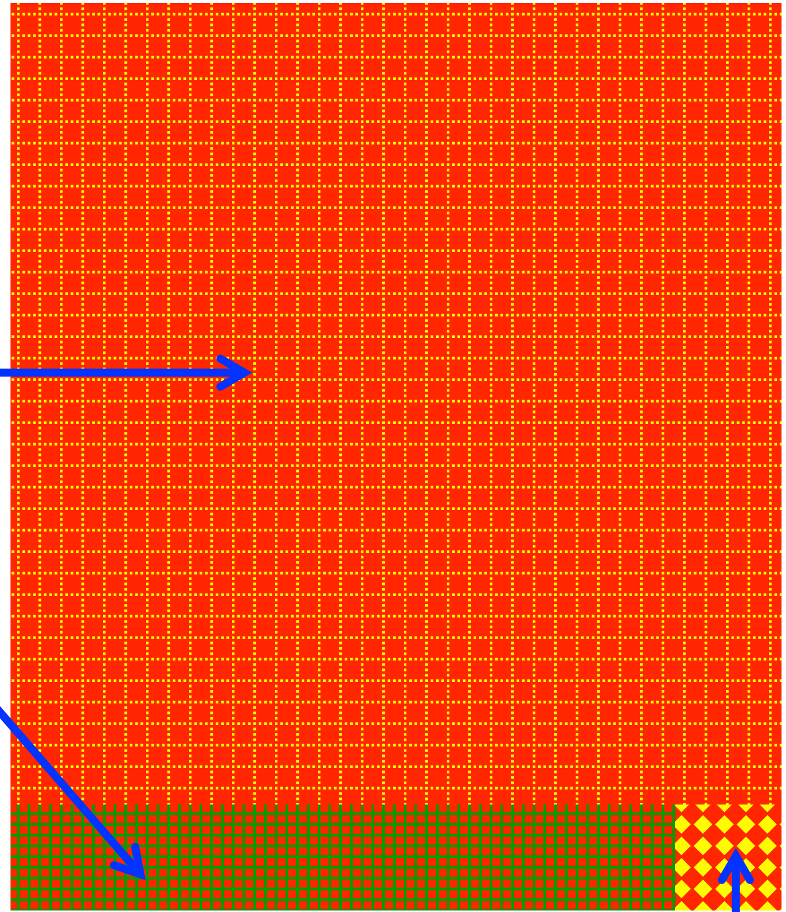
*S. Cadeddu et al., *High Resolution Synthesizable Digitally Controlled Delay Lines*, IEEE TNS vol 62 No. 6, Dec 2015

Concept for a 2nd prototype

Total Maximum area
1.5x1.5 or 3x1.5 mm²
(mini@sic)

Pixel area ≈ 24(48) x 24 x 55 μm²

Biasing and readout I/F



To be tiled on sensors

Possible submission(s):
November 2019
April 2020

Possible test structures

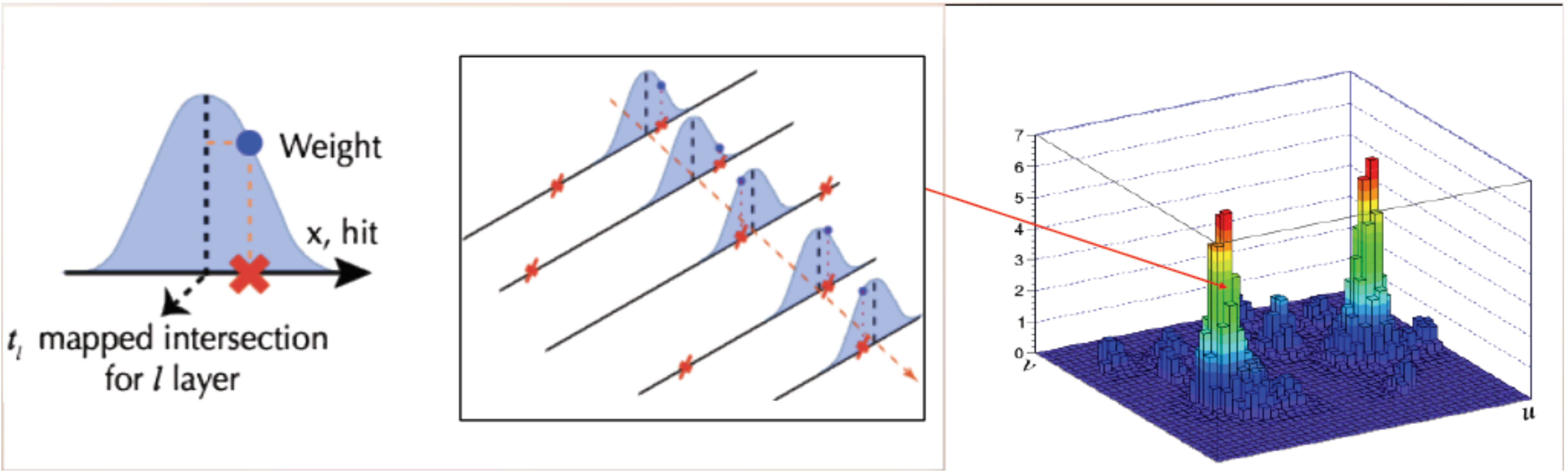
Outline

1. Why 4D ? Why timing?
2. Aim and Structure of the project: organization in Work Packages
3. Why 3D sensors ?
4. 2018 activity and first results
    a. Progress on sensor developments
    b. Progress on front-end electronics
    c. Progress on algorithms for real-time tracking
4. Perspective
5. Conclusion

Pattern Recognition Methods

Our strategy is to follow the RETINA project approach (1), adding time information into the algorithm structure (2)

RETINA project concept



RETINA concept: The detector geometry defines a set of possible tracks. A possible track corresponds to a cellular unit. Any point "seen" by the detector can be associated a weight, according to its distance from the track hypothesis. The algorithm finds tracks as maxima in weight in the track space.

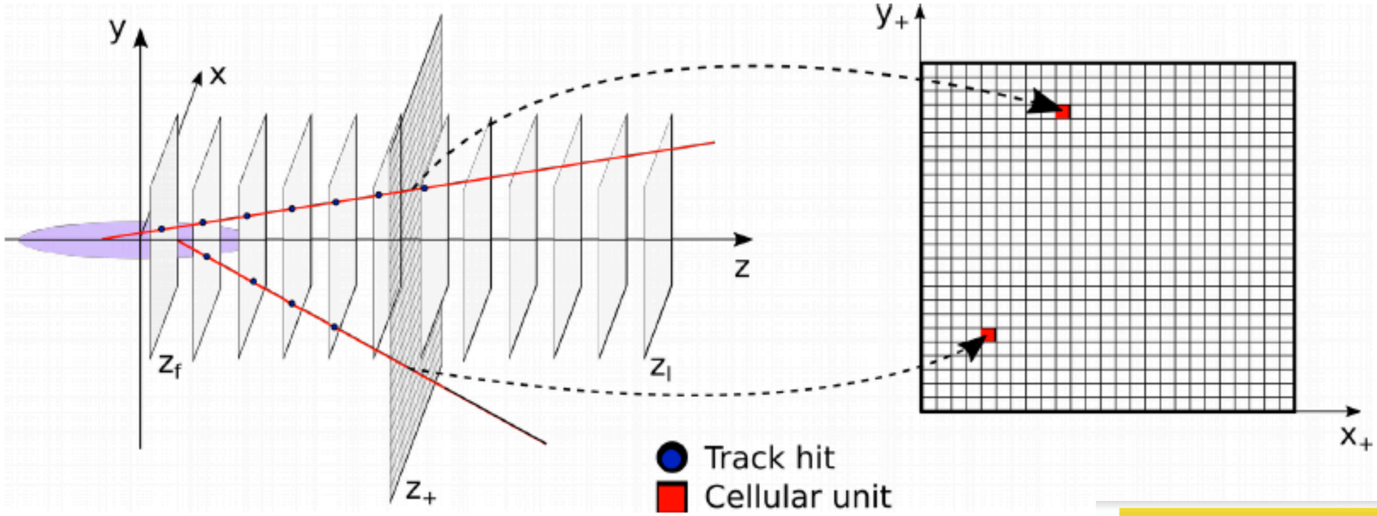
TIMESPOT concept: track points are substituted by stubs.

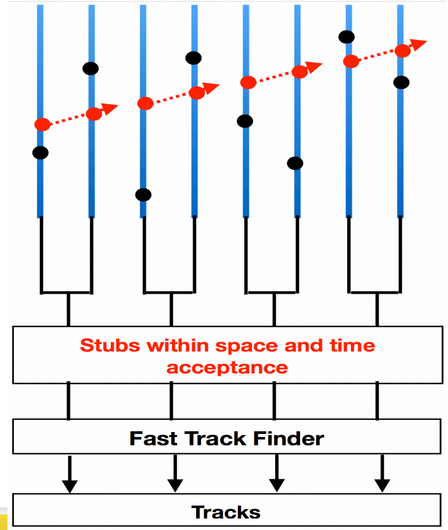
Each cellular unit can be processed in parallel. The algorithm can also be executed on commercial (powerful) FPGA.

(1) A. Abba et al., Simulation and performance of an artificial retina for 40 MHz real time track reconstr., JINST 10 (2015) no 03, C03008
(2) Neri N. et al., *4D fast tracking for experiments at high luminosity LHC*, JINST 11 (2016) no. 11, C11040

WP4: Real-time tracking. 40 MHz Stubs

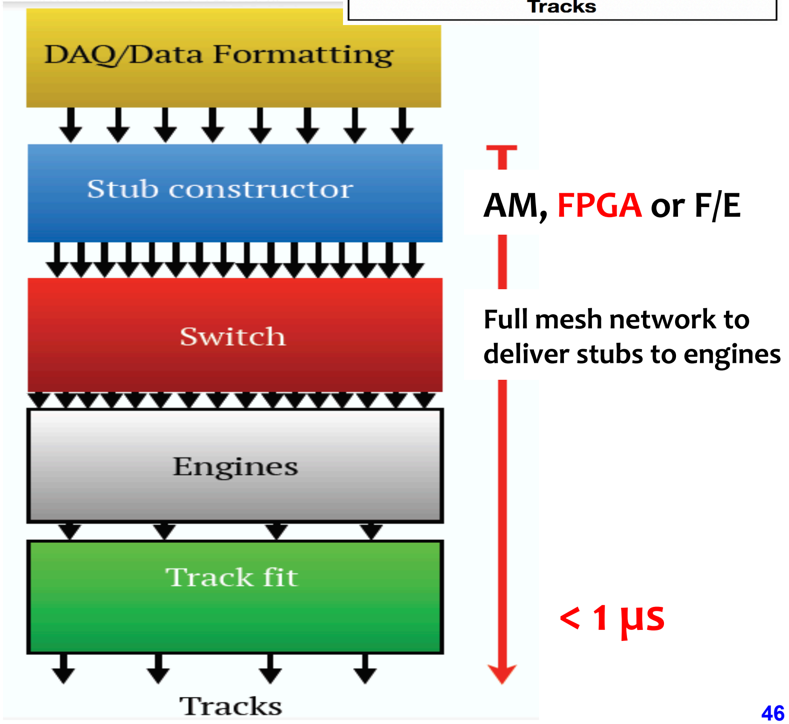
Milano





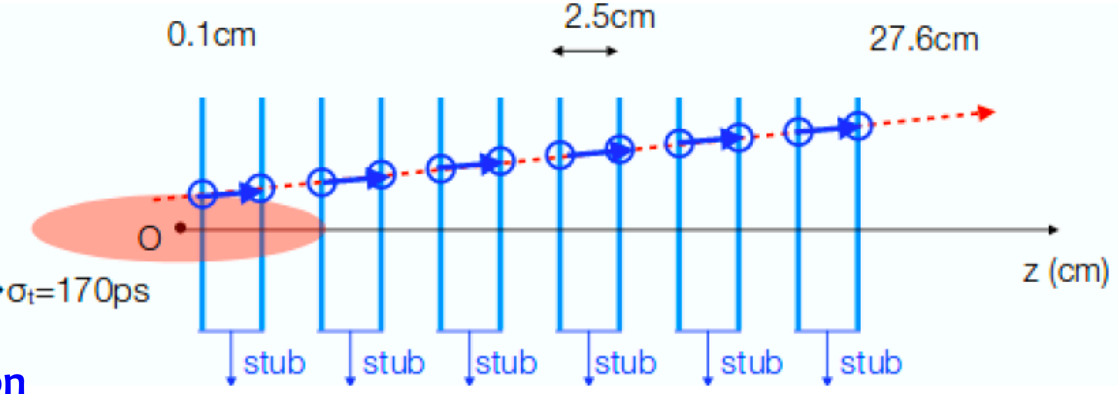
Algorithm steps:

1. Identify stubs i.e. couples of hit in adjacent planes compatible in space and time with tracks from the bunch interaction area;
2. Distribute the stubs in parallel to the Engines;
3. Engines identify tracks from clusters of stubs with similar parameters.



WP4: Test on a LHCb-like tracker

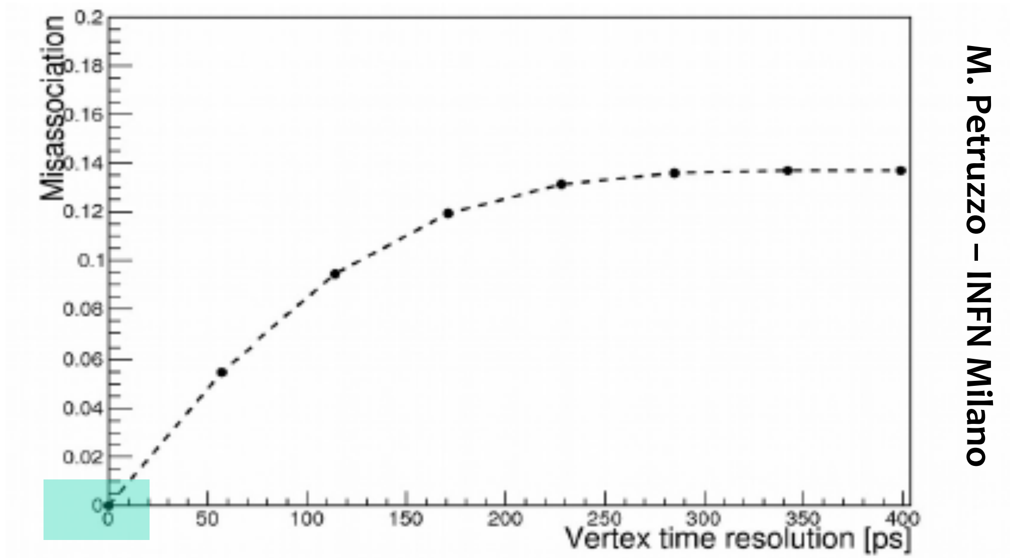
Sensor area = 6x6cm²
pixel size = 55x55μm²
thickness = 200 μm
time res σ_t=30 ps



Stub algorithm tested by simulation on a LHCb-like vertex detector:

- **12 planes of silicon vertex detector**
- **Pilup = 40**
- **1200 tracks/event**
- **Interaction region of gaussian shape (σ_z = 5 cm, σ_t = 167 ps)**

Mis-association vs vertex time resolution



M. Petruzzo – INFN Milano

The 4D fast tracking algorithm has also been in FPGA on a custom board (1):

Two Xilinx Virtex Ultrascale FPGAs
High-speed optical transceivers → up to 1 Tbps input data rate per FPGA
One Xilinx Zynq FPGA

(1) M. Petruzzo et al., A novel 4D finding system using precise space and time information of the hit , TWEPP 2018

WP5: Fast read-out

Bologna

ATLAS TDAQ

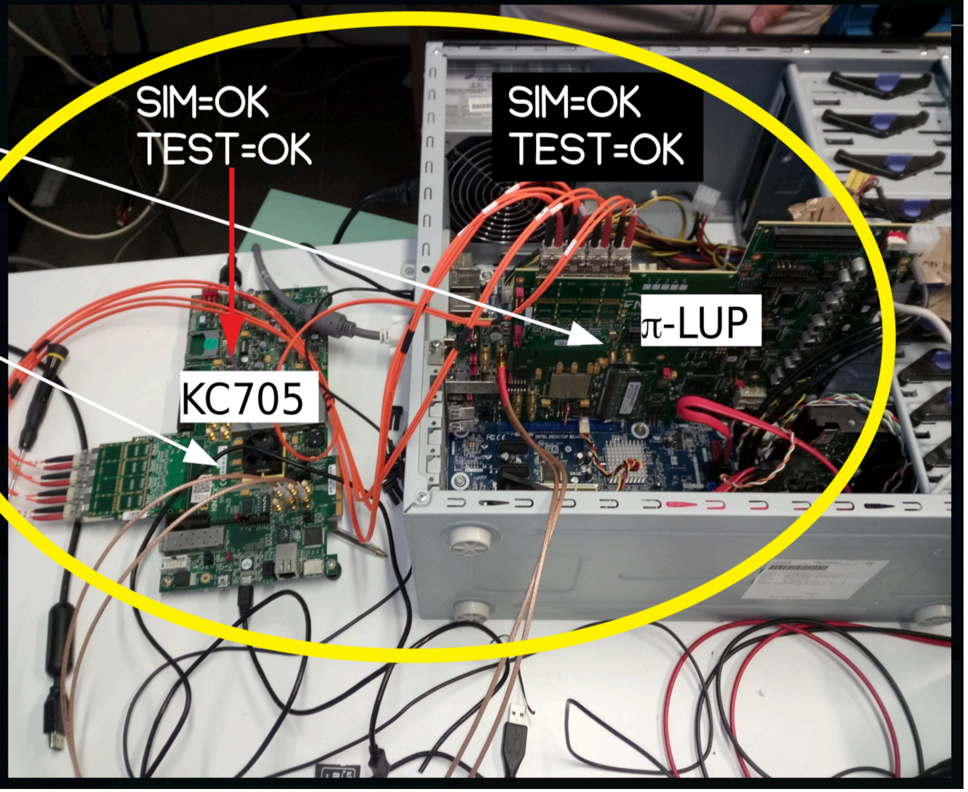
FPGA FW

- 4 x 1.28 Gb/s lanes
  5.12 Gb/s
  RD53A/FEI4 emulator
  - **≲ 6 x RD53A**
  - **≲ 175 x FEI4**

The emulator itself can generate data 10 times faster, if not limited by the PCIe bandwidth

- Driver SW

- **3.2 GB/s** PCIe
  1.6 GB blocks
  transferred at a time



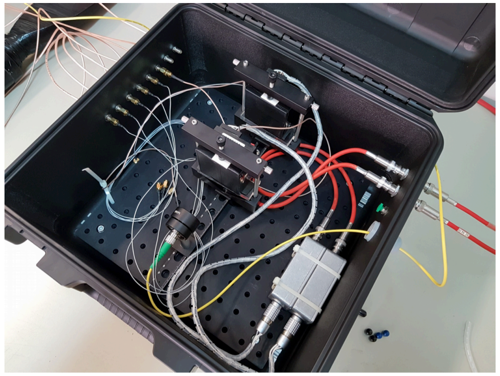
F. Alfonsi, G. D'Amen, A. Gabrielli – INFN Bologna

Three level of testing during the development of the demonstrator:

1. Develop minimal read-out chains (from TDAQ architecture) for Low-performance testing procedures (simple, low cost FPGA systems) → in preparation
2. Use the ATLAS TDAQ emulator for RD53 to generate events with a realistic data format to test real-time algorithms → on going with Milano
3. Use the ATLAS TDAQ as a test-bench for the TIMESPOT prototypes → this year

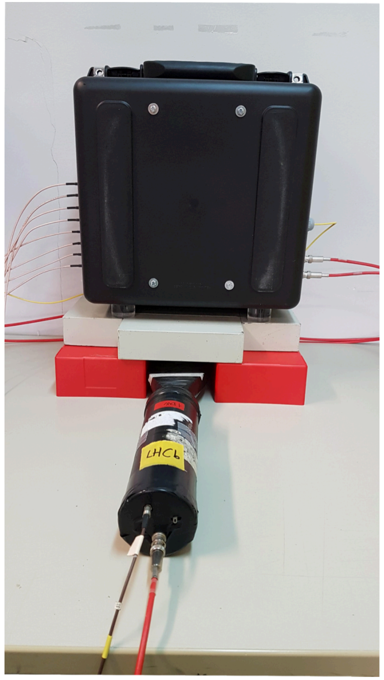
WP6: Test preparation in labs and test-beams

Cagliari, Genova, Padova (LNL), Trento…



Preparation of wafer tests in the labs (short term – Spring-Summer 2019):

1. Trento: first tests (automatic and manual tests) on 3D wafers
2. Cagliari: manual tests under probe station with IR laser and confocal microscope (devices already purchased, under preparation)
3. Torino & Padova: sharing of manual test under PS (setup ready)
4. Cagliari & Genova: preparation of active probe for pixel time response under laser scan
5. Padova (LNL): use of μBeam facility for detailed pixel scan with 1.8 MeV protons (see next slide)



A. Cardini, M. Garau – INFN Cagliari

Preparation of device tests with MIPs under test beam (medium term – Fall-Winter 2019):

1. Preparation of a time-tagger using MCP (almost completed in Cagliari, ~ 15 ps time resolution measured with cosmics).
2. Test-beam test of simple structure (wire bonding)
3. Bonding to TIMEPIX (ADVACAM?) or VELOPIX (LHCb) after temp metal removal → most sensor characteristics testable but timing
4. Test beam with telescope (PSI – already booked October 2018)
5. Fermilab? DESY? (CERN is on shutdown!)

Perspective

During 2019:

- Set-up of test-benches and tests on first prototypes (sensors and electronics)
- Test beams for complete characterization of devices

End 2019 – beginning 2020

Submission of second prototypes

During 2020:

Set-up and tests of demo system

TIMESPOT is financed till the end of 2020.
Clearly, three years will not be sufficient for a final answer.
If TIMESPOT is "successful enough", a kind of TIMESPOT-II must be invented – hopefully at an international level

Summary

- The TIMESPOT project aims at realizing a complete demo-vertex-detector with time-resolved events and real-time reconstruction
- Results on developments concerning the activities of its first year (2018) have been illustrated
- Year 2019 will be a decisive year for TIMESPOT: results on its first prototype batches of sensor and electronics will be obtained and evaluated.
- In the meantime, we are already starting to envisage a possible extended prosecution of our project

THANK YOU