

TILECAL at SLHC

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ATLAS SLHC Steering group

ATLAS High Luminosity Steering group launched mid-2004

Present the case and the issues for an upgrade of ATLAS to be able to exploit the physics potential at $10^{35} \text{ cm}^{-2} \text{ s}^{-1}$

SLHC / machine upgrade

Three possible phases envisaged (from ST)

<http://atlas.web.cern.ch/Atlas/GROUPS/UPGRADES/>

- **Phase 0:** stretch machine to its limits
Increase luminosity by factor 2.3 beyond design value
Comes for free (might need to upgrade injectors however)
- **Phase 1:** upgrade of the interaction regions
Increase luminosity by one order of magnitude
- **Phase 2:** upgrade of the arcs as well
Increase luminosity (as before) and \sqrt{s} by a factor of 2
Includes upgrading the SPS with superconducting magnets
to be able to inject at 1 TeV
New dipoles with 15 T field (2 T safety margin)

TileCal issues / main limitations

✓ Main identified Tilecal limitations to operate at SLHC

- increase of radiation levels
- increase of pile-up
- possible LHC operation with bunch spacing less than 25ns

✓ Start investigations on

- radiation & ageing effects on the sensor (detector)
- radiation effects on the electronics
- pile-up effects on jet energy resolution

ATL-TILECAL-2005-002

Workshop Summary for TILES

✓ ATLAS SLHC Workshop Feb 2005:

SHLC document CERN-ATL-COM-GEN-2005-002

Conclusions & strategy for TILES :

1-No need for upgrading the detector :

- The anticipated light losses induced by radiations dose and ageing at SLHC will not affect the measurement of the jet energy, and a will have a marginal effect on the jet energy resolution
- Nevertheless we know that the gap and crack scintillators have to be replaced after few years of LHC operation.

2- Hopefully same electronics could be kept :

this will depends on the radiation levels observed at LHC start and extrapolation to SLHC.
The strategy is to wait until first measurements of radiation levels are done at LHC start.

3-A/ then perform additional radiation tests on the TILECAL electronics up to safety required levels

3-B/ if electronics components fails and/or if tilecal electronics is not able to cope with not yet known bunch crossing frequency, a partial upgrade or a complete redesign has to be investigated.

Workshop Summary for TILES

✓ 1- Ageing studies

Del Prete et al, A Maio et al

✓ 2 & 3- A further radiation tests

possibly needed on the TILECAL electronics up to safety required levels

From ATL-TILECAL-2005-002 :

TID: MB, HV micro, HVopto, mezzanine, 3in1, (interface)

NIEL: LVPS, ELMB, interface,

Activities

Impact of Bunch crossing freq. on Electronics

inputs from K Anderson and C. Bohm

- ✓ Tilecal should in principle be able to cope with every scenario with bunch spacing of 25 and 75 ns, using present electronics. Super bunch scenario is difficult to handle (obsolete scenario now)
- ✓ Bunch spacing 12,5ns, electronic frequency at 25ns
Events on the peak & events at $\pm 12,5\text{ns}$ => new treatment of the signal at the ROD level
=>FEASIBLE . Need studies for the signal treatment in ROD
- ✓ Bunch spacing 15ns, electronic frequency at 30ns
Events on the peak & events at $\pm 15\text{ns}$ => new treatment of the signal at the ROD level
30ns frequency ok for all cards, Potential pb with the interface (Glink clock fixed to 25ns, Deskew2 should cover the full clock period)
=>Tests with TTC-vi and TTC-vx at 30ns needed to conclude. At worse Interface card to be redone . Cost ? If Interface redone, do we want to redo all FE at the same time... ?
- ✓ Bunch spacing 10ns ?
More difficult to handle. not studied.

Since SLHC scenarios were evolving , we didnt push more for studies, waiting to a reduced number of favoured BC possibilities. Inner Dectector obviously had a different view.

Activities

Since Mid November

- ✓ Submission of R&D proposals for ATLAS upgrades is opened.
- ✓ ATLAS got a request from the CERN interdepartemental working group (POFPA) to provide a preliminary costing figure for the detector upgrade, taking into account the differences for bunch spacing values of 10 resp. 15 and 12.5 (for early dec2005)

Activities

✓ actions (for next Tile week?)

1. More studies on the impact of the bunch crossing freq on the TILES electronics

- **10,12,5 & 15 ns cases** : BC identification :How to treat signal without sample on the peak?
- **15 ns case** : tests on interface? Unlikely
cost estimate for a new interface
- **10 ns case**: up (down) to which frequency the FE electronics is able to run?
(NO QPLL, but GLINK fixed,...)
Buffer windows large enough?
proposal for a new FE design. Everything to be redone or only parts ?

2. Provide a cost estimate in function of scenario & component(s) to be replaced.

- 15 ns case 0 < cost < new interface cost ?
- 12,5 ns case 0MCHF?
- 10 ns case cost for Total redesign ?

Activities

Others questions

3. TILES R&D for SLHC ?
4. Should we envisaged Radiation tests before LHC starts for components with lower safety margin (as part of R&D?)
5. If SLHC, ATLAS will be longer into operation.
Even if electronics is OK, technology obsolescence and amount of spare components is an other point to take into account

Activities

✓ First crude costing estimate for a TILECAL upgrade

On the following basis :

- 1- No need for upgrading the calorimeter except the gap and crack scintillators
- 2- a total replacement of the electronics is needed
- 3- PMTs are not replaced
- 4- and starting from the 95 cost of the present electronics,

MOU 95/MCHF :		7MCHF
Pmts 310chf*10000		- 3MCHF

		4MCHF
inflation +overcost (x2?)	4x2=8	8MCHF
LVPS		1MCHF
Scintillators		?MCHF

=> crude estimate for a full electronic upgrade ~ 10MCHF