MIF
Upgrades HL-LHC & Calice

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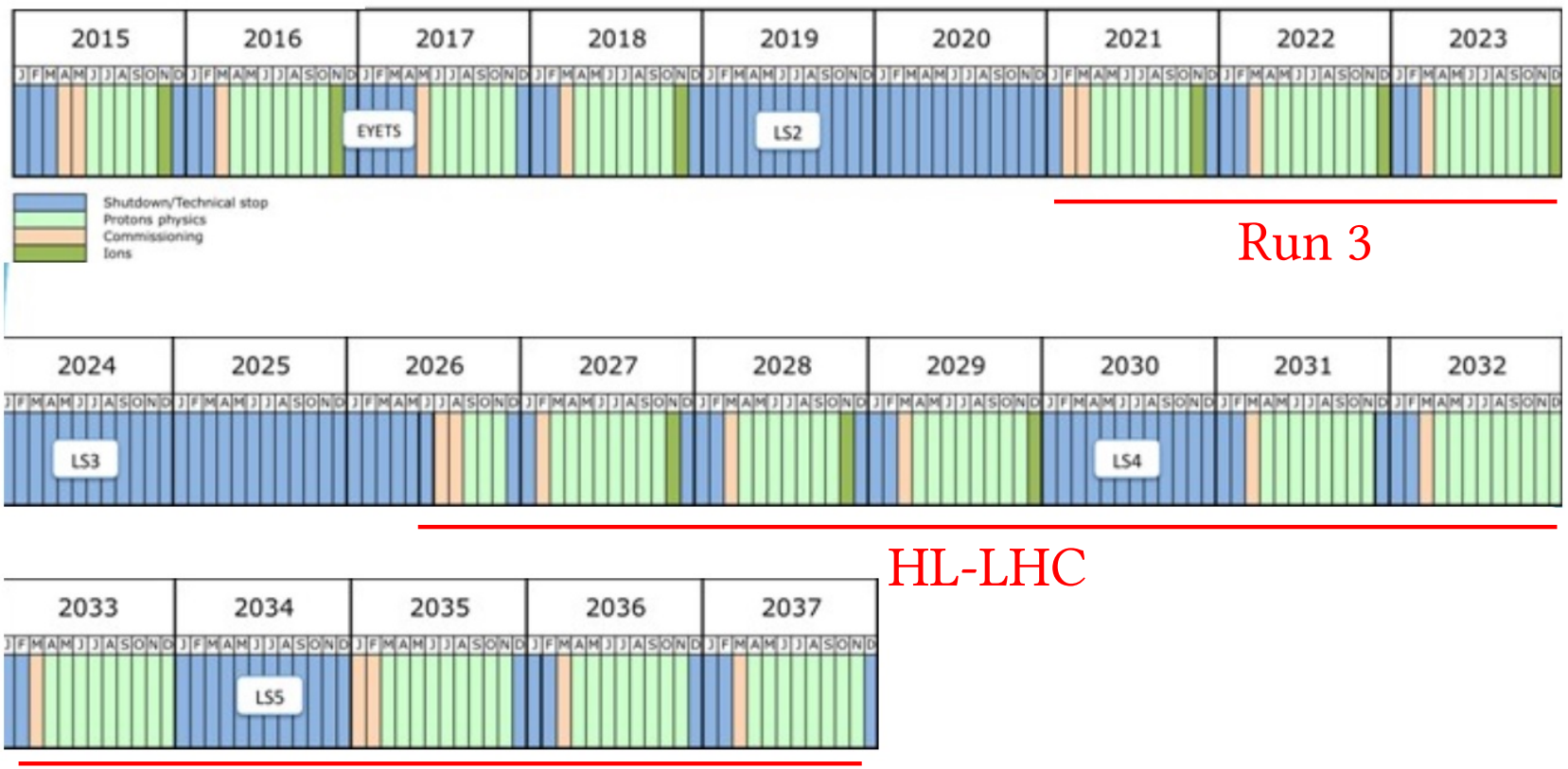
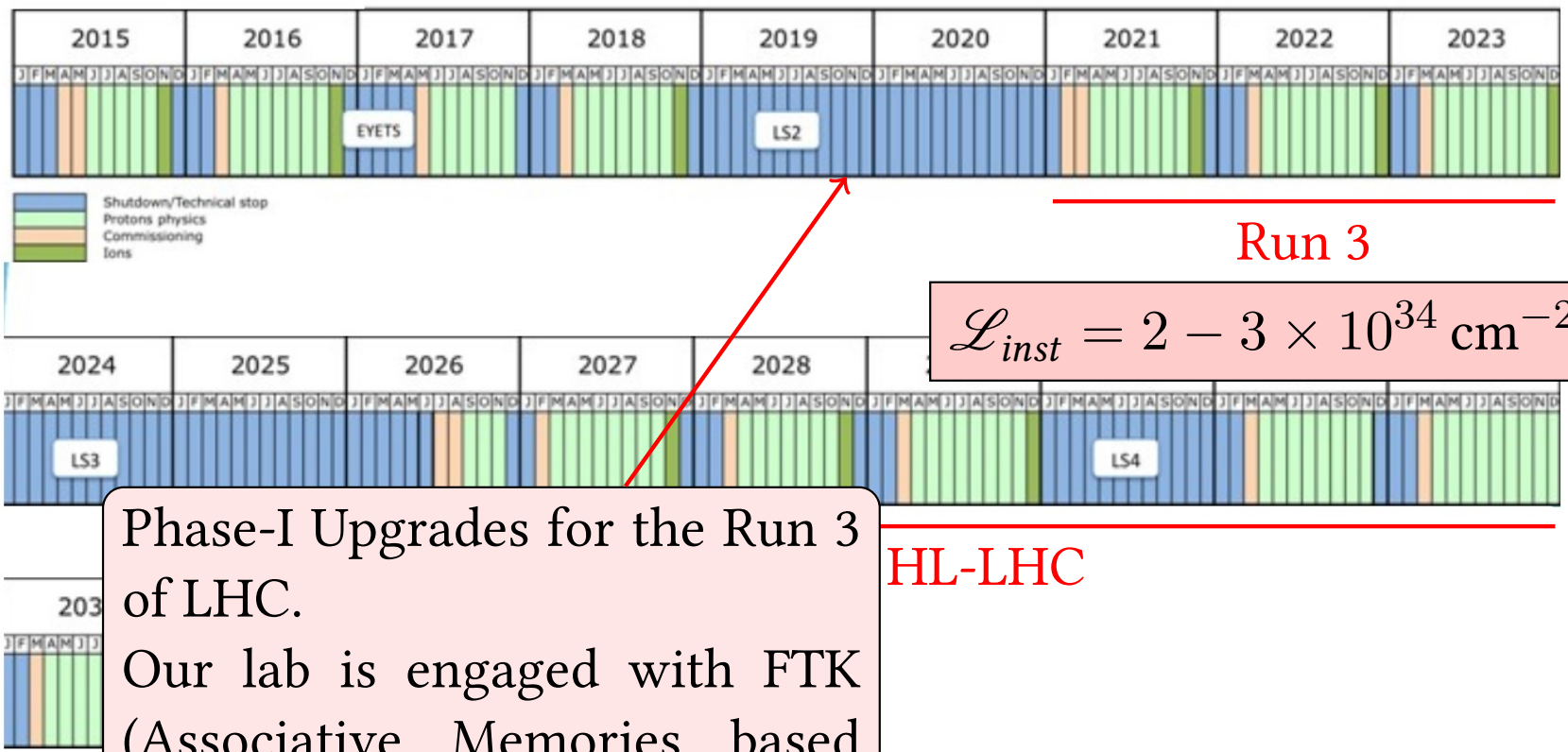
Introduction

Medium to long term strategy for the MIF groups is dominated by the HL-LHC schedule.
A major upgrade program is under way and it is expected to be realized by 2026. Then the HL-LHC will run for 10 years.
Nevertheless the R&D for future colliders (ILC, CLIC, ...) is already ongoing or it is going to rump up soon. It is also the right time to look ahead.

LHC Timeline



LHC Timeline

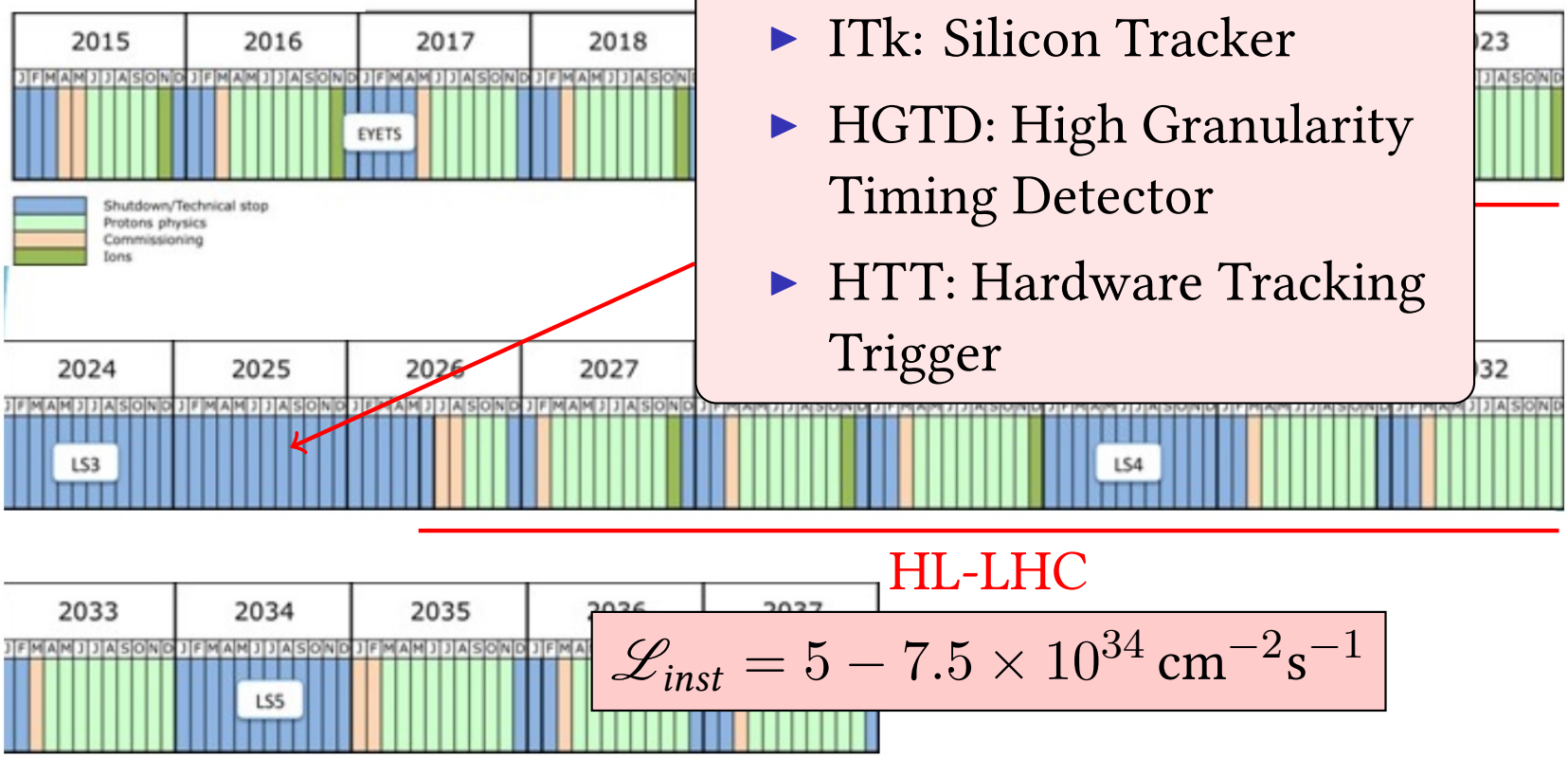


Phase-I Upgrades for the Run 3 of LHC.
Our lab is engaged with FTK (Associative Memories based tracking trigger processor).

LHC Timeline

Phase-II Upgrades for the HL-LHC.
Our lab is engaged with

- ITk: Silicon Tracker
- HGTD: High Granularity Timing Detector
- HTT: Hardware Tracking Trigger



HL-LHC

$$\mathscr{L}_{inst} = 5 - 7.5 \times 10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$$

ITk

The current ATLAS Inner Tracker can't cope with HL-LHC conditions. ATLAS has a major upgrade program to replace the whole tracker.

- New **Pixel** and Strip detectors
  - Higher granularity (for pixels 50x50 or 25x100 μm^2)
  - Radiation hardness (up to 3×10^{15} n_{eq}/cm^2)
  - Hit efficiency at least 97% at 600 V bias voltage
  - LPNHE has a significant activity in sensor design and R&D
- New Front-End electronics
  - RD53 FE chip. LPNHE is contributing also to this project.
  - ATLAS FE chip prototype expected to be submitted in Sep 2019
- New mechanics, services, optimized for low material budget

ITk @ LPNHE

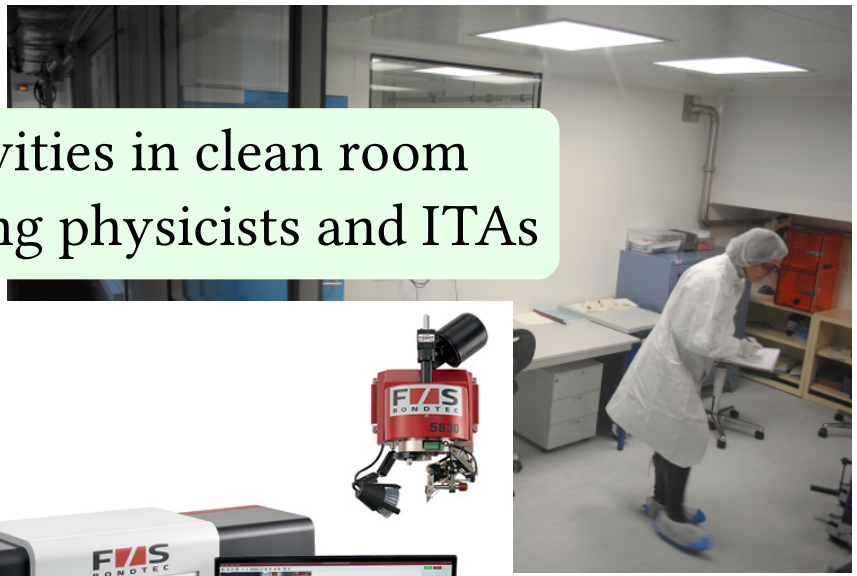
The activities for ITk at LPNHE are currently planned up to 2024.
Main area of responsability:

- Outer barrel modules assembly site (in collaboration with LAL and Saclay: the Paris Cluster)

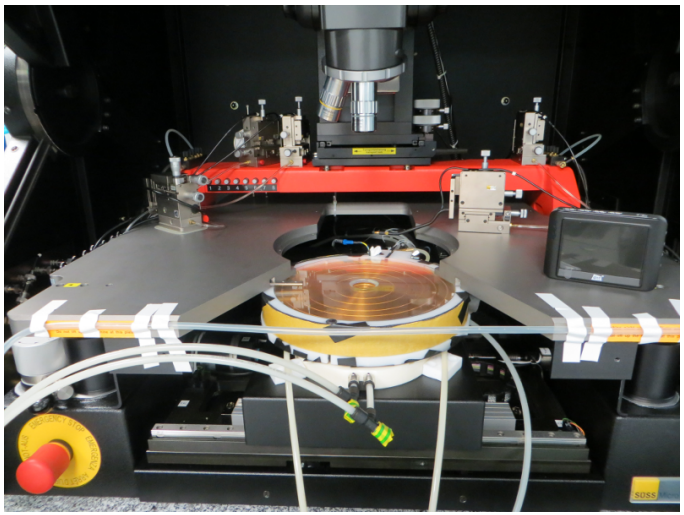
Other areas:

- Test beam
  - Coordination
  - Partecipation & operations
  - DAQ
- Front-End electronics R&D
  - Memeber of the core design team of RD53 (A/B)

ITk Outer Barrel Assembly Site



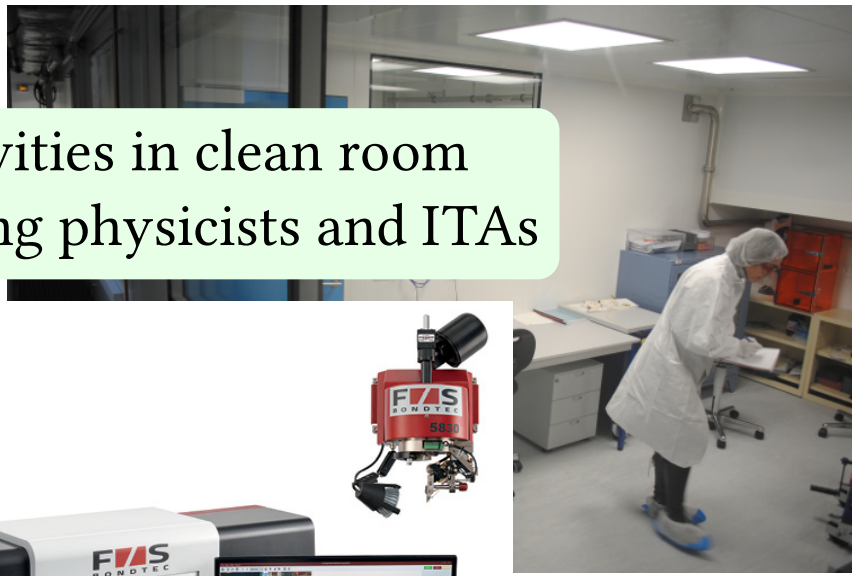
Activities in clean room involving physicists and ITAs

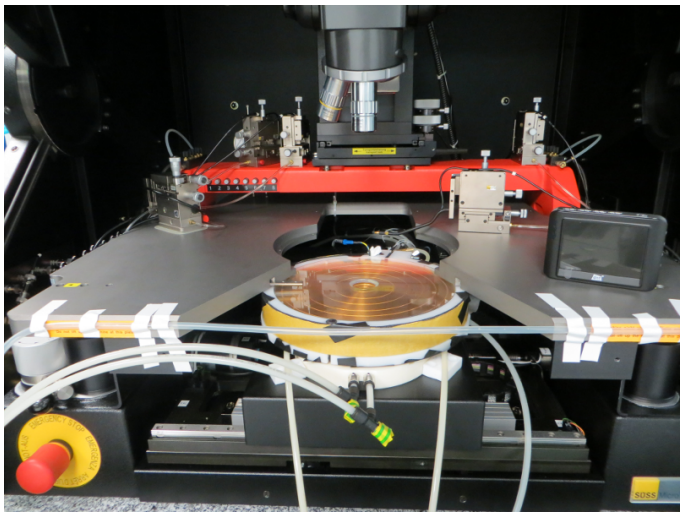


Sensor measurements (electrical, mechanical) to qualify and select good sensors to be mounted on modules. Then modules wire bonding and electrical tests before shipping for assembly.

ITk Outer Barrel Assembly Site

Activities in clean room involving physicists and ITAs

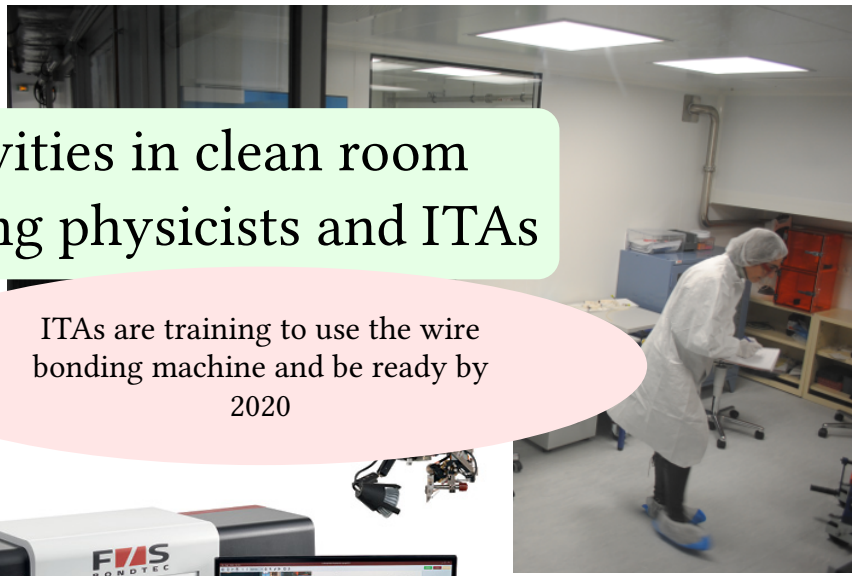




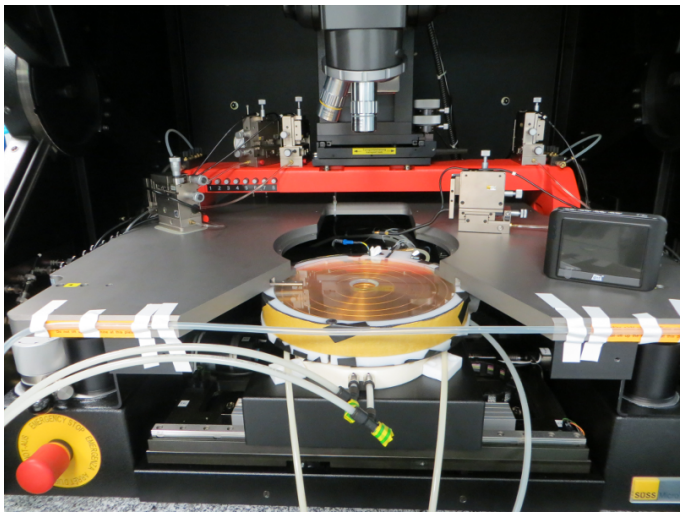
Our clean room qualified for the Market Survey phase.
We already received some wafers to measure.
We will complete the equipment with a microscope/profilometer.

ITk Outer Barrel Assembly Site

Activities in clean room involving physicists and ITAs

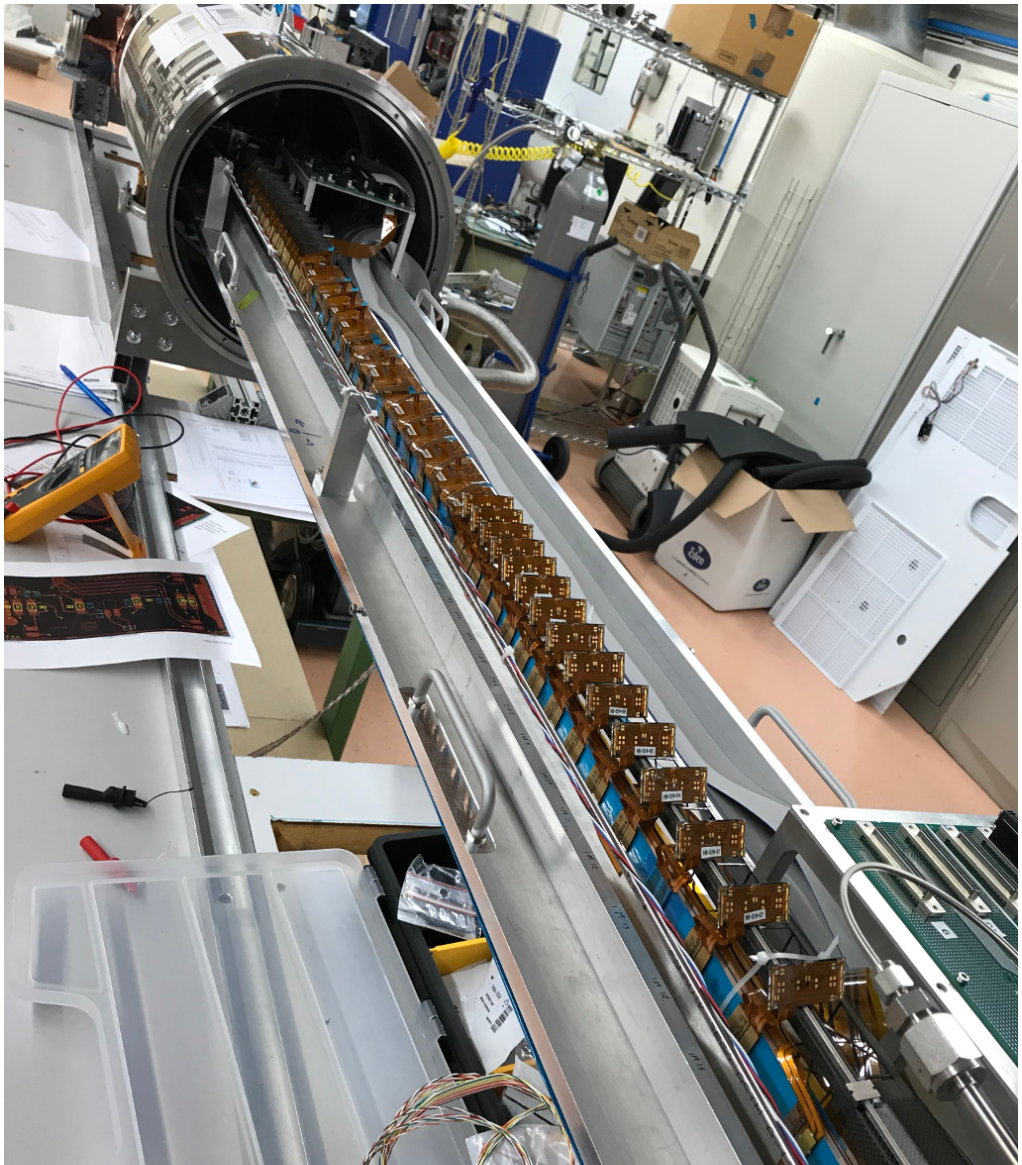


ITAs are training to use the wire bonding machine and be ready by 2020



Scale from the current R&D activities to fully "industrialized" mode of qualification/production.
Organization and QA is another challenge!

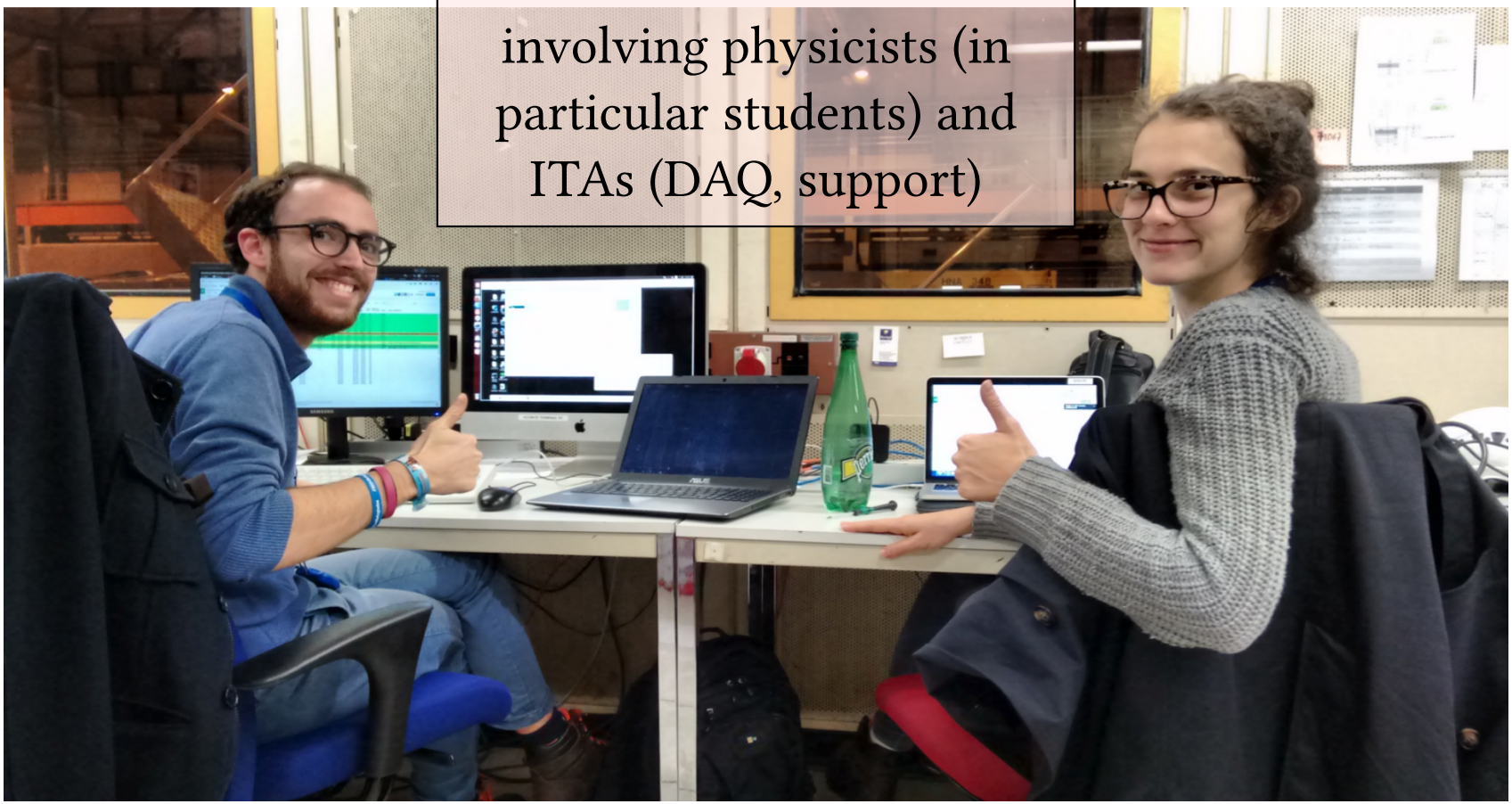
ITk Demonstrator



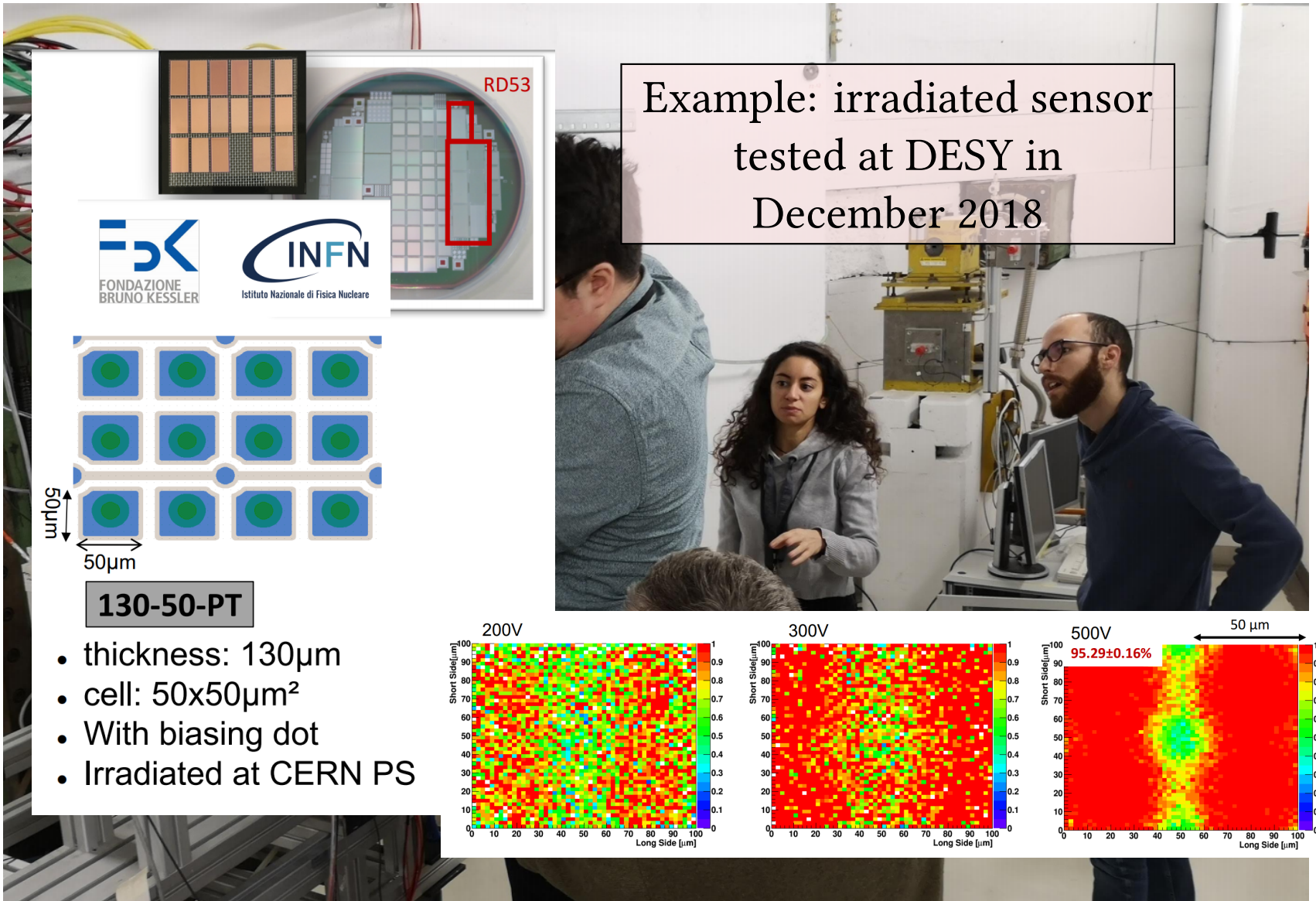
Demonstrator of an ITk stave to study mechanics and thermal properties.
A significant contribution from LPNHE: many thermal modules tested in our Climate Chamber.
Also some electrical modules tested.
A complete slice demonstrator (from stave to services to cables) is planned

ITk Test Beams

Test beams activities involving physicists (in particular students) and ITAs (DAQ, support)



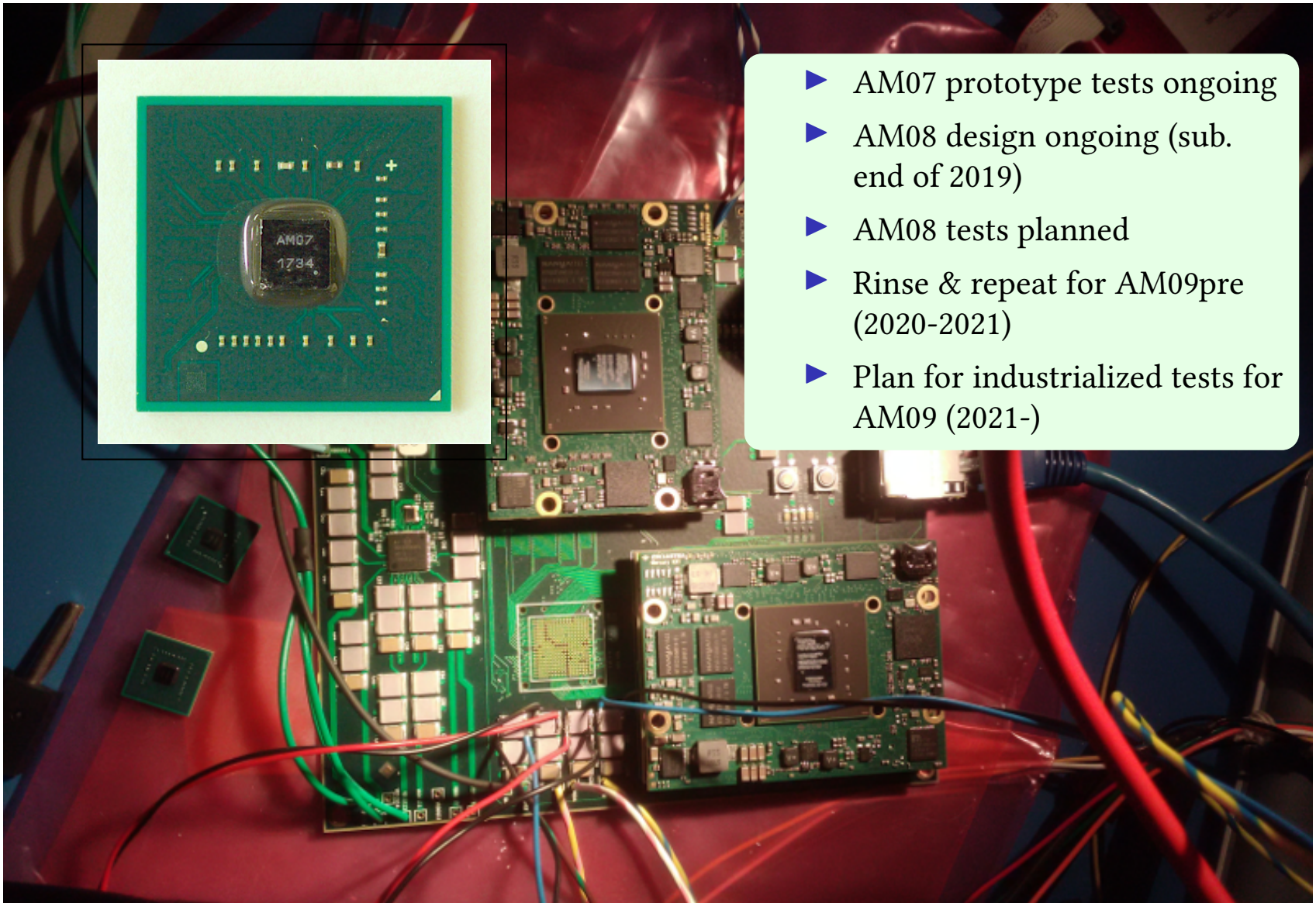
ITk Test Beams



HTT

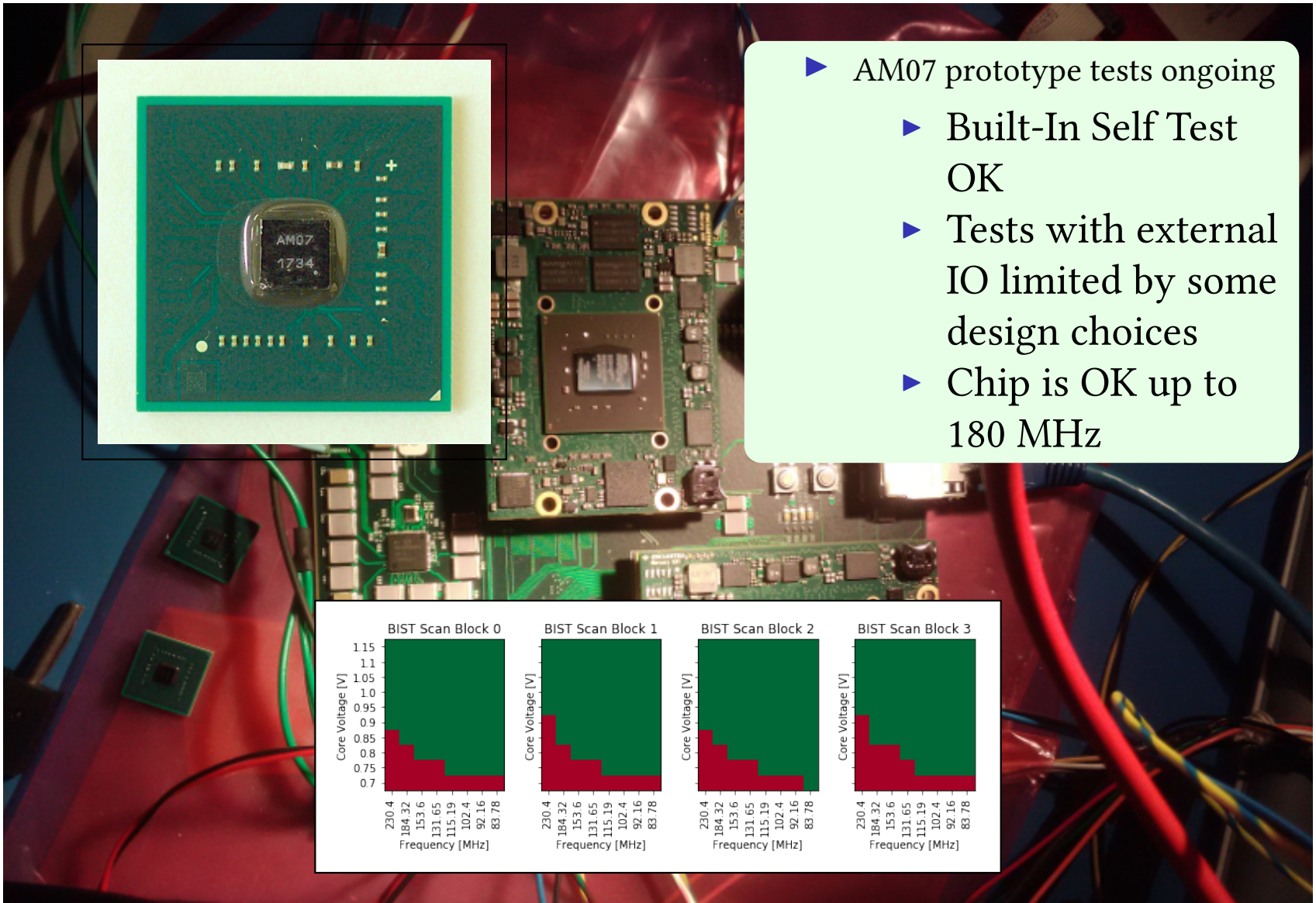
- The Hardware Tracking Trigger (HTT) will be the co-processor for the high level trigger of the ATLAS TDAQ Phase-II.
- It will provide on demand the trajectories of the charged particles in ITk.
- It will be able to run up to 4 MHz trigger rate (as the readout of ITk)
- At LPNHE we are committed mostly on the Associative Memory chip development
  - Intense activities planned up to 2021-2022
  - Support until completion of the HTT Upgrade in 2024

HTT @ LPNHE: Associative Memory



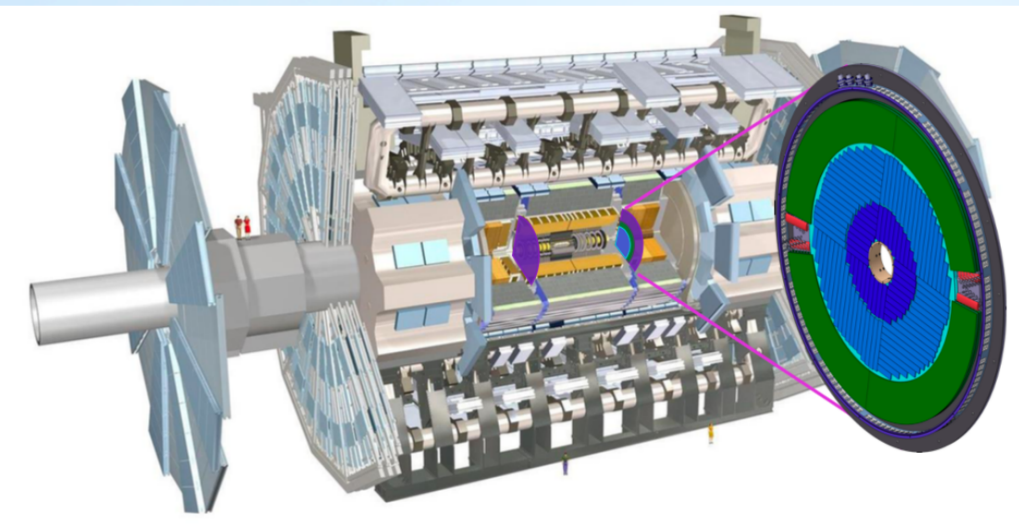
- AM07 prototype tests ongoing
- AM08 design ongoing (sub. end of 2019)
- AM08 tests planned
- Rinse & repeat for AM09pre (2020-2021)
- Plan for industrialized tests for AM09 (2021-)

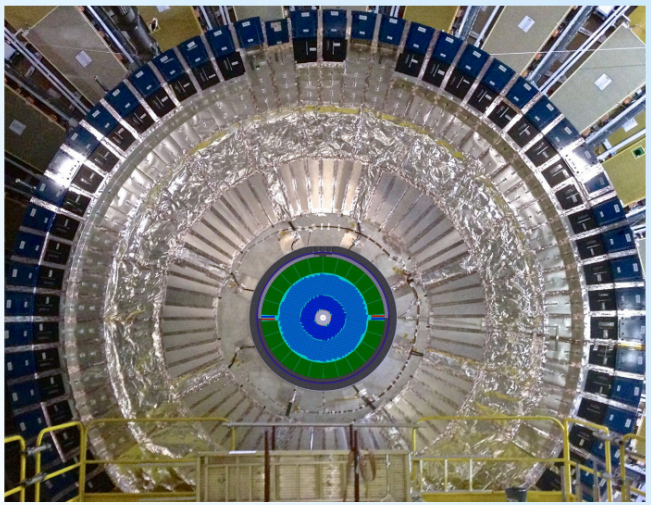
HTT @ LPNHE: Associative Memory



- AM07 prototype tests ongoing
  - Built-In Self Test OK
  - Tests with external IO limited by some design choices
  - Chip is OK up to 180 MHz

HGTD in ATLAS





Pseudo-rapidity coverage	$2.4 < \|\eta\| < 4.0$
Thickness in z	75 mm (+50 mm moderator)
Position of active layers in z	$z = 3443, 3454, 3468, 3479$ mm
Radial extension:	
Total	$110\text{ mm} < R < 1000\text{ mm}$
Active area	$120\text{ mm} < R < 640\text{ mm}$
Pad size	$1.3 \times 1.3\text{ mm}^2$
Sensor thickness	$50\ \mu$m
Number of channels	3.59M
Active area	6.4 m^2
Average number of hits per track:	
$2.4 < \|\eta\| < 3.1$	≈ 2
$3.1 < \|\eta\| < 4.0$	≈ 3
Time resolution per track	30 – 50 ps ps

Provides time and luminosity measurements

2 identical detectors,
one on side A, one on side C,
fixed on LAr cryostat

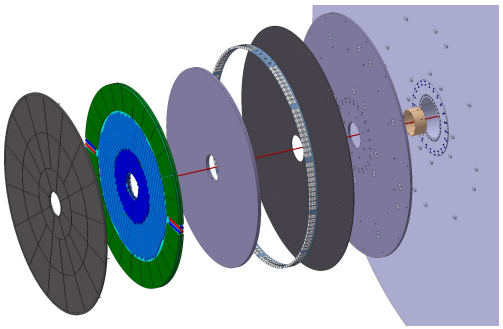
Operating temperature -35 °C
CO_2 cooling is used
N_2 gas flushing

HGTD @ LPNHE

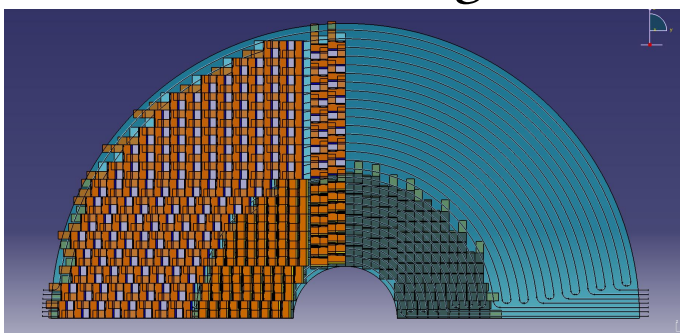
The activities for HGTD are planned up to 2026

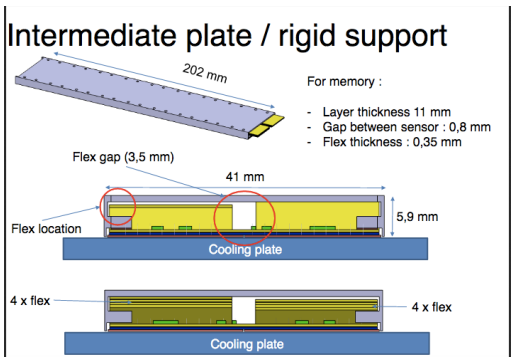
- Our laboratory is committed for the module assembly and the development of mechanical solutions for assembly
  - This activity will ramp up in the next years and last until 2026
- Test beam activities are currently ongoing and more test beam campaings are foreseen up to 2021
  - A key element for the success of HGTD will be the test of irradiated sensors / modules

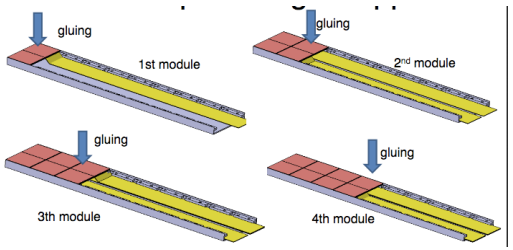
HGTD @ LPNHE



HGTD Design



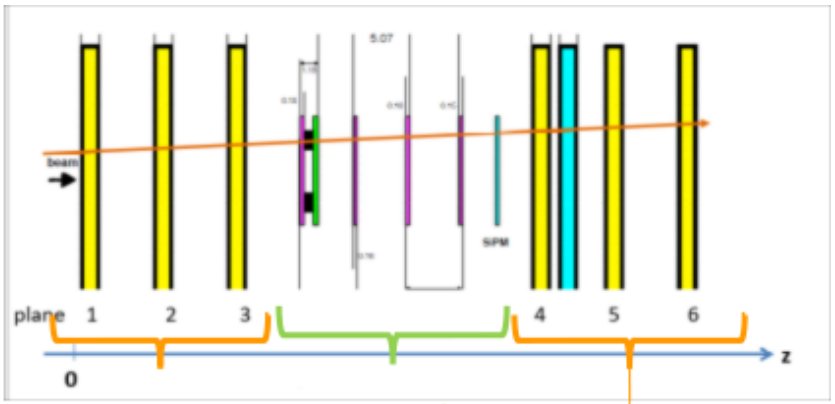




Disk concept

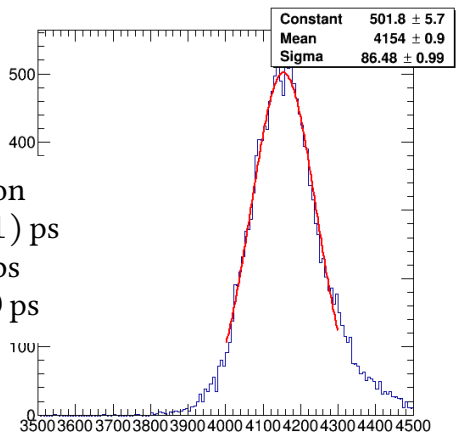
- Design highly optimized for performance
- 2 double sided disks per end-cap
- Electronics radially distributed at the periphery
- Read-out rows and assembly plates
- Longest readout row: 19+18 modules
- Modules assembled on staves (R>320mm)
- Modules assembled on half-disks (R<320 mm)

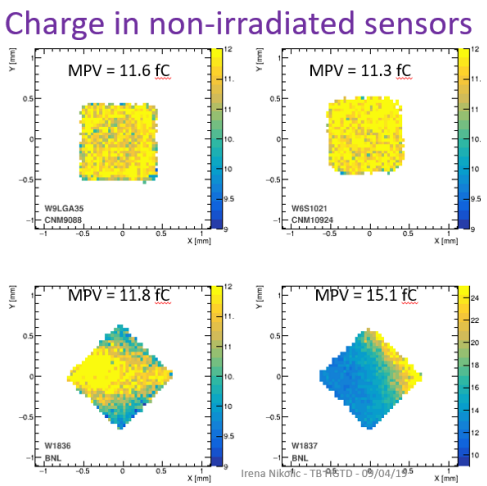
HGTD Testbeams (slide from Irena Nikolic & Sophie Trincaz-Duvoid)

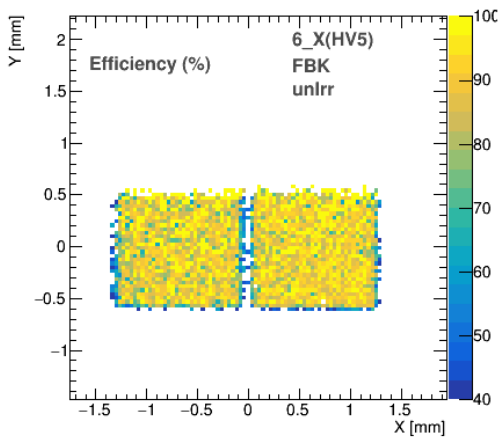


Depuis 2016 plusieurs campagnes de tests en faisceau au CERN pour tester les capteurs LGAD prévus pour HGTD.
Participation aux prise de données par le groupe du LPNHE et analyse des données.
Etude de l'uniformité des capteurs, de leur efficacité, charge, gain, résolution en temps...
Développement du programme de tracking utilisé par le working group de HGTD pour mesurer l'uniformité

Time resolution
$\sigma = (86 \pm 1)$ ps
$\sigma_{\text{SiPM}} = 86$ ps
$\sigma_{\text{LGA35}} = 29$ ps



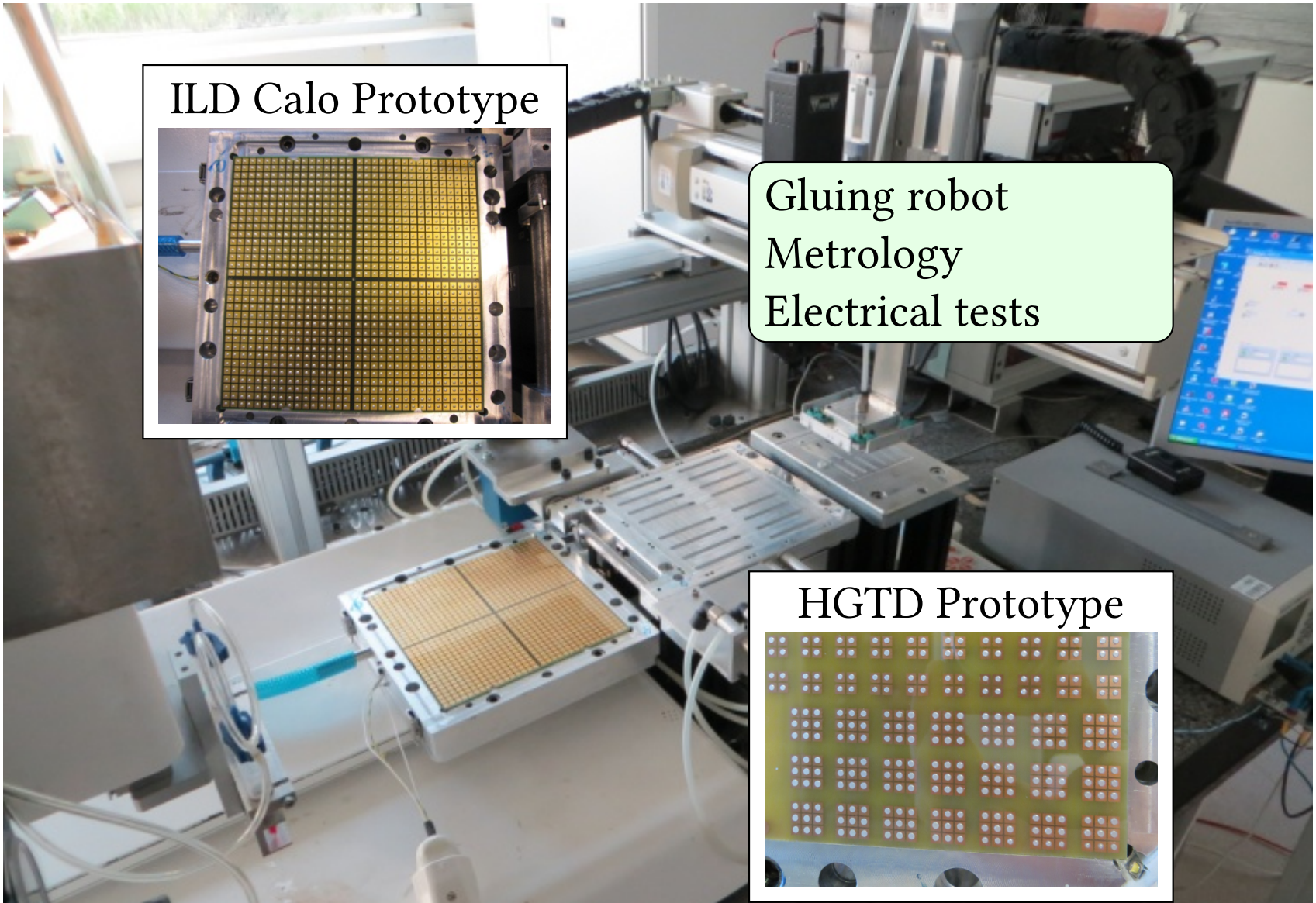




Calice

- Calice is an R&D program for the ILD SiW Electromagnetic Calorimeter at the future ILC collider.
- Currently in the lab there is limited quantity of personnel dedicated to Calice, but in the past a significant intrumentation has been developed.
- Limited activities planned beyond 2019. ILC schedule is still very uncertain.
- Synergy with other MIF projects (HGTD)

Calice @ LPNHE



Conclusions

- Both ATLAS Calo and ATLAS Tracking groups are engaged in the upgrade programs for the Phase-II of LHC (HL-LHC)
- This engagements imply various activities up to 2024-2026
- Upgrade Projects
  - ITk
  - HTT
  - HGTD
- The lab has also a technical activity for the Calice R&D project
  - Mainly due to uncertainties in the ILC approval/schedule this activity is limited
- We should start to think what we want to do next, after HL-LHC
  - ILC obvious candidate
  - Other leptop colliders?
  - Reflection: some of our key strenghts (hardware tracking, radiation hardness) are less attractive for a lepton collider, others are more