Laboratoire d'Annecy-le-Vieux de Physique des Particules

hipeCTA: High Performance Computing for CTA

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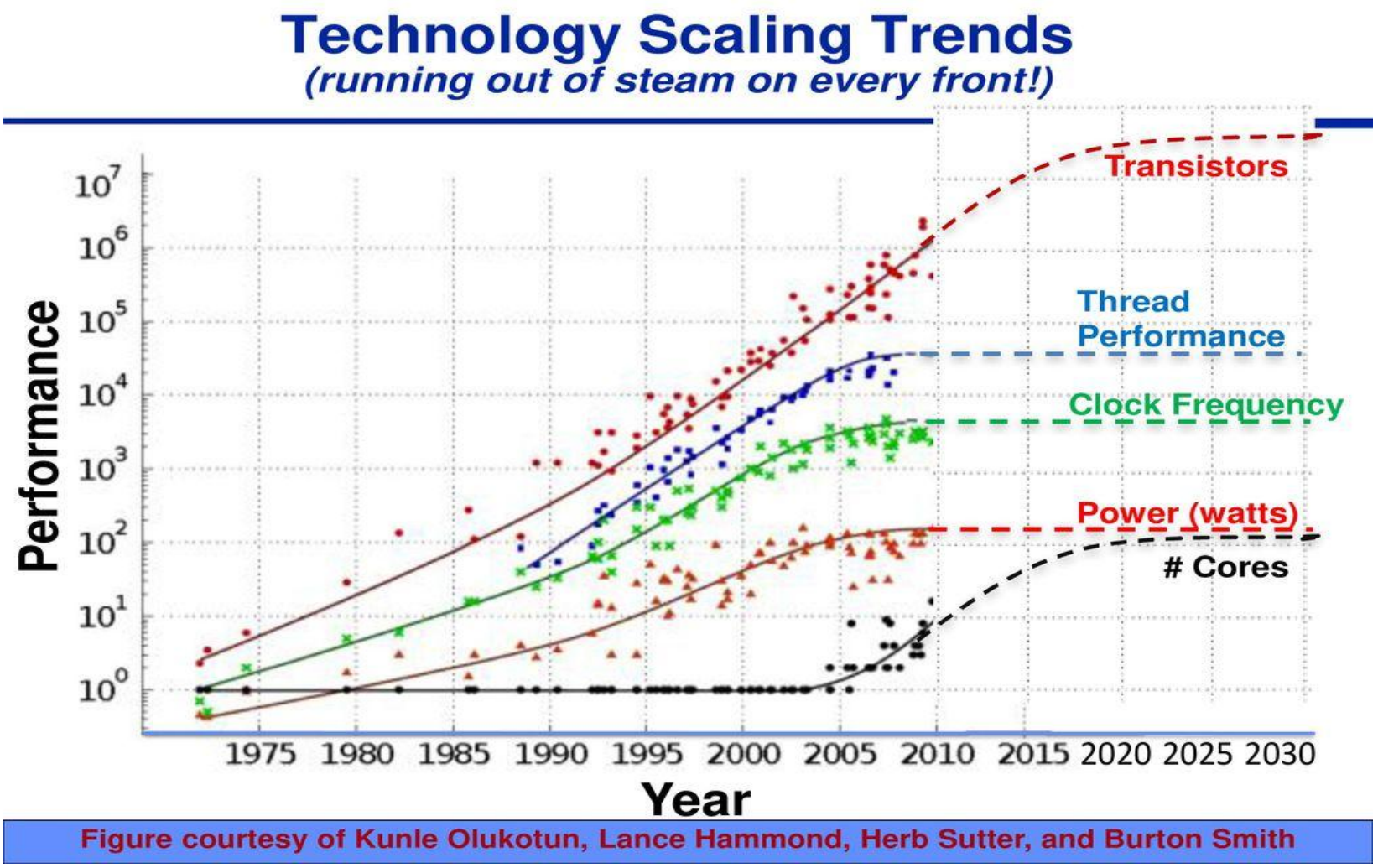
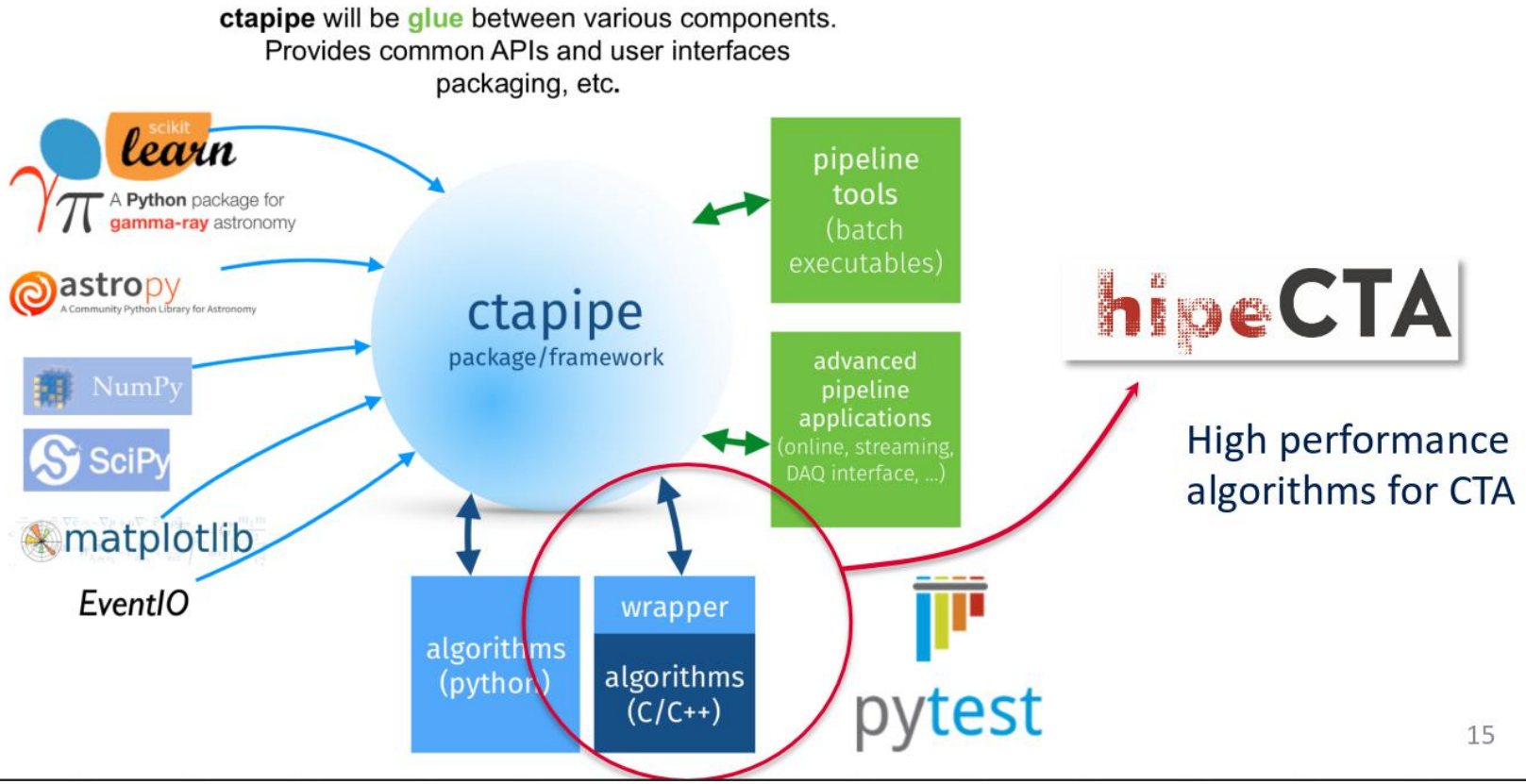
cta Asterics Astronomy ESFRI & Research Infrastructure Cluster cnrs UNIVERSITÉ SAVOIE MONT BLANC


Technology Scaling Trends
(running out of steam on every front!)
Performance
Year
Transistors
Thread Performance
Clock Frequency
Power (watts)
Cores
10^0
10^1
10^2
10^3
10^4
10^5
10^6
10^7
1975 1980 1985 1990 1995 2000 2005 2010 2015 2020 2025 2030
Figure courtesy of Kunle Olukotun, Lance Hammond, Herb Sutter, and Burton Smith

how to reduce the computation time ?

- Make the most out of the capabilities of modern CPUs
  - vectorization
    - SIMD process multiple data elements at the same time, with a single instruction.
  - data prefetching techniques
    - CPU automatically fetchs instructions or data from their original storage in slower memory to a faster local memory before it is actually needed

ctapipe + hipeCTA



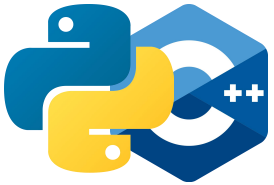
HiPeCTA, HiPeData and HiPeRTA

hipeCTA

- uses vectorization and makes the most of data prefecting
  - R0 to DL1 : Calibration , integration , cleaning, hillas parameters
  - It is developed to be used under the ctapipe framework.
    - Same functions API, unit tests based on ctapipe comparison
  - **HiPeRTA**
    - Real time analysis
    - share code/algorithms with HiPeCTA

hipeDATA

- a vectorization ready data format.
  - memory access patterns designed to make the most of data prefetching
    - Contiguous data, Cache Friendly
- proposed to CTA
  - Being benchmarked vs other formats



Computing performance benchmarks

- From hard drive (~100 MB/s max)

Format\Software	ctapipe	hipeCTA
simtel	~130hz (36 MB/s)	~196hz (54MB/s) *
hipedata	~165hz (45 MB/s)	~350hz (98MB/s)

*limited speed factor because of required copy data to 1, 2 or 3D **aligned** numpy array

- From RAM (DDR4) : target = RTA

Format\Software	ctapipe	hipeCTA	
simtel	~185hz	~370hz *	← I/O bound
hipedata	~280hz	~6300hz	← CPU bound

Note: 1hz = 1 image/s R0 ➡ DL1