UNIVERSITY OF BIRMINGHAM
SCHOOL OF PHYSICS AND ASTRONOMY

Silicon vertex tracker studies for a future electron-ion collider

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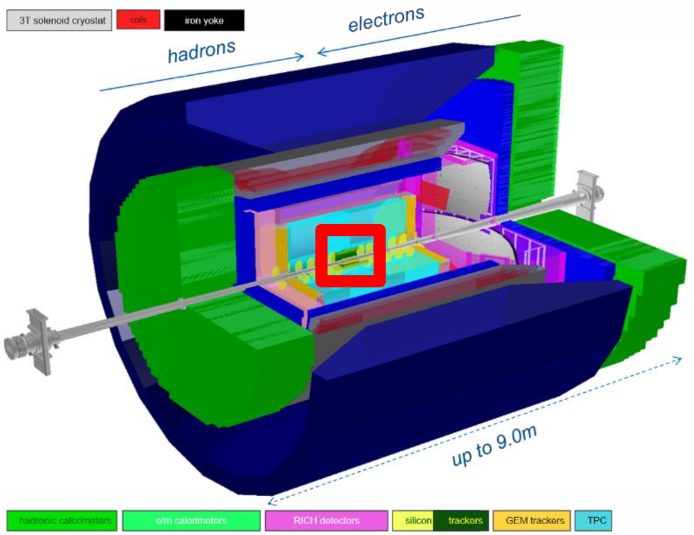
Outline

- Silicon vertex tracker
  – Why is it important?
- Simulations
  – Geometric parameters of the SVT
- Pixel sensors
  – The parts that make up the SVT
- Towards an EIC-specific sensor
- Conclusions and outlook

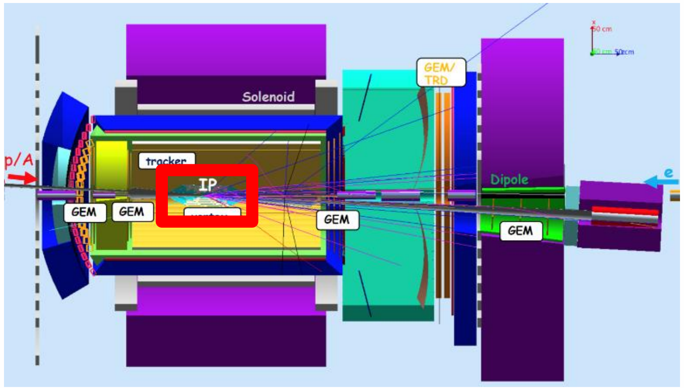
Silicon vertex tracker

- Innermost part of the detector.
- Main detector for **vertex position finding**
- Contributes to **momentum measurements**

- Requires:
  - **Very fine spatial resolution**, to separate primary and secondary vertices
  - **Low material**, to reduce multiple scattering
- Baseline used in studies: ALICE ITS upgrade



BeAST concept (BNL)
https://indico.cern.ch/event/722363/contributions/3031250/



JLEIC concept (JLab)
http://accelconf.web.cern.ch/AccelConf/ipac2017/papers/thpab084.pdf

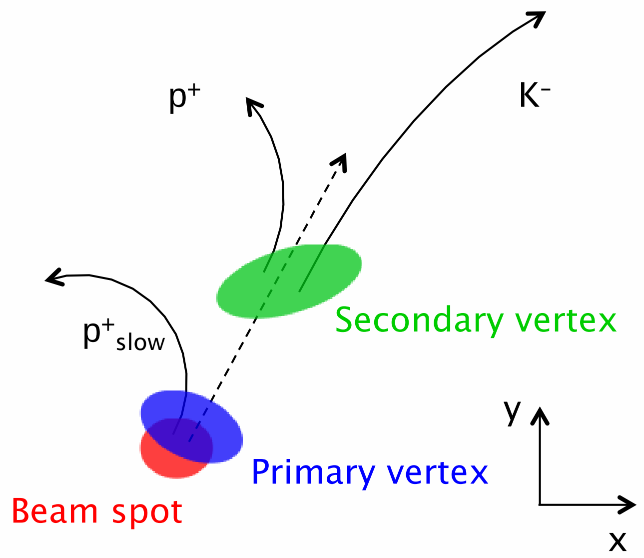
Open charm reconstruction

- Signature is **displaced (secondary) decay vertex**

Particle	Decay	Branching	$c\tau$ [μm]
D^0	$K^-\pi^+$	3.9%	123
D^+	$K^-\pi^+\pi^+$	9.5%	311
D^{*+}	$D^0\pi^+_{slow}$	67.7%	

Example:

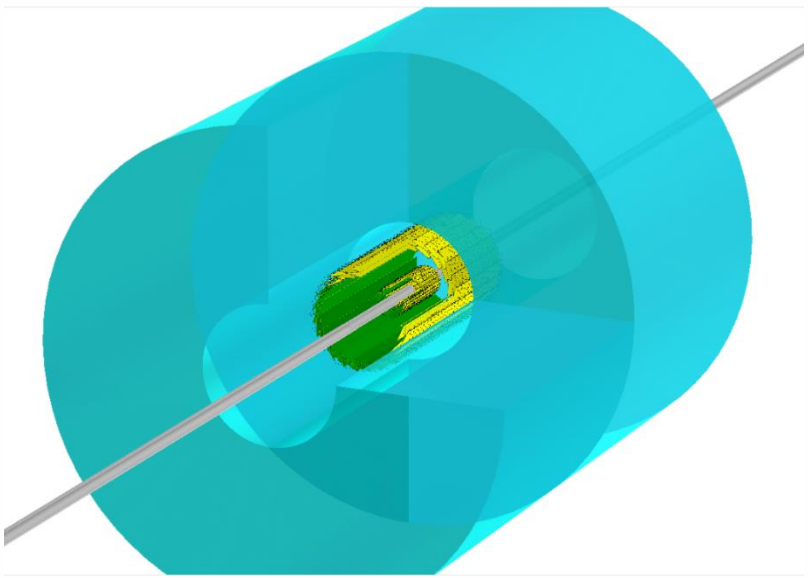
$$D^{*+} \rightarrow D^0 p^+_{slow} \rightarrow \left(K^- p^+\right) p^+_{slow}$$

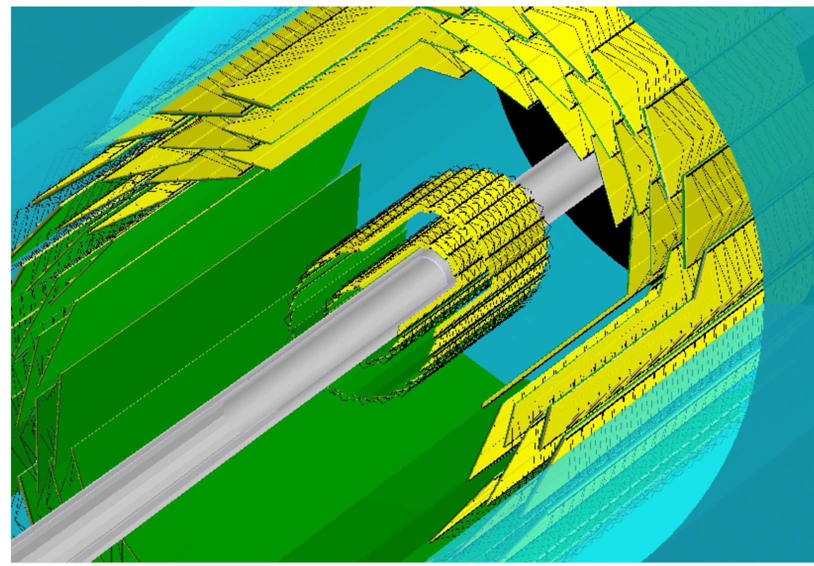


- Requires excellent impact parameter resolution in r-ϕ and z
  - Dominated by **position** and **resolution** of innermost tracking layer
    - Close as possible to beam pipe
    - Highest possible spatial resolution

Simulation studies

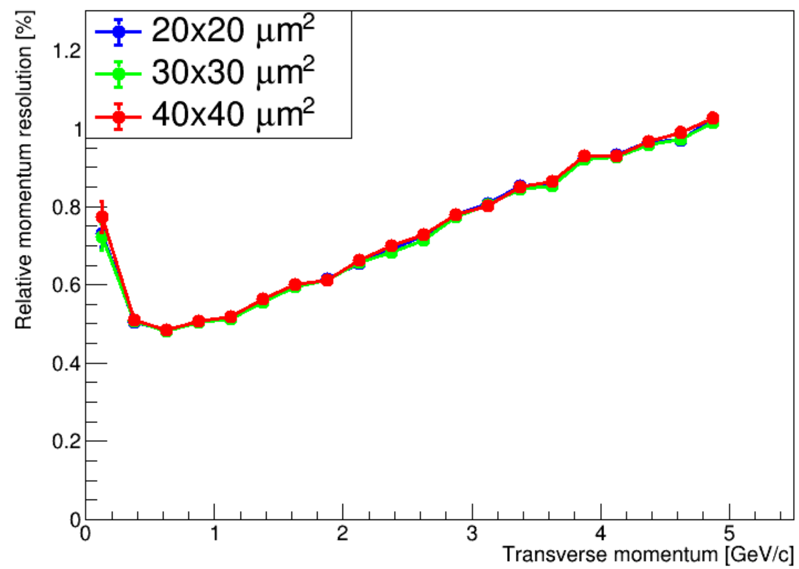
- Studies of full silicon vertex tracker done using **EICROOT**
  – A specific simulation package for the EIC, containing particle generator, GEANT propagation, hit digitisation, and track finding
- **Momentum resolution** and **pointing resolution** studied
- Different layouts and pixel sizes investigated



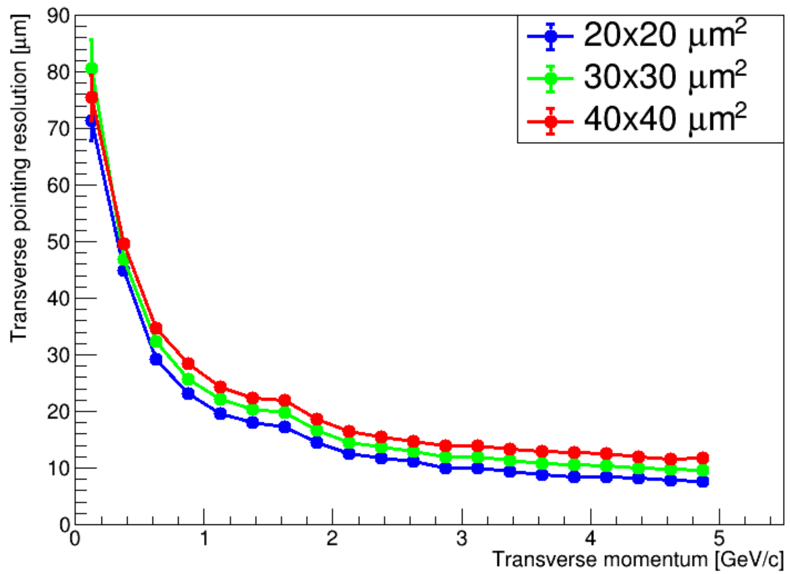


Simulation results – barrel pixel size

Relative momentum resolution



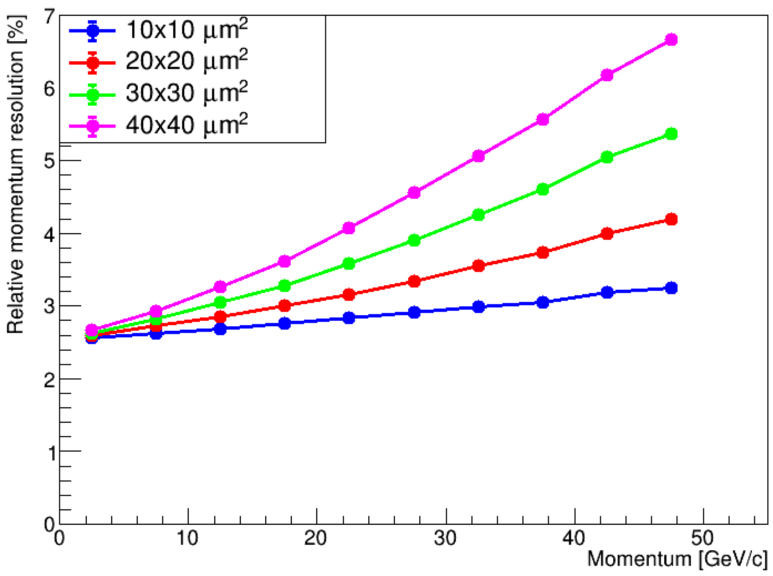
Transverse pointing resolution



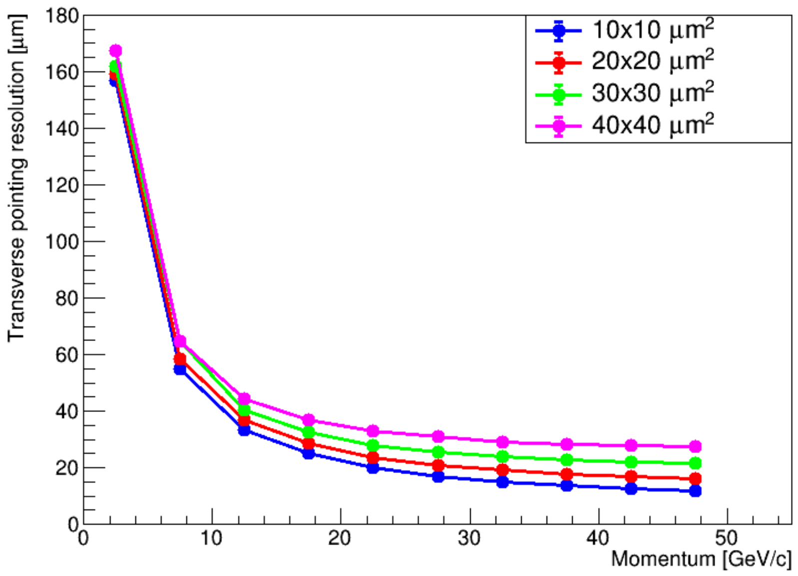
- Pseudorapidity |η| < 0.5 (barrel region)
- Pixel size has no effect on momentum resolution
- Pointing resolution improves with reduced pixel size

Simulation results – disk pixel size

Relative momentum resolution



Transverse pointing resolution

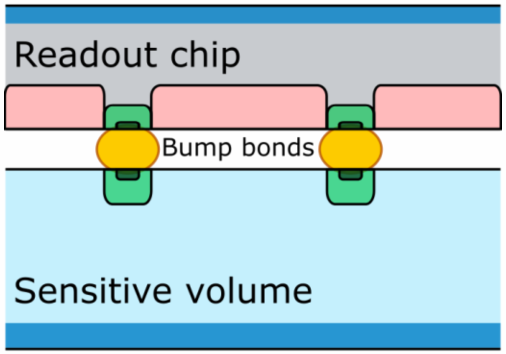


- Pseudorapidity η = 3 (disk region)
- Both **momentum resolution** and **pointing resolution** improve with reduced pixel size
- For best performance: **use small pixels** located **near the interaction point**

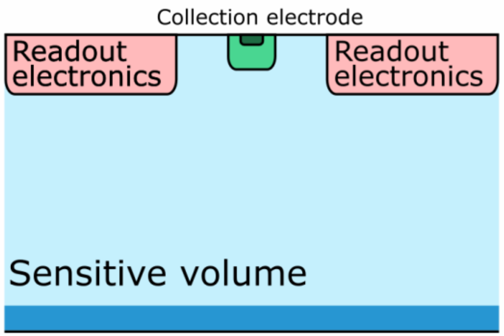
Pixel sensors

- Hybrids
  - Sensitive volume and readout electronics on separate chips
  - Up until now most commonly used in silicon vertex trackers
  - Radiation tolerant and fast
- Monolithic Active Pixel Sensors (MAPS)
  - Sensitive volume and readout electronics on same chip
  - Made using commercial CMOS technology
  - Thin and fine granularity
- Depleted Monolithic Active Pixel Sensors (DMAPS)
  - Utilising high voltage/high resistivity CMOS technology
  - Depleted volume intended to be as large as possible

Hybrid sensor



Monolithic sensor



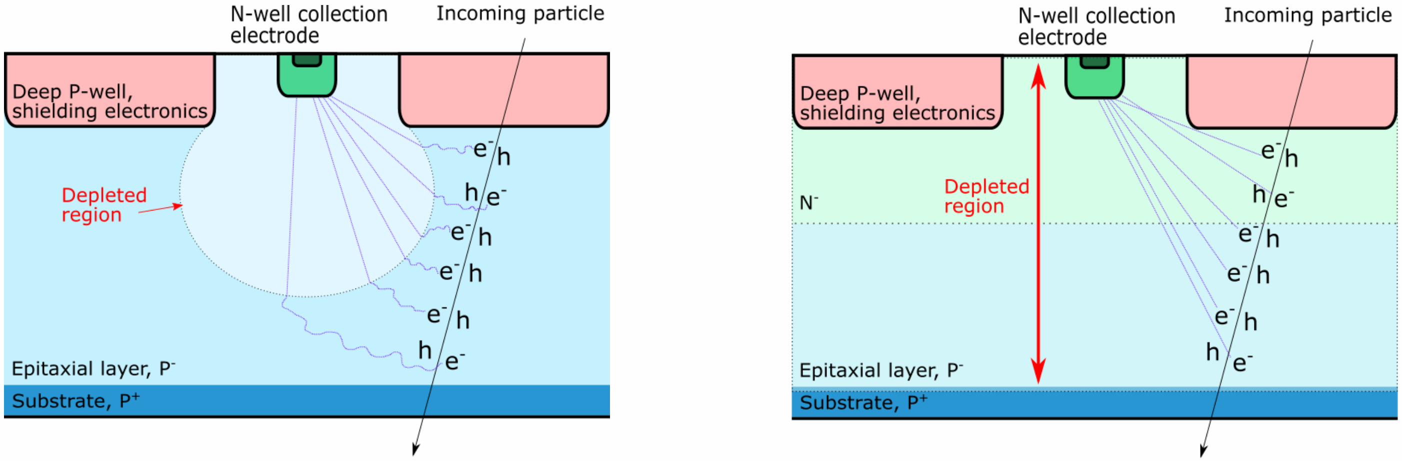
Advantages of DMAPS

- Lower cost
- Mass production in commercial CMOS technologies
- Lower material budget
- Avoids bump-bonding (complex and laborious)

- Depletion gives **faster** and **more uniform** charge collection compared to standard MAPS

TowerJazz Investigator

- TowerJazz 180 nm CMOS imaging process
- Monolithic test chip, with many different pixel flavours.
  - Different pixel size, collection electrode size, spacing between collection electrode and p-well with electronics
- Two process versions; standard and modifed
  - Modified has a deep planar junction to **increase depletion**
- Measurements made using iron-55 source.

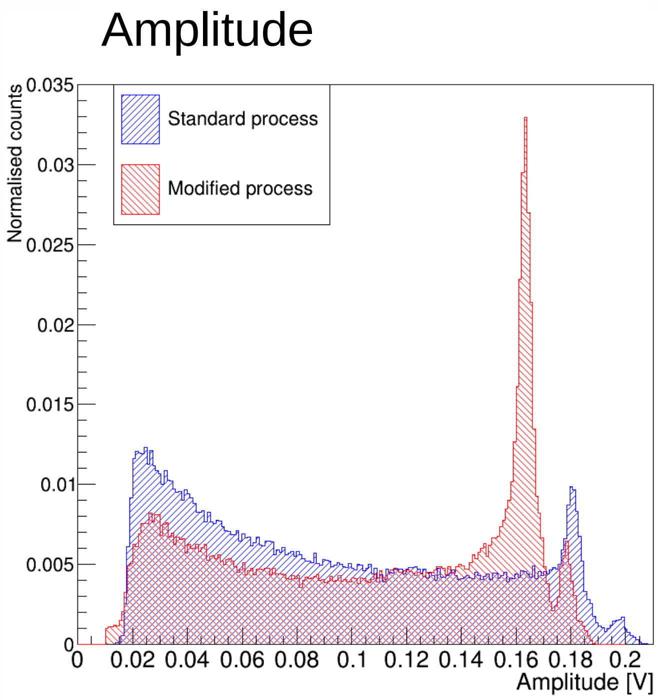


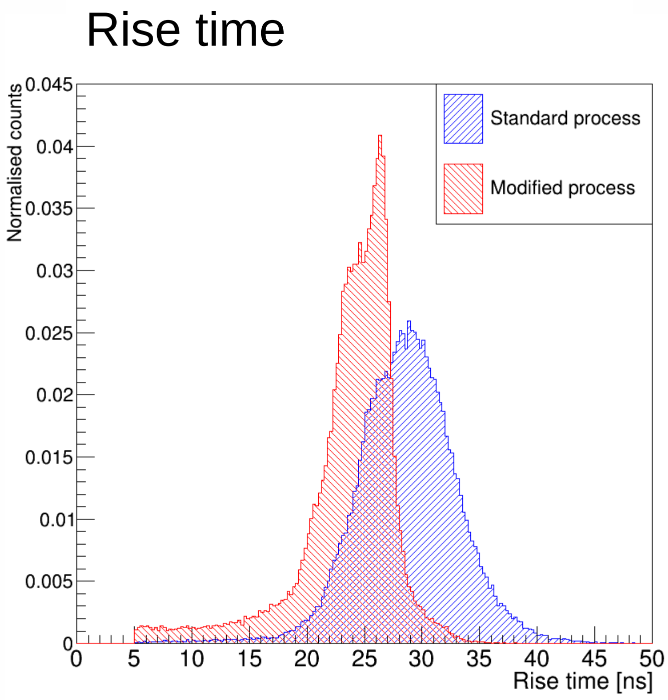
Standard process (MAPS) Modified process (DMAPS)

W. Snoeys et al, http://dx.doi.org/10.1016/j.nima.2017.07.046

Results

- Results shown for a 28x28 µm^2 pixel

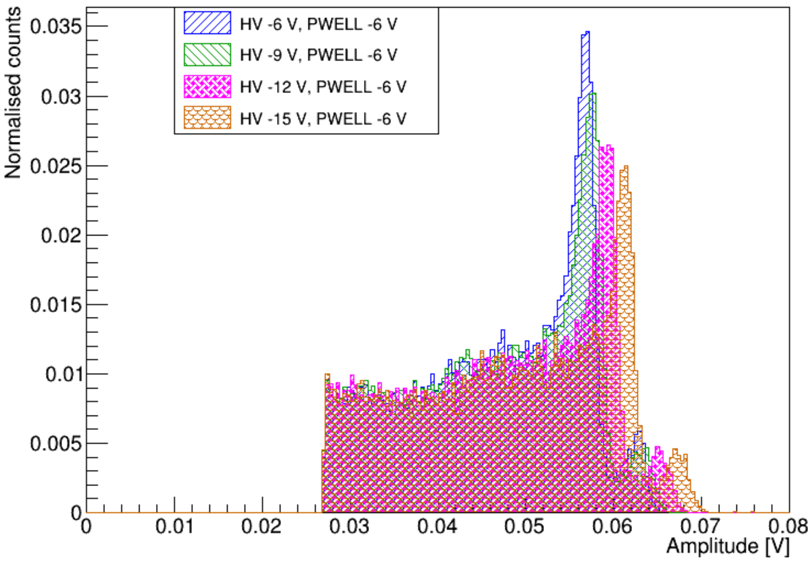


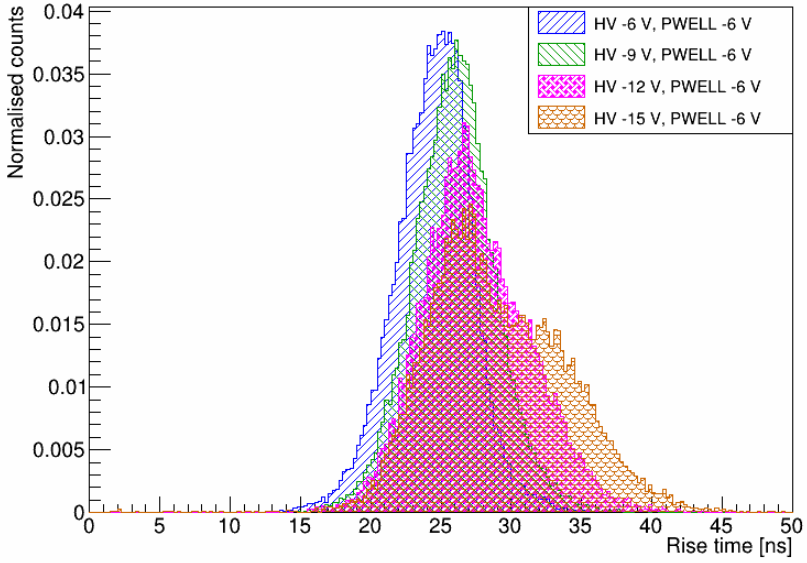


- For a 20x20 µm^2 pixel, the differences are smaller
- For larger pixels and spacing, the modified process shows worse performance

Results

- Chip in modified process dubbed TJ1B enables separate biasing of p-well and substrate (HV)
- Results of different substrate biasing shown below





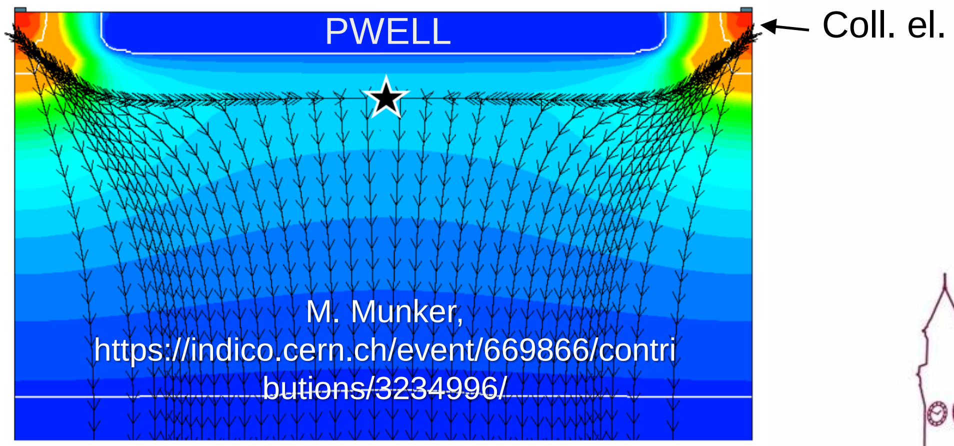
- Increasing substrate voltage **decreases signal-to-noise ratio**
- Increasing substrate voltage makes rise-time distribution **wider**

Conclusions of technology investigation

- Modified process performs better up to 30x30 µm^2 pixel size
- Smaller difference between processes at smaller pixels
  - Due to higher relative depletion already in the standard process
- Higher bias voltage does **not** improve signal
  - Due to shape of electric field: **minimum at pixel border**

- Results consistent with simulations and published results from similar sensor [1]
- Higher potential difference between p-well and substrate gives **longer path** and **slower charge collection**

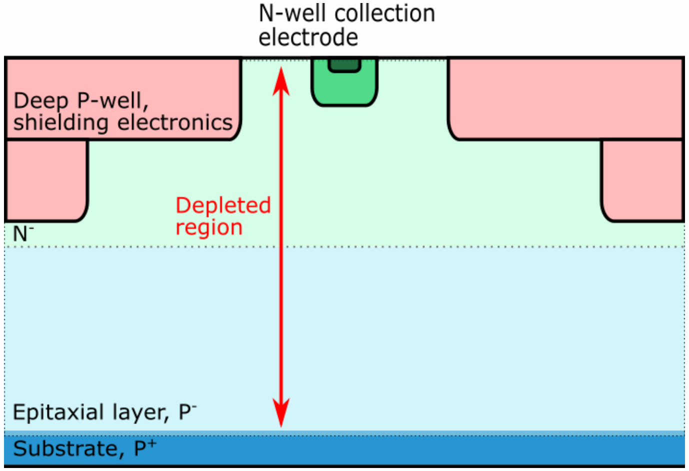
TCAD simulation - electrostatic potential minimum at pixel border:

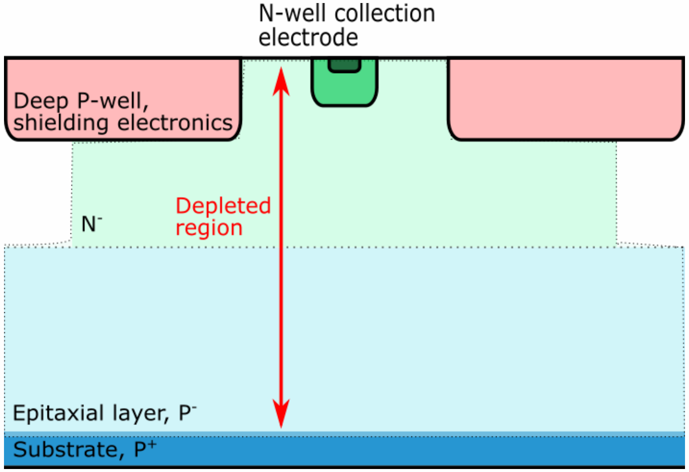


[1] M. Munker et al. https://doi.org/10.1088/1748-0221/14/05/C05013

miniMALTA chip

- Pixels modified to fix the problem at edges
  - Extra deep p-well
  - Gap in the n layer
- Both modifications made to ”funnel” the electric field towards collection electrode
- Analysis ongoing of testbeams of this chip. Initial results positive
- Publication in the works





M. Munker et al. https://doi.org/10.1088/1748-0221/14/05/C05013

Towards an EIC-specific sensor

- Work with chip designers at the Rutherford Appleton Laboratory (RAL)
- Goals:
  - Develop high-granularity silicon vertex tracker
  - Investigate feasibility of time-stamping layer
- Time-stamping bunch crossings keeps track of **polarisation** in event
- Challenges: timing and pixel size
- Latest results: Timing resolution of **4 ns** can be reached, using a constant fraction discriminator
  - **Not** possible in small pixels
- Study ongoing

	EIC DMAPS Sensor	
Detector	Silicon vertex tracker	Time stamping layer
Technology	TowerJazz 180 nm	
Pixel size [μm x μm]	20x20	Max 350x350
Integration time	2000 ns	
Timing resolution	N/A	< 9 ns (BNL) < 1 ns (JLAB)
Power	< 35 mW/cm^2	
Radiation fluence	< 10^{10} 1 MeV neq/cm^2	

Conclusions and outlook

- Results so far:
  - Simulations show that we want **small pixel size** and detector layers **close to the beampipe**
  - TowerJazz modified process suits our needs, but **sensor layout is crucial**
  - Extra modifications can potentially be beneficial
    - Needs further investigation
- Current work:
  - Analysing miniMALTA testbeam data
  - Finish simulating different detector layouts, focusing on the area encompassing both barrel and disks
- Future work:
  - Continued sensor development with RAL
  - Full event reconstruction in simulations, investigating heavy-flavour observables
  - Test of single-photon avalanche diodes (SPADs)
  - Tests of the TowerJazz MonoPix chip (from Bonn)

Thank you for your attention

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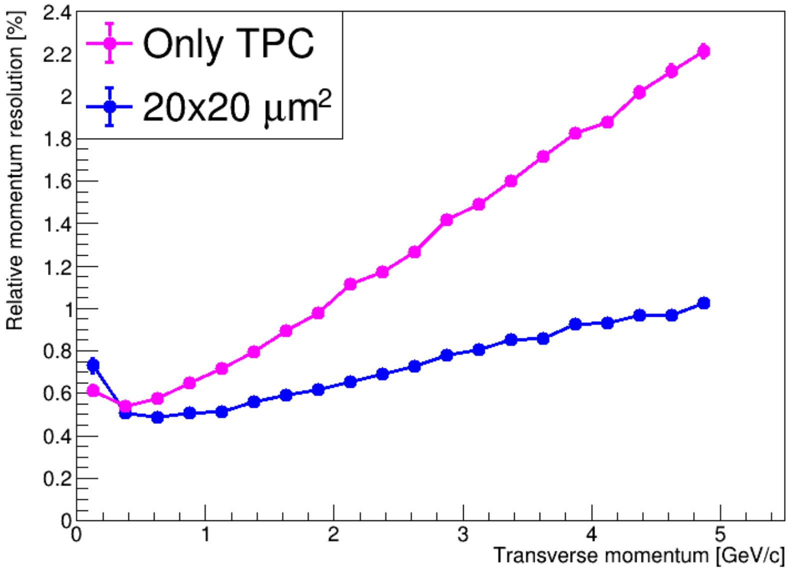
BILPA

EIC R&D
eRD18

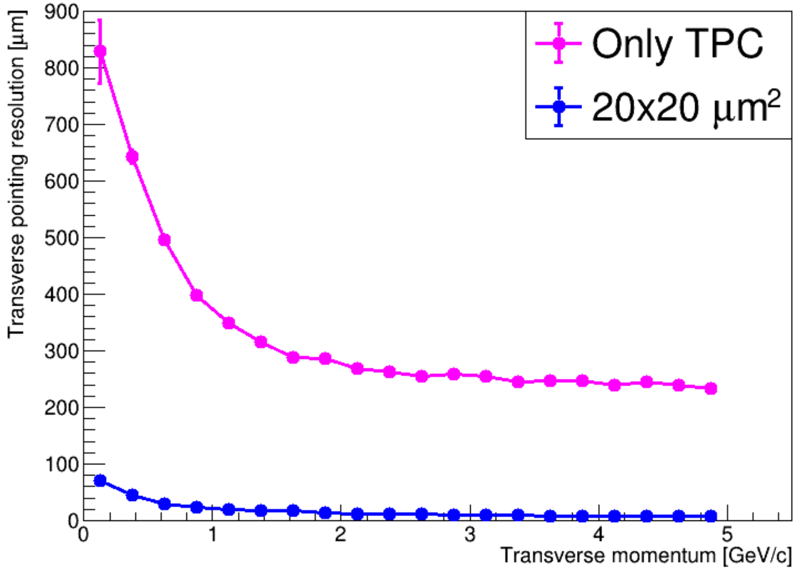
Backup

Simulation results

Relative momentum resolution



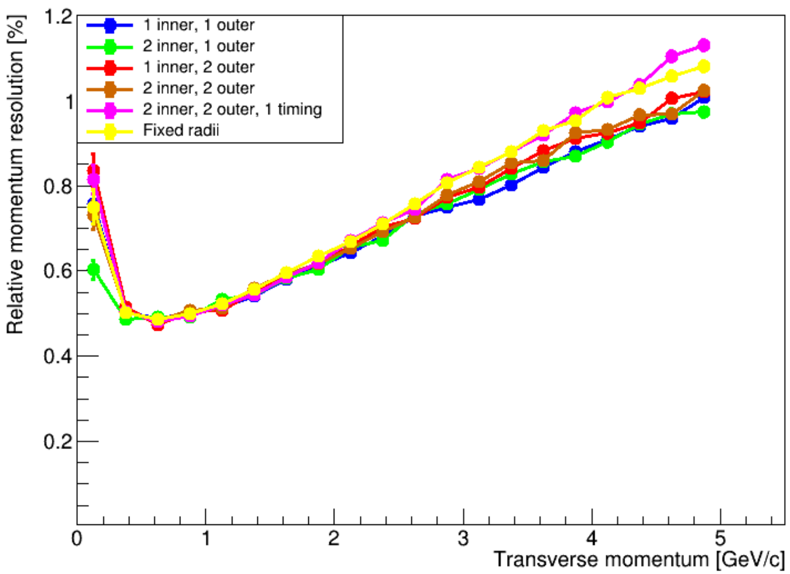
Transverse pointing resolution



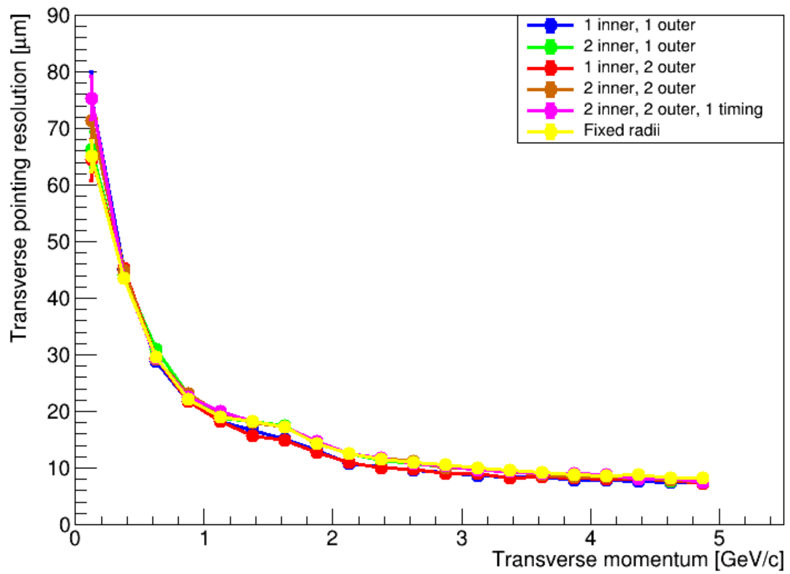
- Relative momentum resolution better for only TPC at very low momenta, due to multiple scattering
- Everywhere else, a SVT improves performance

Simulations – different layouts

Relative momentum resolution

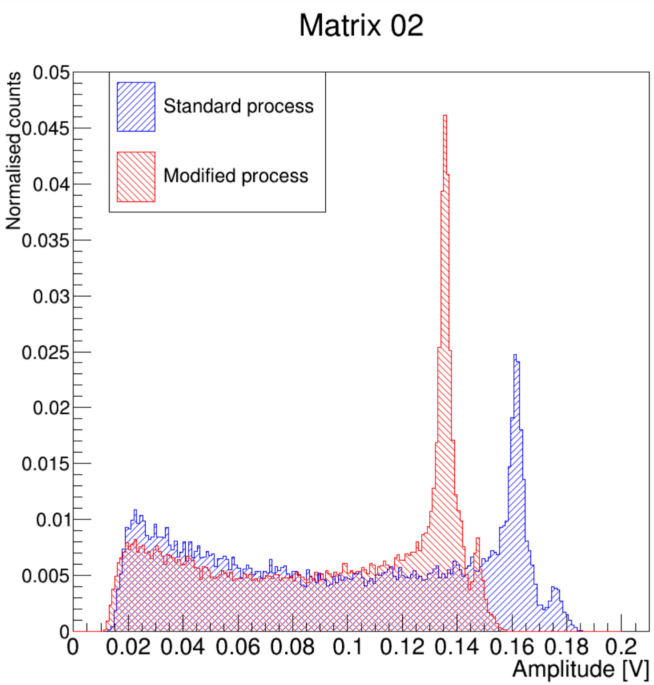


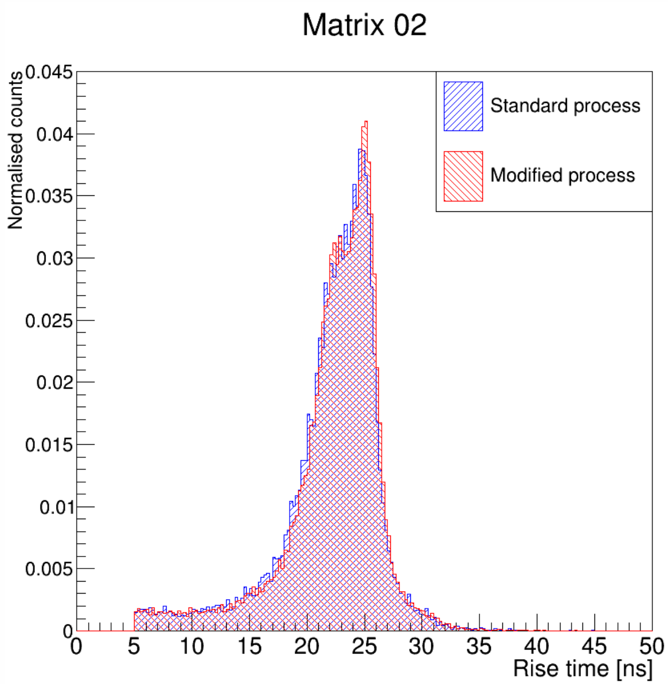
Transverse pointing resolution



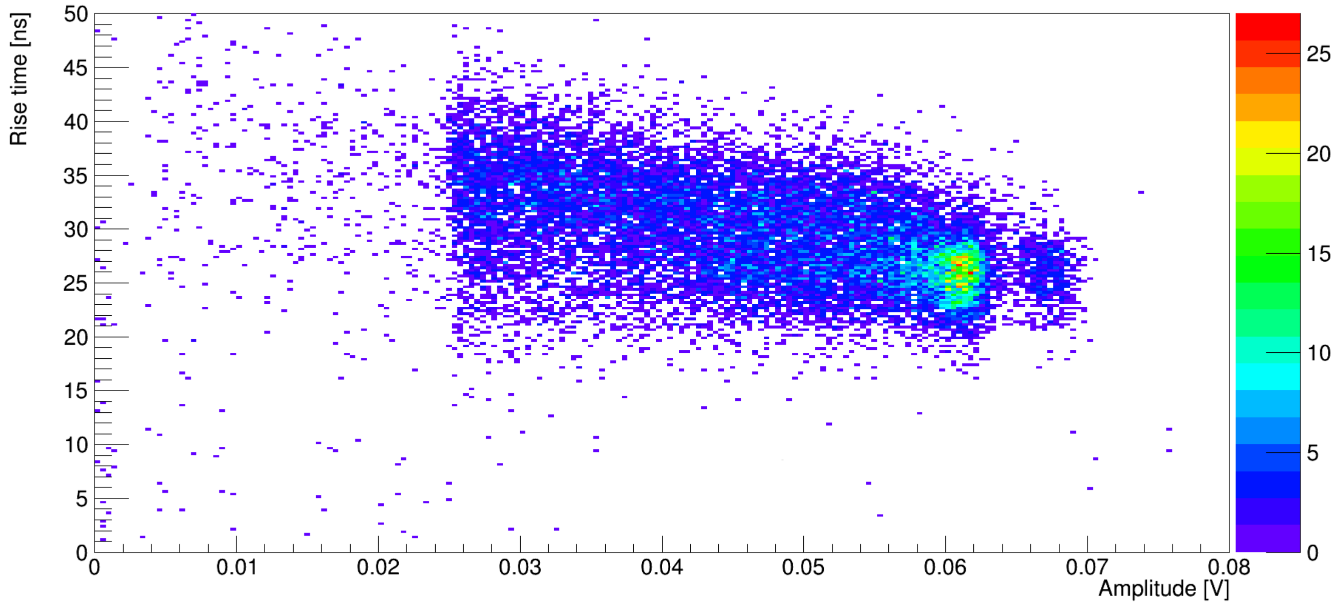
- Different layer configurations and positions (details available on request)
- Not much difference for different configurations
- relative momentum resolution slightly worse when a thick timing layer (1.6% X_0) is added
  - This is the case in ”fixed radii” as well

Results - 20x20 µm² pixel





Rise time vs amplitude



- 28x28 μm^2 pixel, HV -15 V, PWELL -6 V
- Smaller charges come from pixel border (due to charge sharing)
- Smaller charges have longer rise times
- Conclusion: Increasing HV makes charges from pixel edges arrive later at the collection electrode