The ALICE Inner Tracking System Upgrade and future plans

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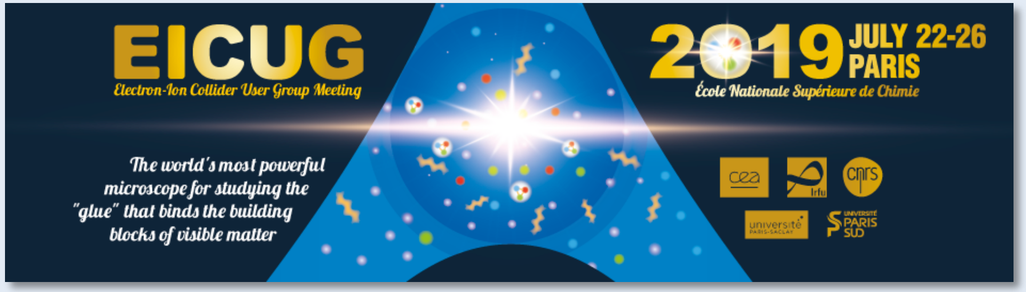
ALICE-PUBLIC-2018-013 https://cds.cern.ch/record/2644611



Outline

- **ALICE LS2 Upgrade**
- **LS2 Inner Tracking System Upgrade (ITS2)**
  - Motivations
  - Detector layout
  - ALPIDE: Monolithic Active Pixel Sensor
  - Main components and material budget
- **Concepts for a future fast and lightweight heavy-ion detector**
  - Motivations
  - Design guidelines
  - Vertex detector
  - New MAPS sensor
  - Roadmap

ALICE Upgrades in LS2 (2019-2020) – Layout and key systems

New Inner Tracking System (ITS)

Novel MAPS technology

- CMOS Active Pixel Sensors

→ improved resolution, less material, faster readout

New Muon Forward Tracker (MFT)

- CMOS Active Pixel Sensors

→ vertex tracker at forward rapidity

New TPC Readout Planes

Largest GEM application

- 4-GEM detectors, new electronics

→ continuous readout

New trigger detectors (FIT, AD)

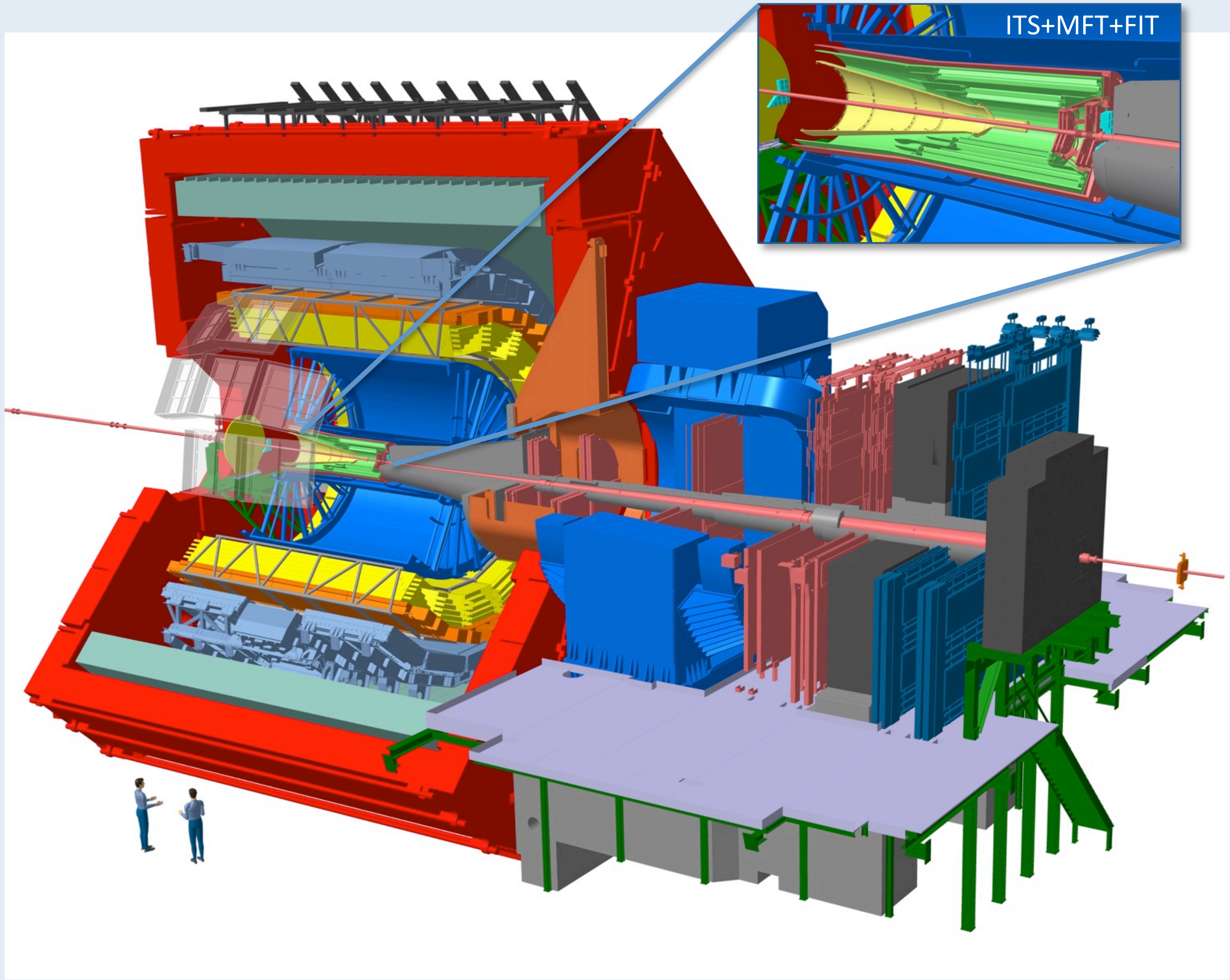
- Centrality, event plane

Upgrades readout

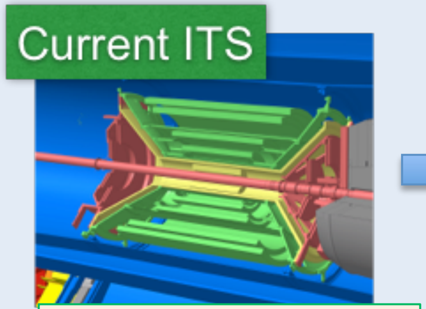
- TOF, TRD, MUON, ZDC, Calorimeter

Integrated Online-Offline system (O^2)

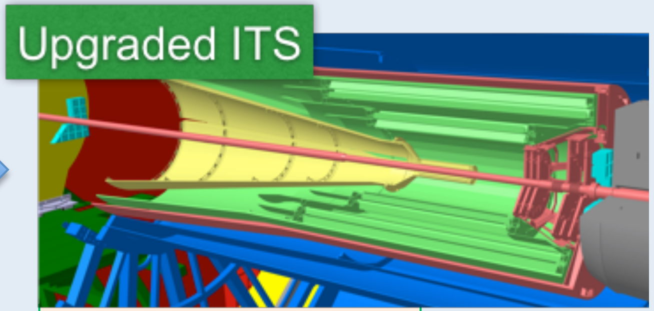
- Record minimum-bias Pb-Pb data at > 50kHz (currently ~ 1 kHz)



ITS Upgrade in LS2 (ITS2)



6 layers
39mm < r < 440mm
-1 ≤ η ≤ 1



7 layers
22mm < r < 400mm
-1.3 ≤ η ≤ 1.3

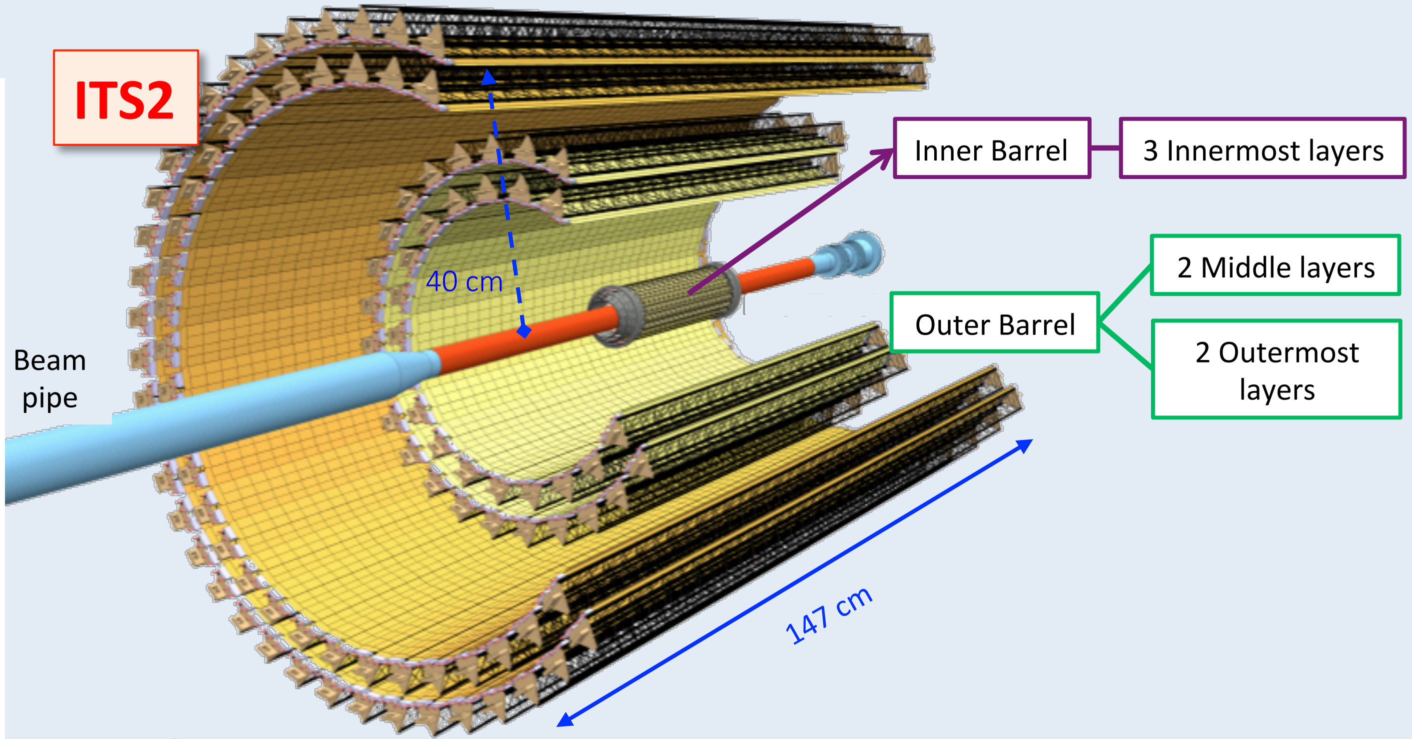
Motivations and goals

- Improved vertex and tracking precision and efficiency at low p_T
  - ☞ closer to IP, smaller pixels, less material
- Faster readout

Based on novel MAPS ALPIDE (vs ITS1)

- $10\ m^2$ active silicon area, 12.5 G-pixels
- Closer to interaction: **22 mm** (39mm)
- Higher intrinsic resolution (smaller pixels):
  - **~5 μm** in rϕ and z directions (12 and 100 μm)
- Power density < $40mW / cm^2$
- Max particle rate ~ $100MHz / cm^2$ (w/o pile-up)
- Fake hit rate: **< $1Hz/cm^2$**
- Less material: **~0.3% X_0 for Inner Barrel** (1.1% X_0)
- Faster readout: **100 kHz Pb-Pb** (1 kHz)

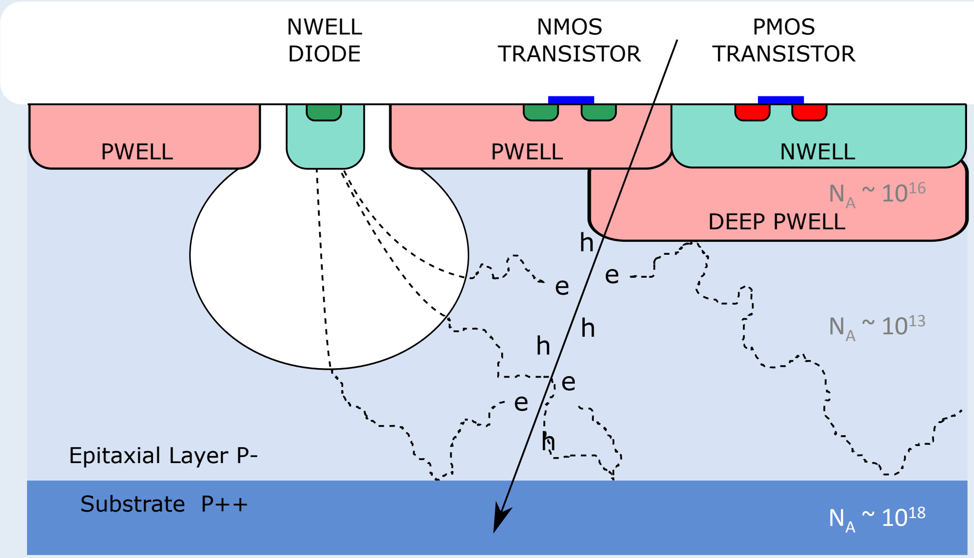
ITS2



⇨ further improvements exploiting technological innovations

ITS Upgrade in LS2 (ITS2)

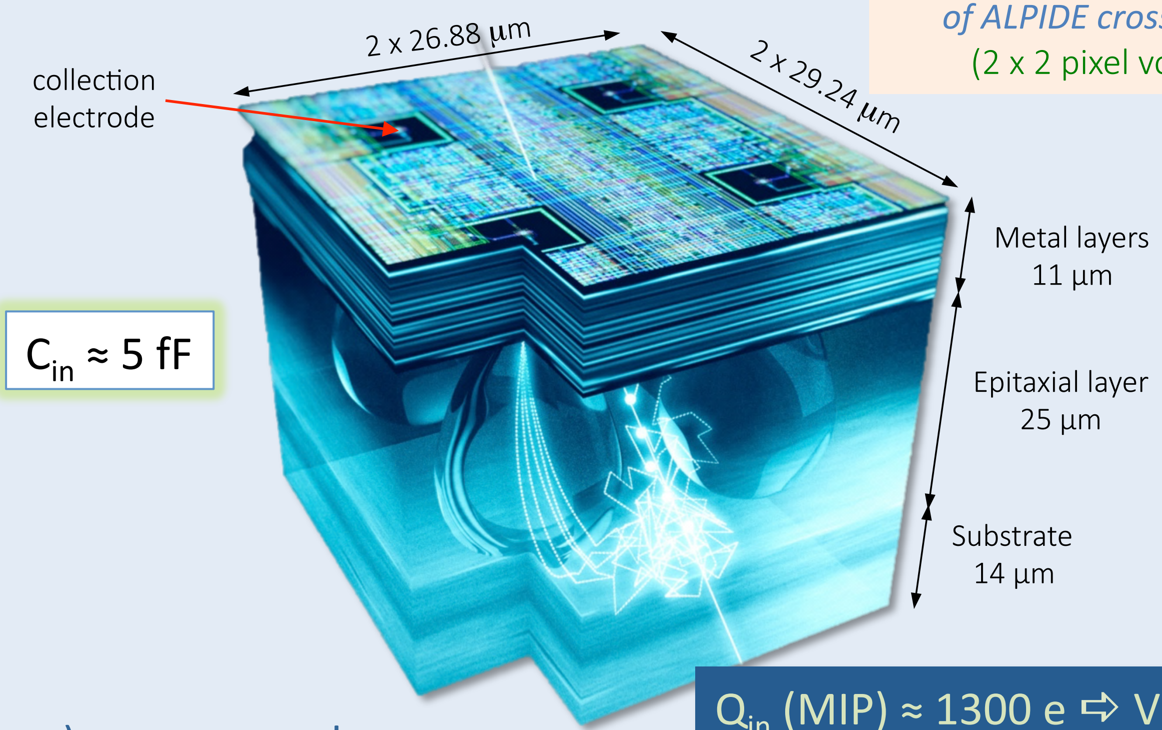
ALPIDE: CMOS Pixel Sensor using TJ 0.18μm CMOS Imaging Process



pixel capacitance ≈5 fF (@ V_{bb} = -3 V)

$C_{in} \approx 5$ fF

Artistic view of a SEM picture of ALPIDE cross section (2 x 2 pixel volume)

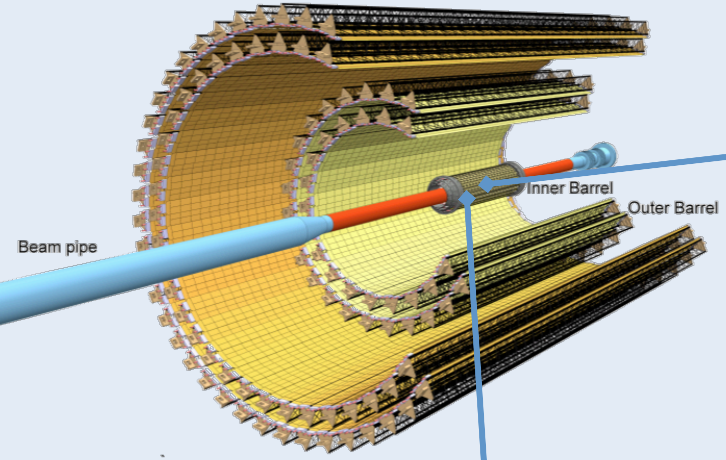


Q_{in} (MIP) ≈ 1300 e ⇨ V ≈ 40mV

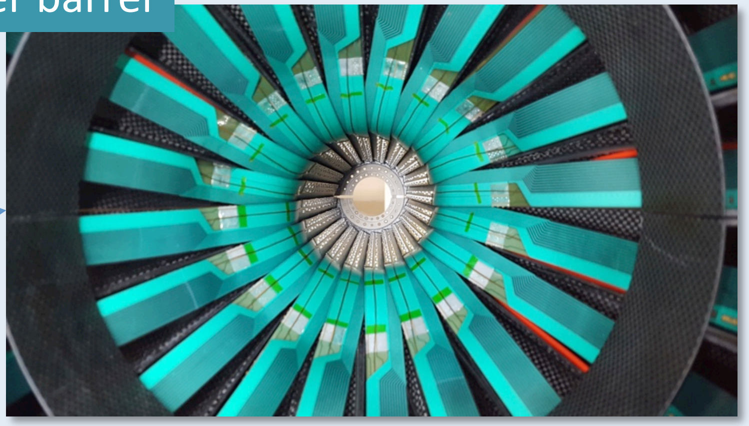
- High-resistivity (> 1kΩ cm) p-type epitaxial layer (25μm) on p-type substrate
- Small n-well diode (2 μm diameter), ~100 times smaller than pixel => low capacitance (~fF)
- Reverse bias voltage (-6V < V_{BB} < 0V) to substrate (contact from the top) to increase depletion zone around NWELL collection diode
- Deep PWELL shields NWELL of PMOS transistors

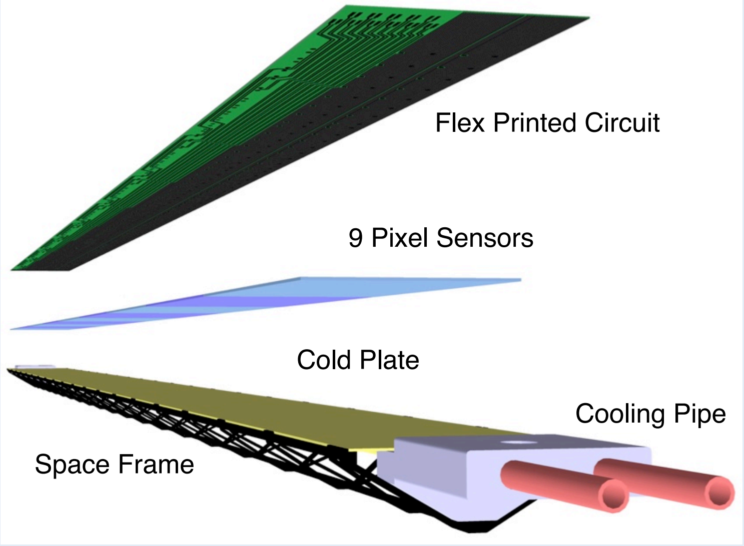
➔ full CMOS circuitry within active area

ITS2 – Material Thickness

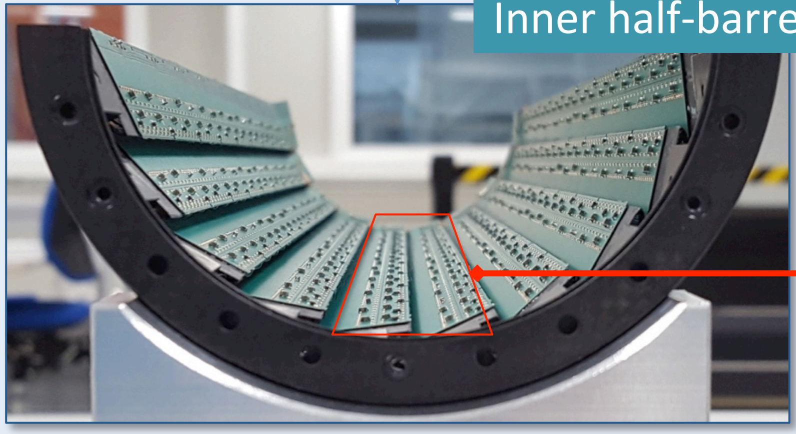


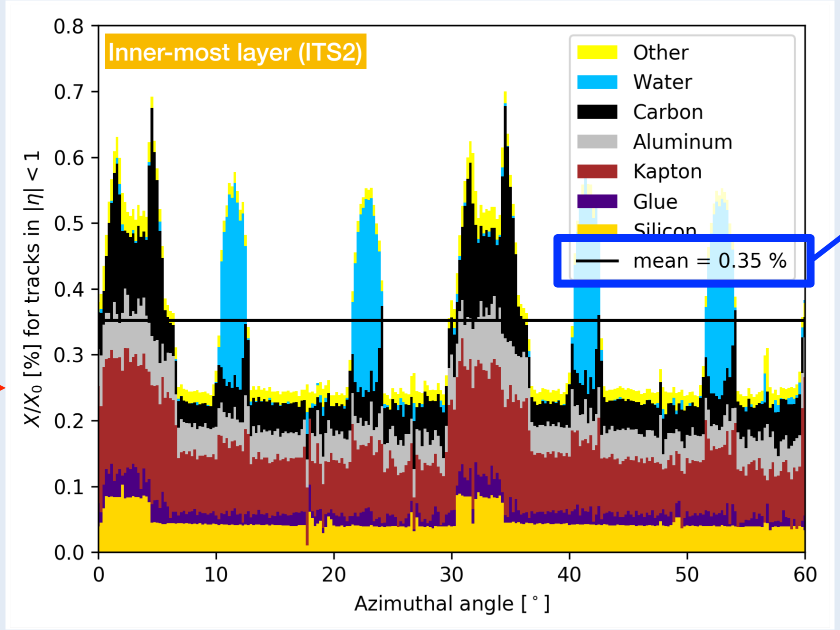
Inner barrel





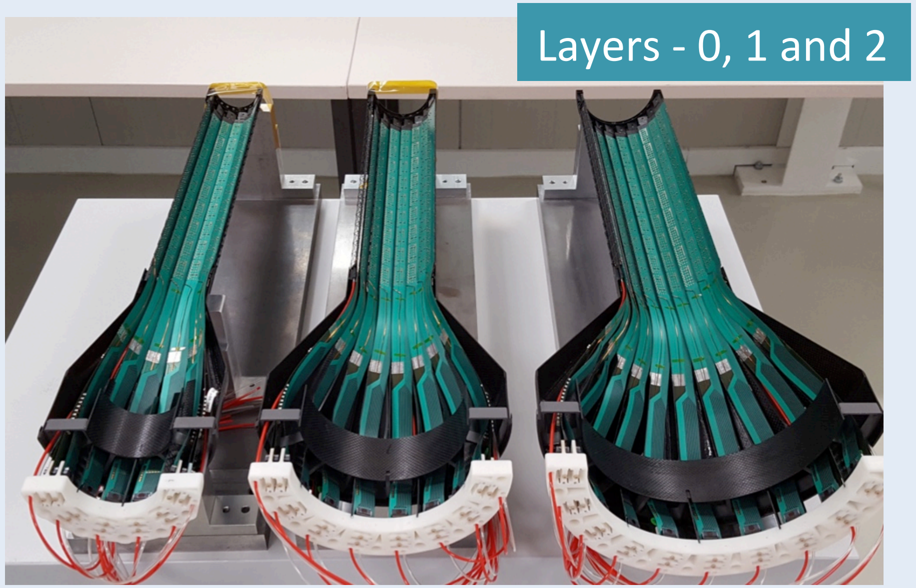
Inner half-barrel

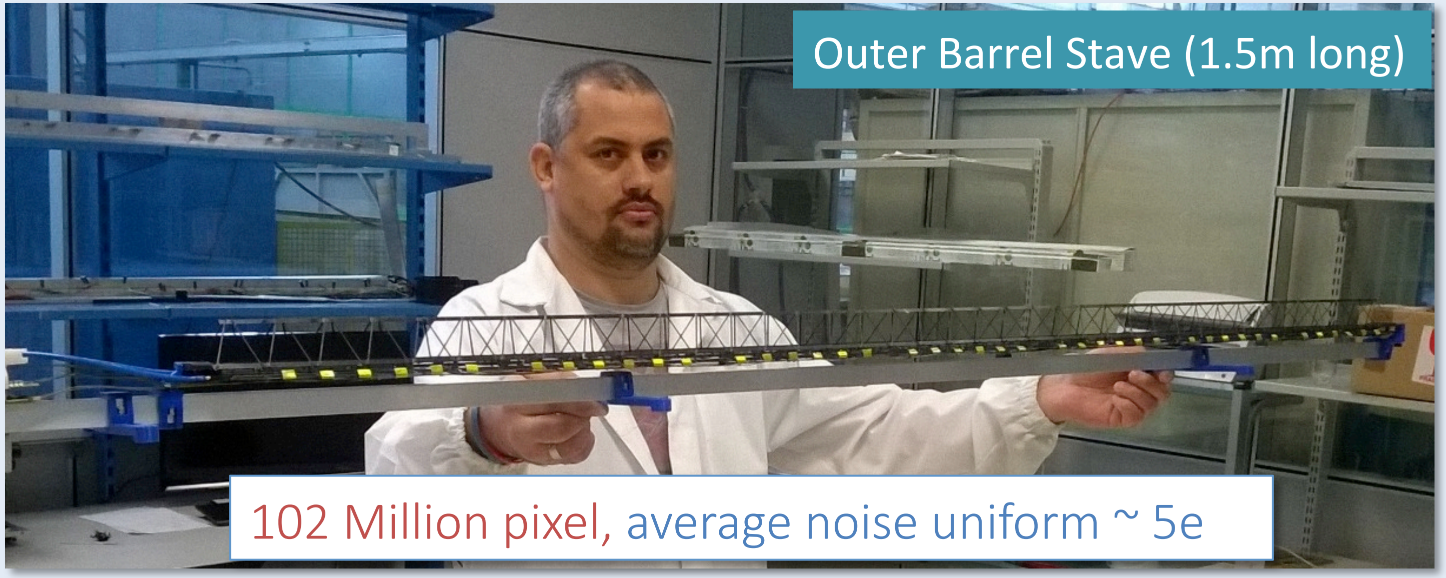




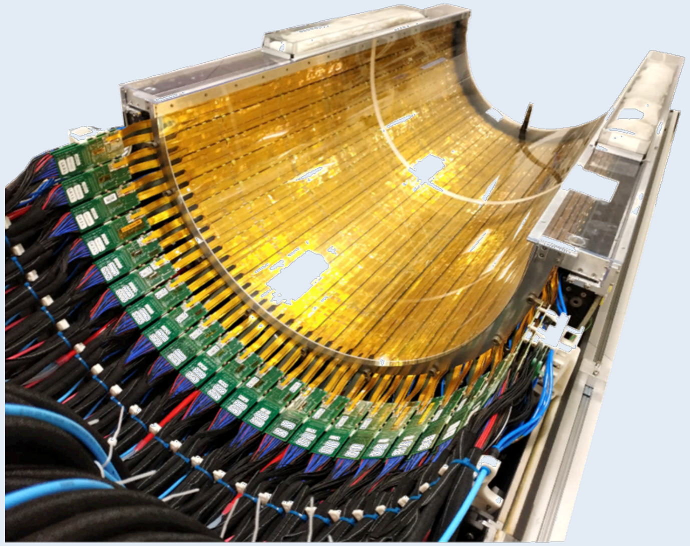
Silicon ⇨ only 15%

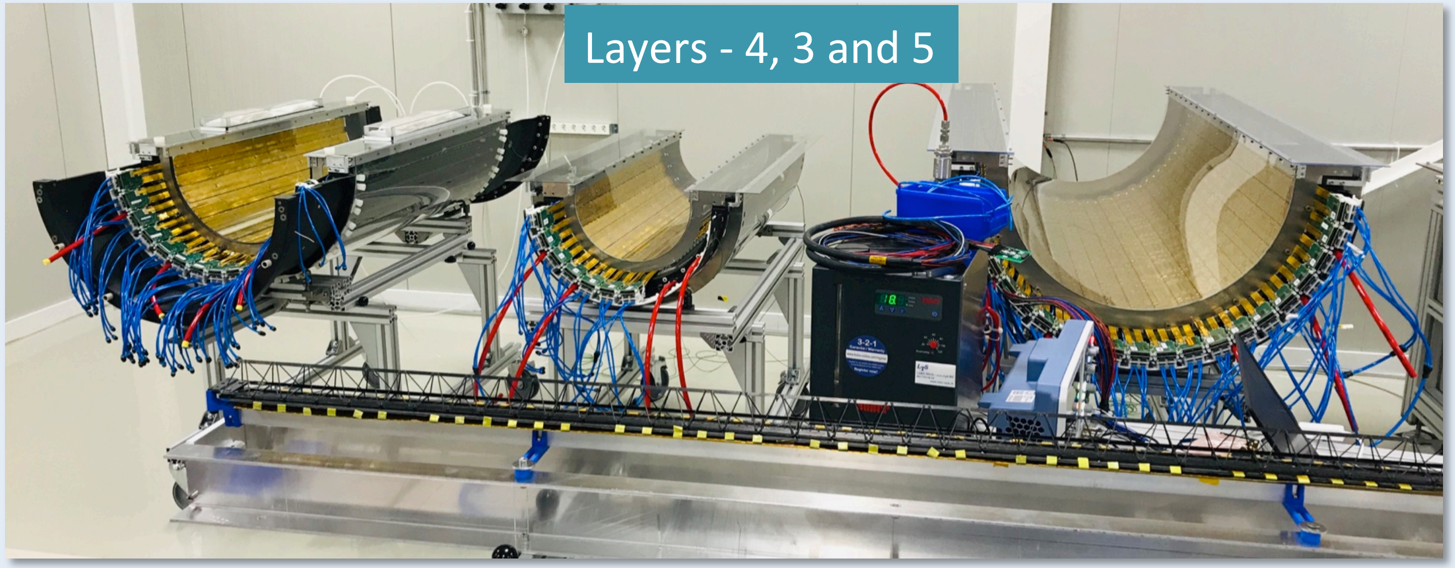
ITS Upgrade in LS2 (ITS2)


Layers - 0, 1 and 2


Outer Barrel Stave (1.5m long)

102 Million pixel, average noise uniform ~ 5e




Layers - 4, 3 and 5

TPC Continuous Readout with GEMs (Gas Electron Multiplier)

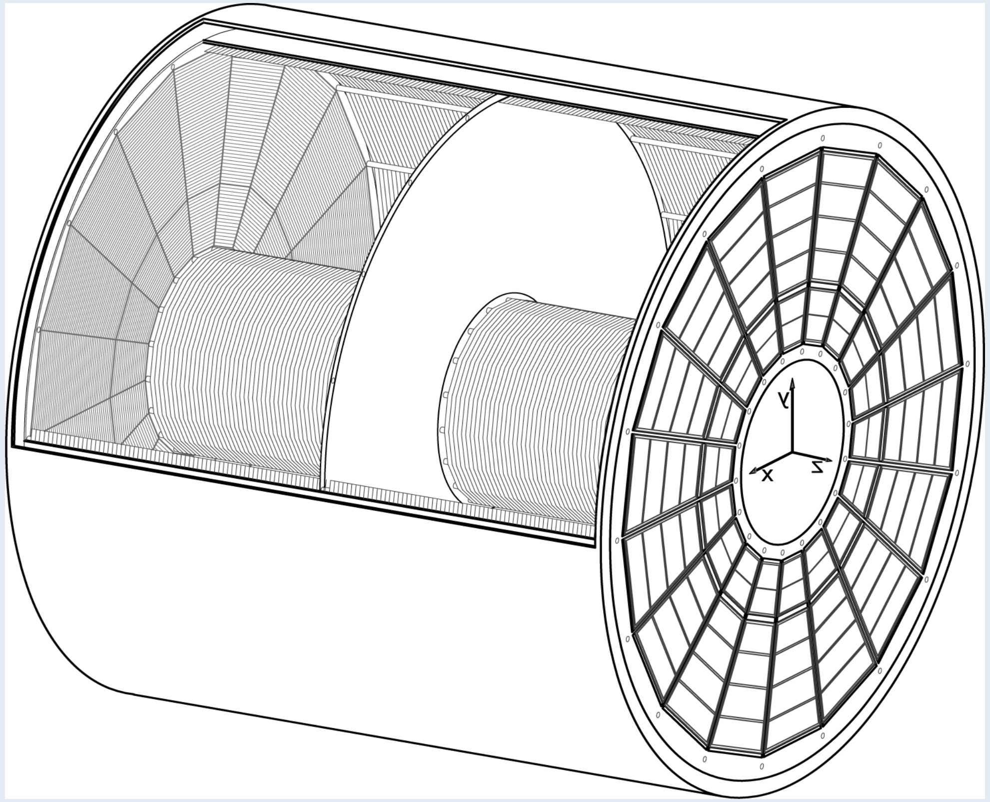
Gate-less TPC for continuous readout

Current MWPC: readout rate limited by ion backflow

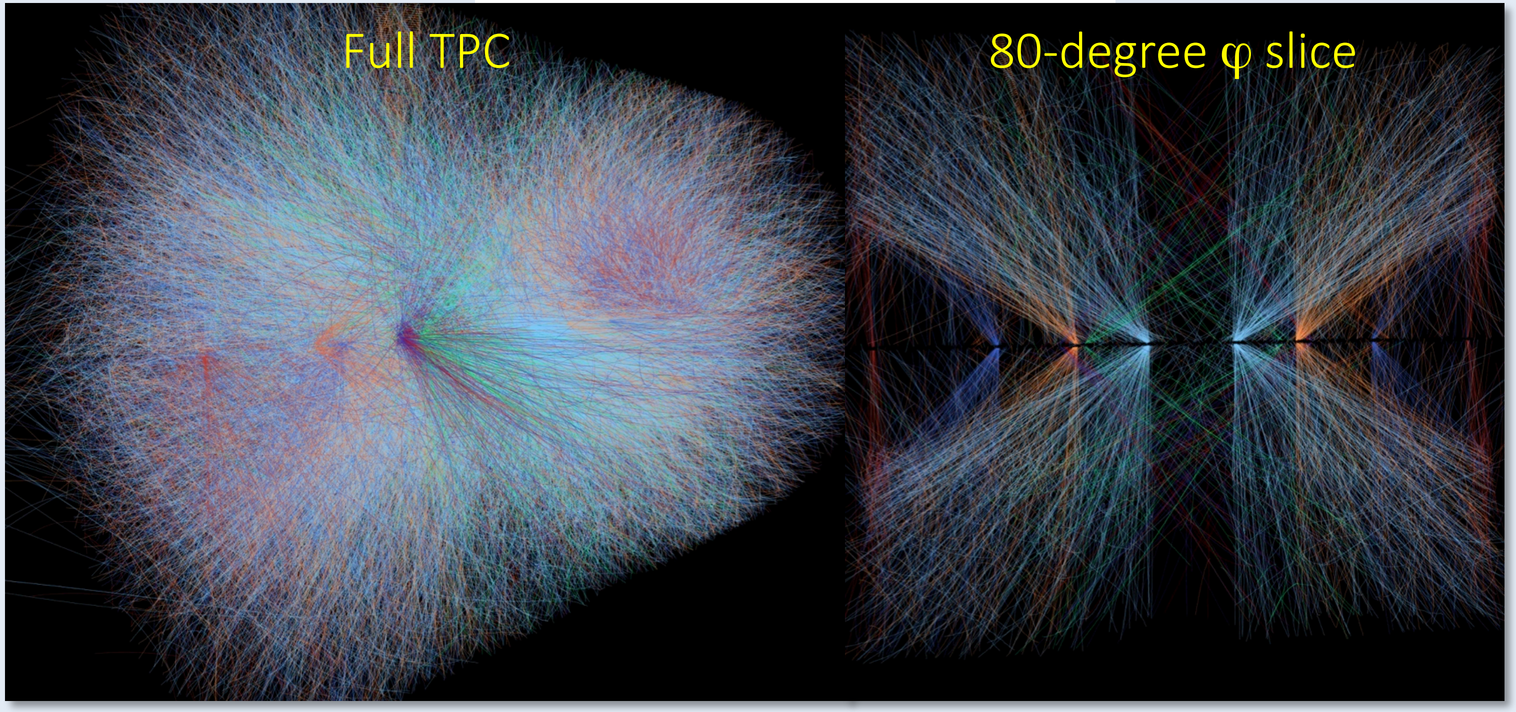
Operate TPC at 50 kHz ⇨ no gating grid

Need to minimize IBF ⇨ Replace MWPC with 4-GEMs

100 m^2 single-mask foils GEM production



Pb-Pb Collisions @ 50kHz



⇨ GEM provides ion backflow suppression to **< 1%**

⇨ 524 000 pads readout continuosly (10bit x 5MSPS) via 6552 links ⇨ **3.4 TByte/sec**

A new HI dedicated experiment beyond LS4?

With the LS2 upgrade, ALICE will reach the maximum rate with a spectrometer based on a TPC

⇨ Maximum interaction rate limited by space-charge (ions) accumulated in drift volume (distortions ≈10cm) and track density (inner region signal occupancy ≈ 40%)

Running at higher rates seems excluded with a TPC

Running ALICE beyond RUN4? ⇨ Completely new detector without TPC

The use of CMOS technologies opens new opportunities

⇨ Vertex detectors, large area tracking detectors and digital calorimeters

- enhanced performance (very high spatial and time resolution)

an “all-MAPS” detector

☞ *Such a detector could play a central role in HI physics at the LHC in the 2030’s*

A new HI dedicated experiment beyond LS4?

Design guidelines

- Increase rate capabilities (factor 50 wrt to ALICE RUN4): $<L_{NN}> \sim$ up to 10^{34} $cm^{-2}s^{-1}$
- Improve vertexing
  - Ultra-thin wafer-scale sensors with truly cylindrical shape, inside beampipe
  - spatial resolution < 3μm
  - material thickness < 0.05% X_0 /layer
- Improve tracking precision and efficiency
  - About 10 layers with a radial coverage of 1m
  - Spatial resolution of about 5μm up to 1m
  - whole tracker could be less than 6% X_0 in thickness (at mid-rapidity)
- Tracking over a wide momentum range, down to a few tens of MeV/c, and rapidity coverage $|\eta| \leq 4$

Magnetic fields of < 0.5T would be sufficient but 1T is also considered

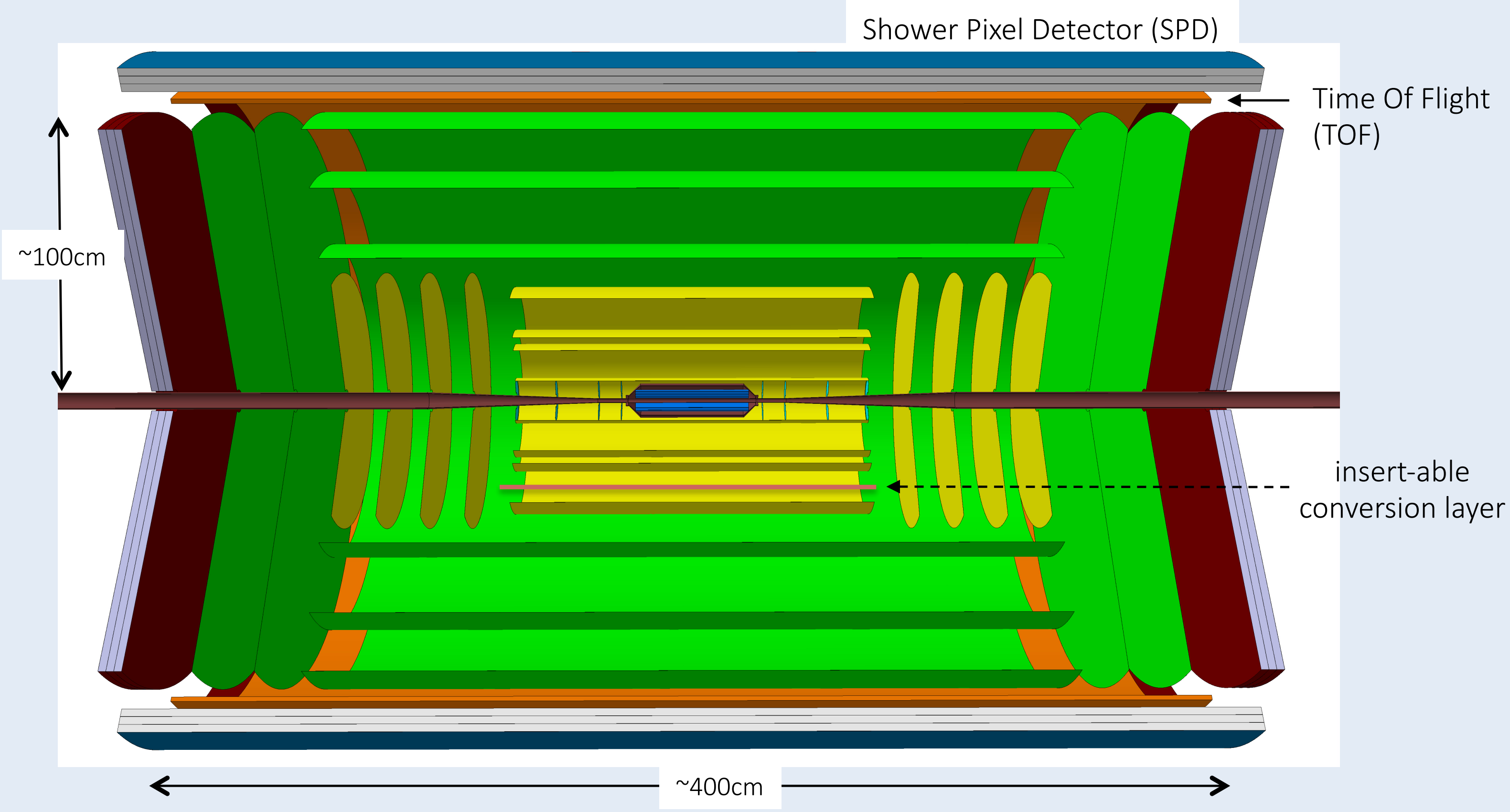
A new experiment based on a “all-silicon” detector

Tracker: ~10 tracking barrel layers (blue, yellow and green) based on CMOS sensors

Particle ID:

- TOF with outer silicon layers (orange)
- Shower Pixel Detector (outermost blue layer)

Extended rapidity coverage: **up to 8 rapidity units**



Magnetic Field

- B = 0.5 or 1 T

Spatial resolution

- Innermost 3 layers: $\sigma < 3\mu m$
- Outer layers: $\sigma \sim 5\mu m$

Vertex material thickness

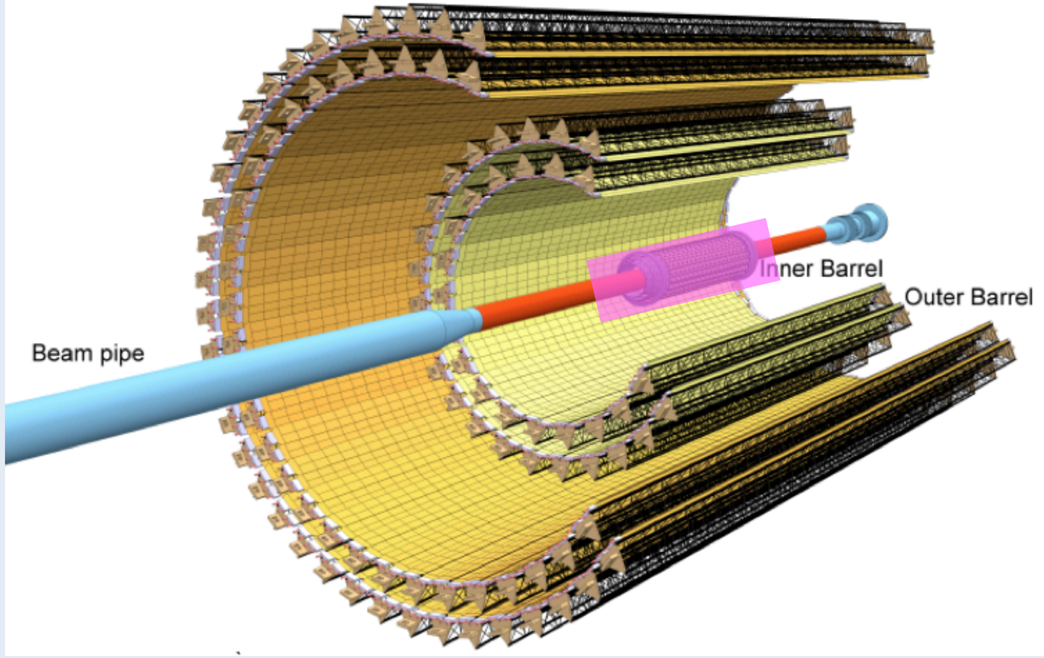
- X/X0 ~ 0.05% / layer

Time Measurement

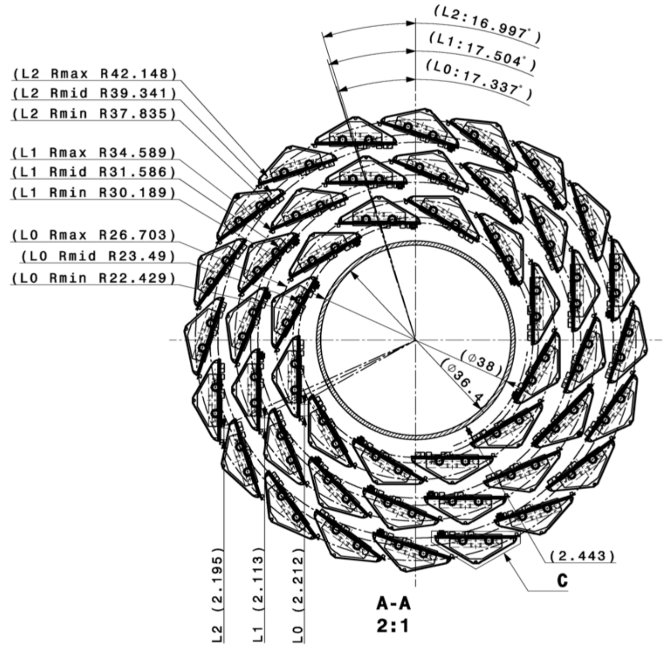
Outermost layer integrates high precision time measurement ($\sigma_t \sim 20ps$)

ITS Upgrade in LS2 (ITS2)

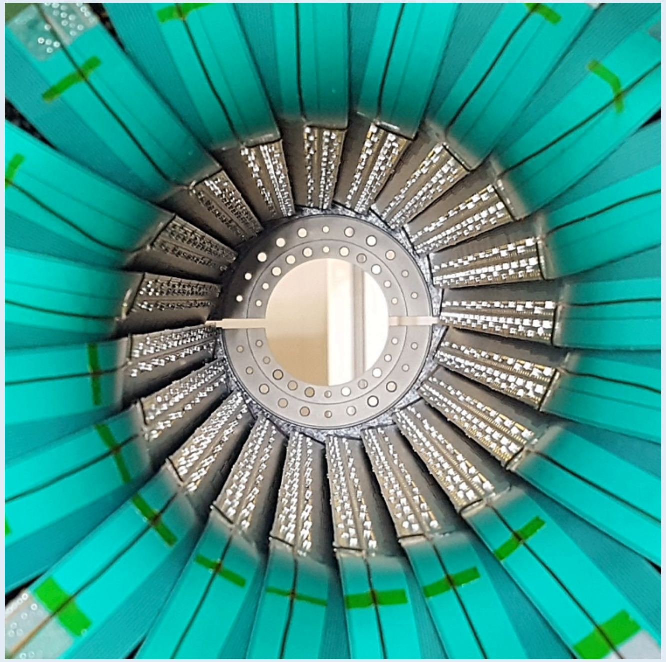
ITS2 layout



Inner barrel

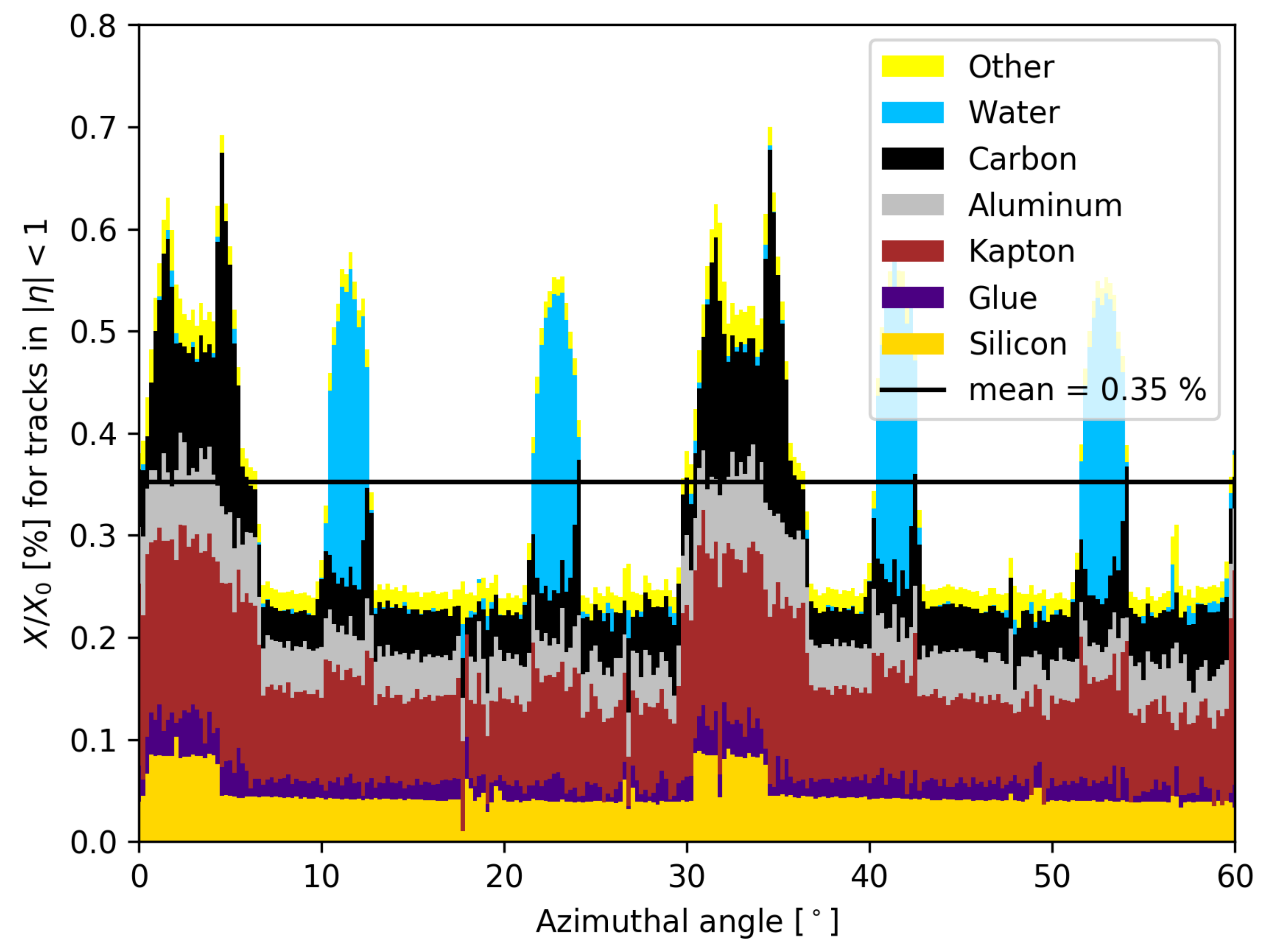


Layer 2 (20 staves)



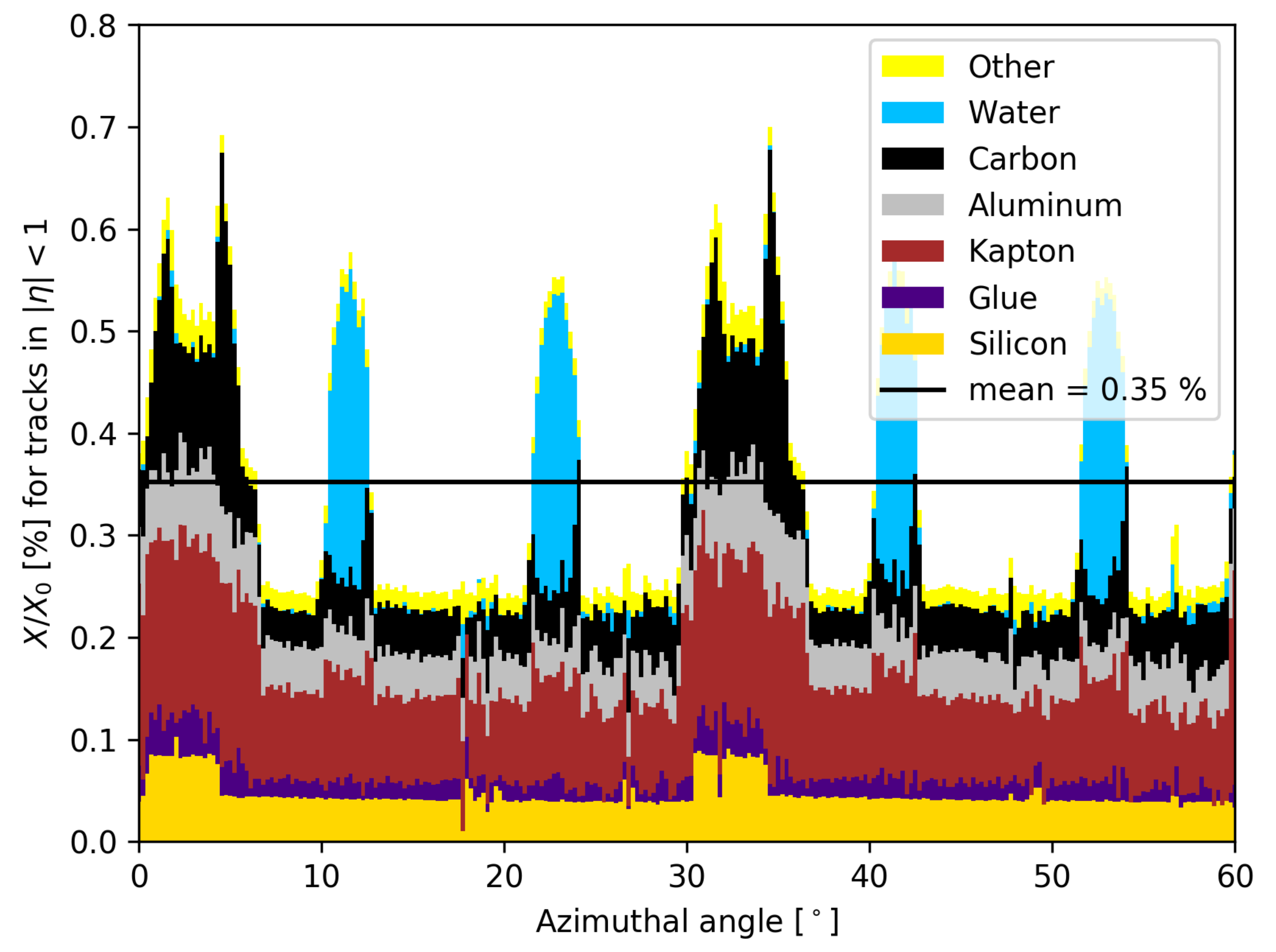
- Already very good performance estimates for ITS2
- Still, further improvements for the measurements of heavy-flavour hadrons and low-mass di-leptons possible
- **Key questions:**
  - ☞ **Can we get even lighter?**
  - ☞ **Can we get even closer?**

Material budget



- Si only 1/7th of total material
- Irregularities due to overlaps
  + support/cooling

Material budget



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Remove cooling

☞ reduce power consumption in fiducial volume <20 mW/cm^2

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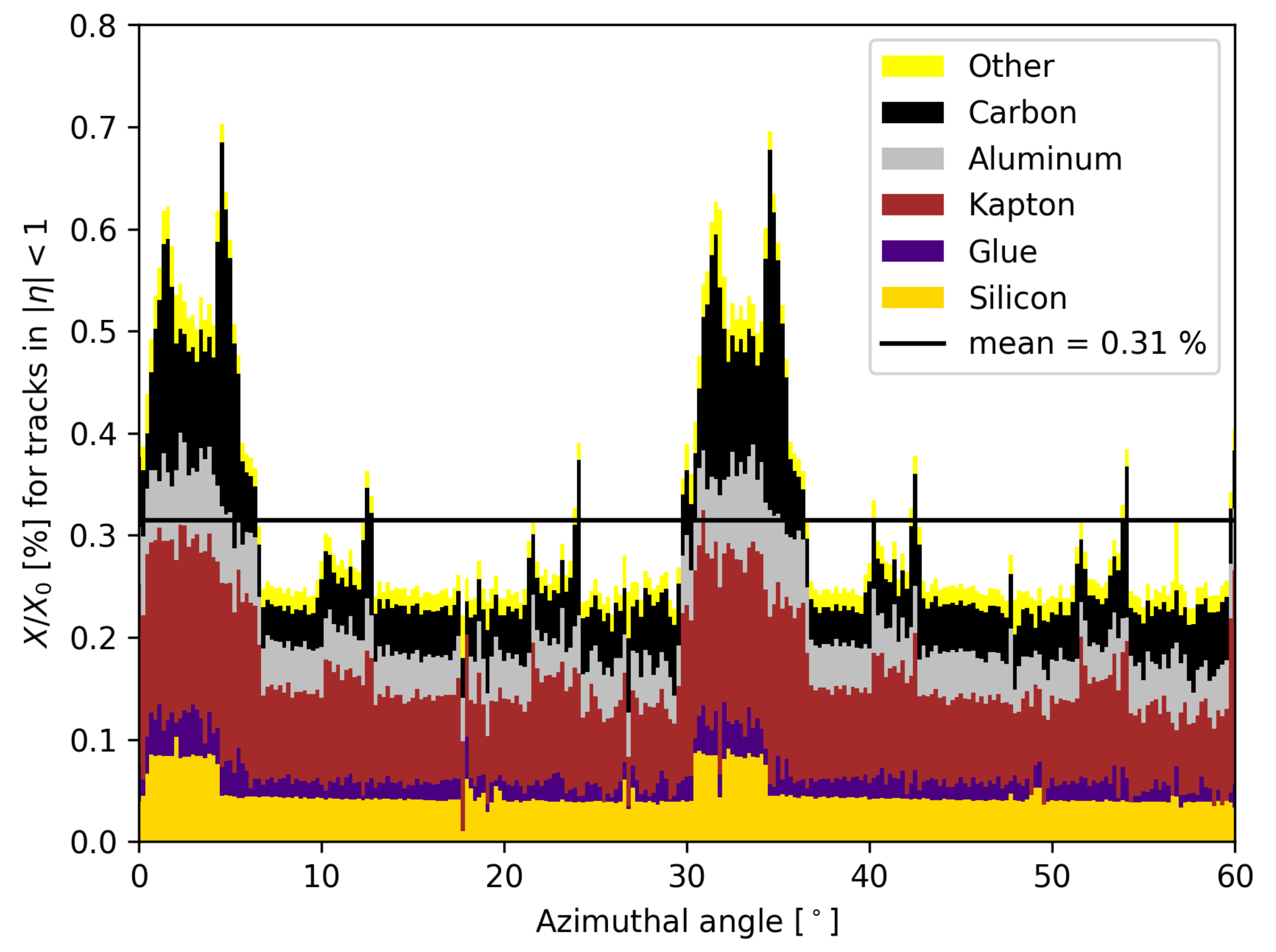

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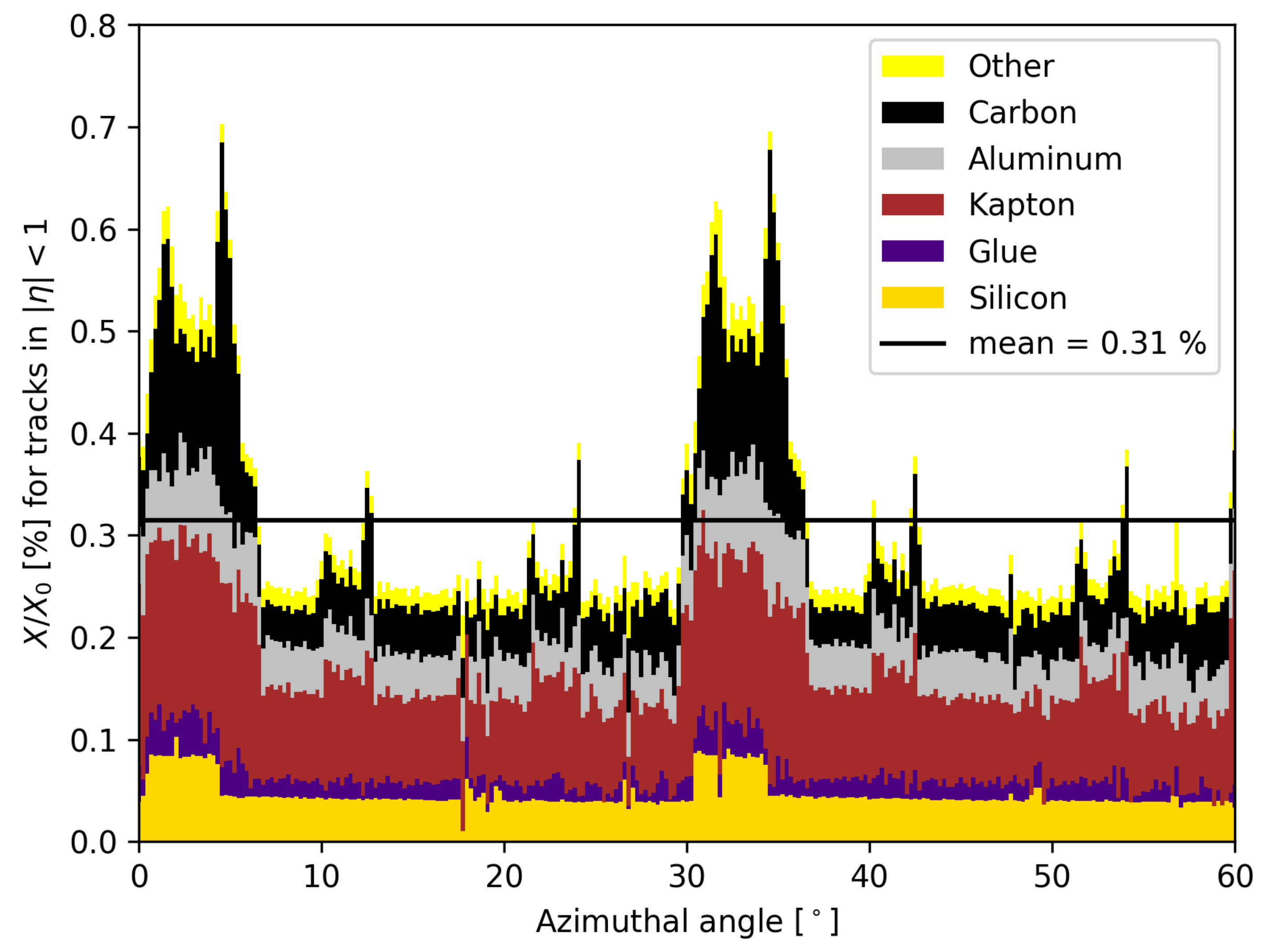

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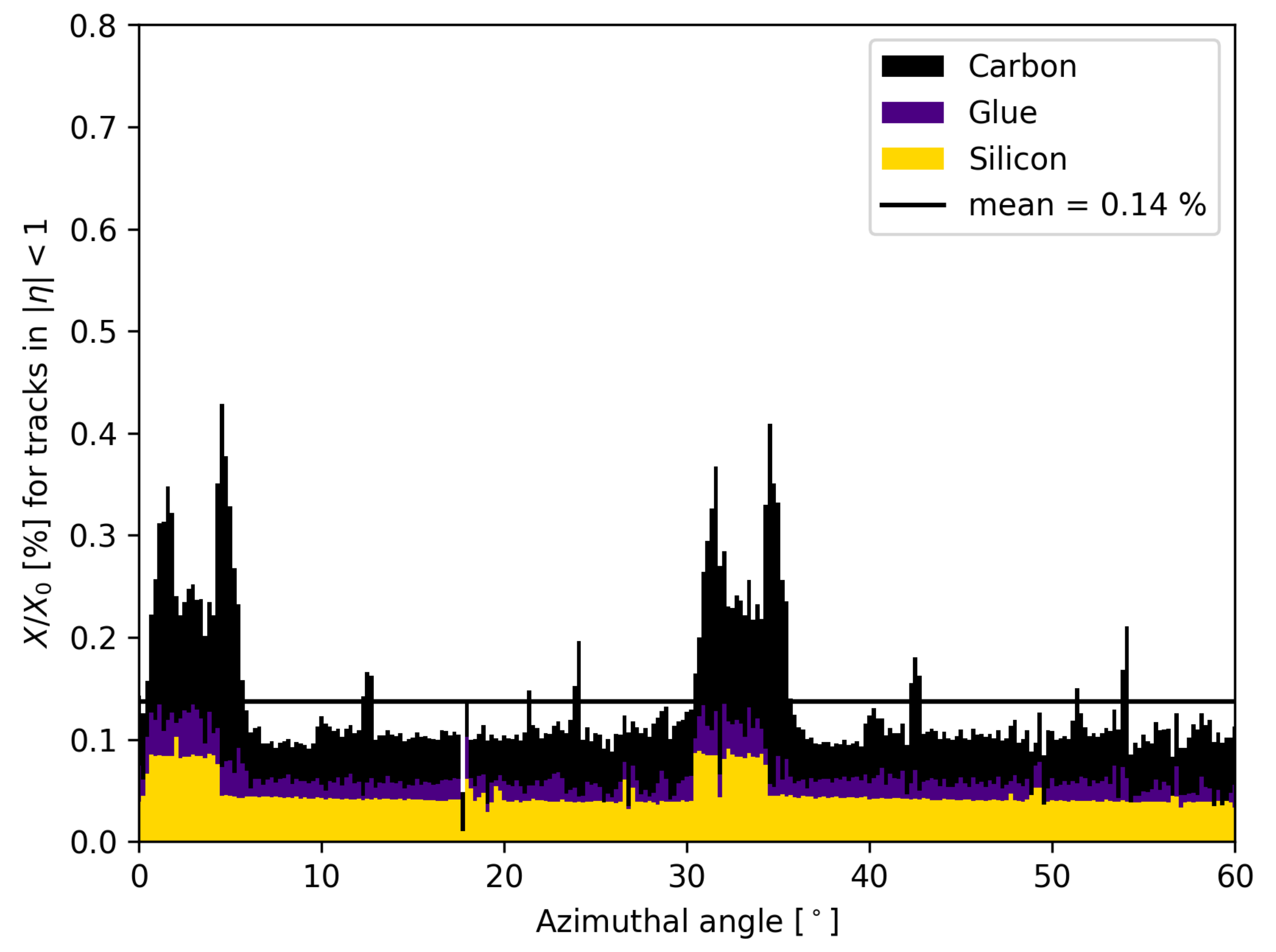
Remove external data lines + power distribution

☞ make a single large chips and use CMOS metal layers

Material budget



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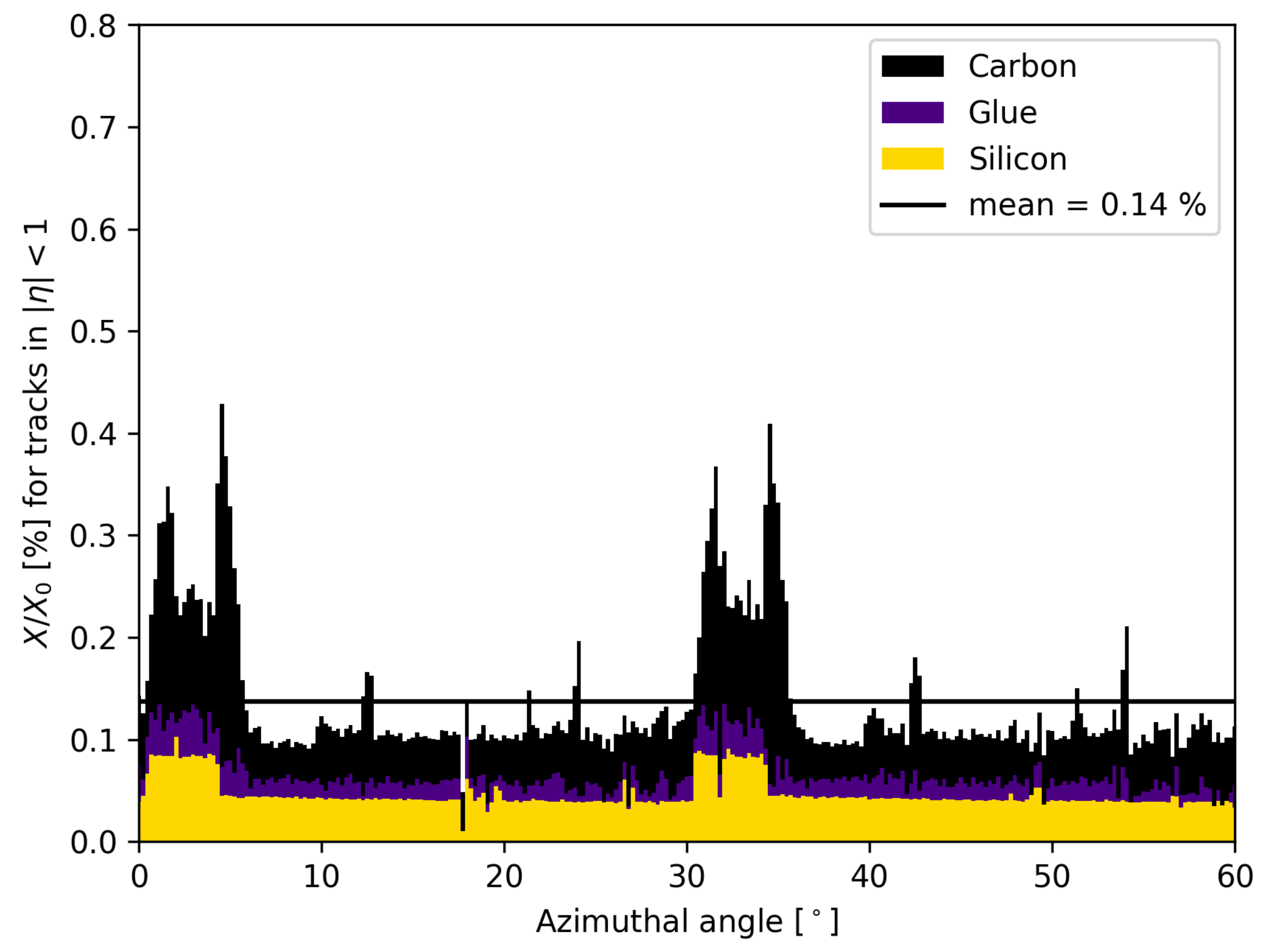

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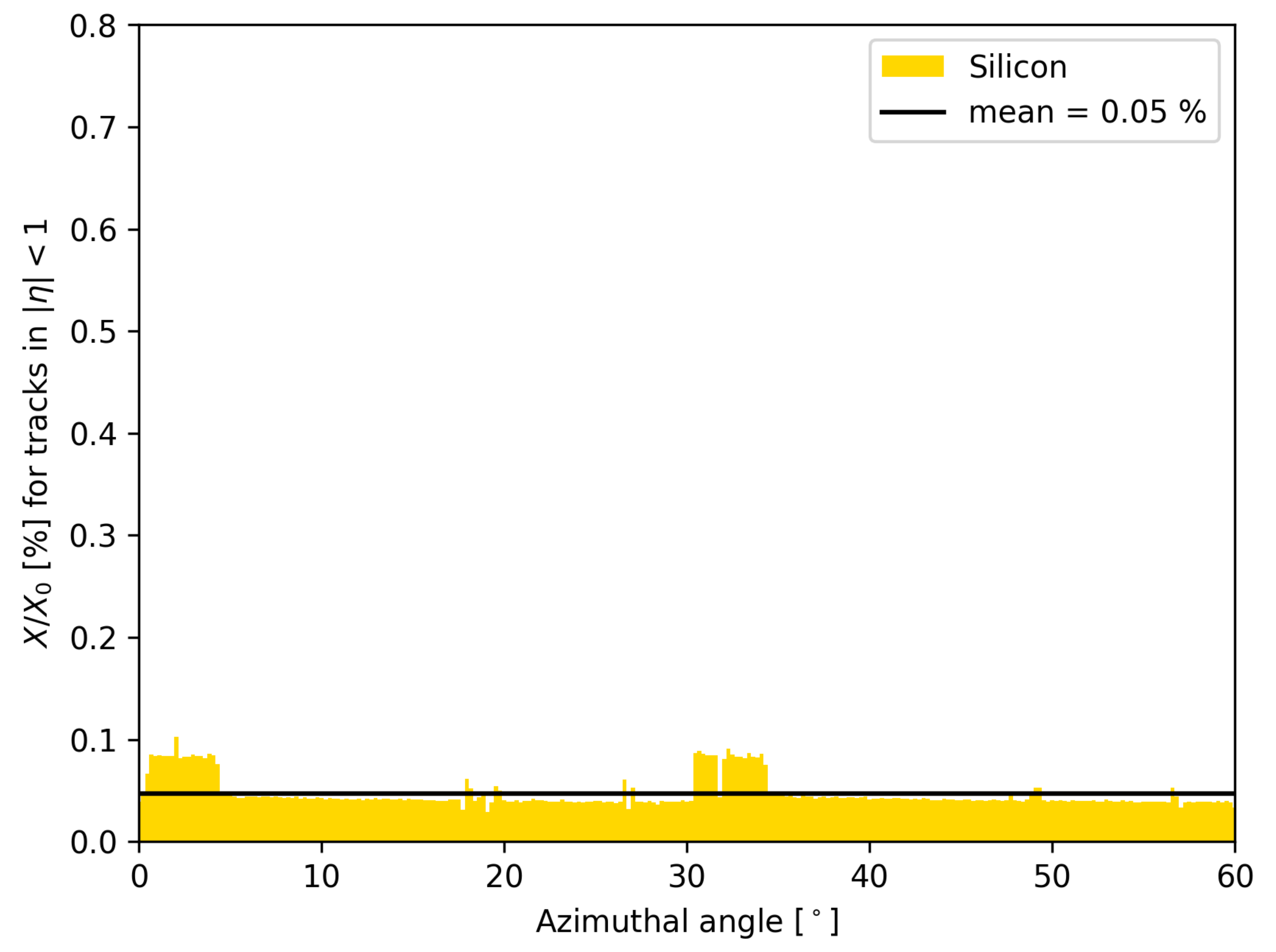
Move mechanical support outside acceptance

☞ benefit from increased stiffness by rolling Si wafers

Material budget



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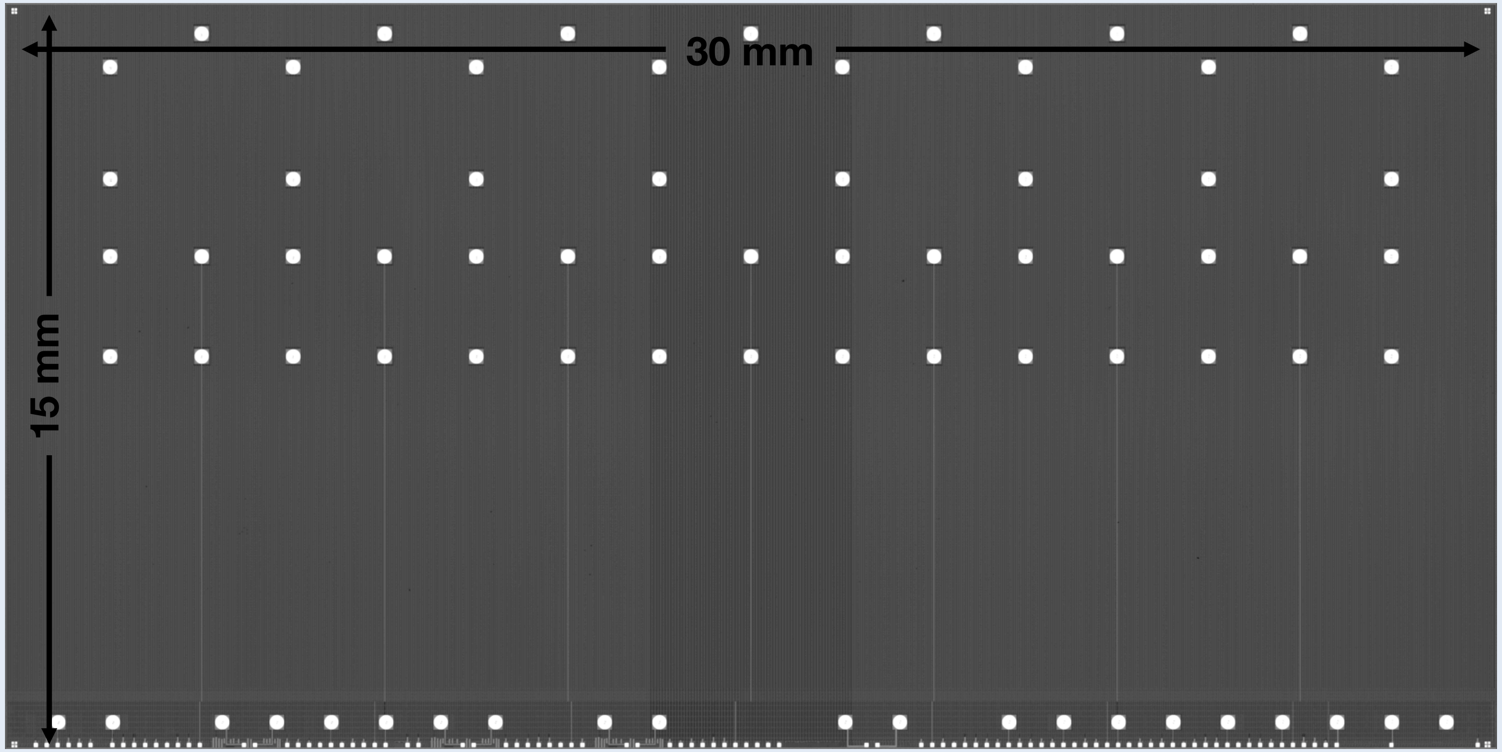
Air cooling

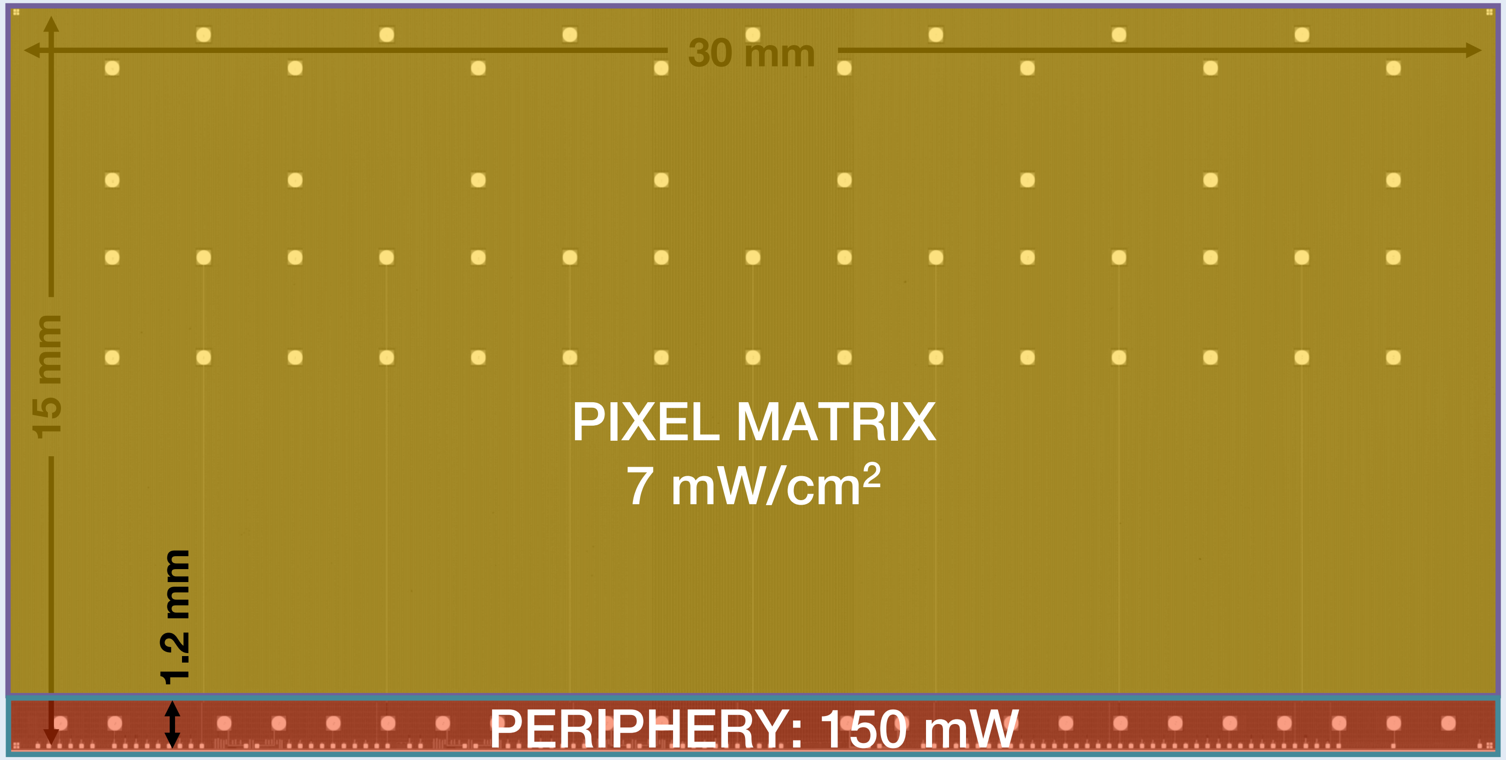
ALPIDE



- Air cooling possible as of ~20 mW/cm^2
  - ☞ ALPIDE already close: ~40 mW/cm^2

Air cooling

ALPIDE



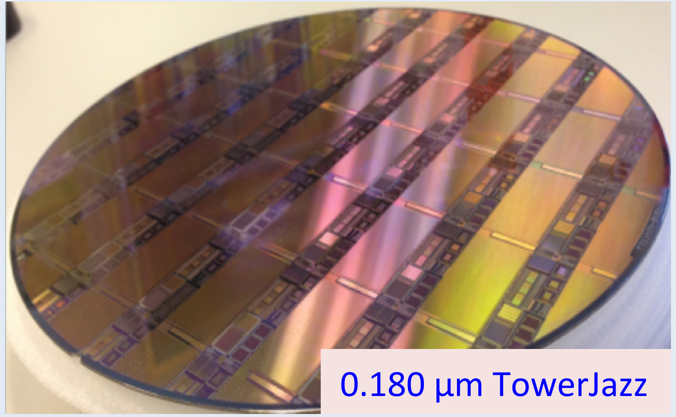
- Air cooling possible as of ~20 mW/cm^2
  - ☞ ALPIDE already close: ~40 mW/cm^2

Actually largely sufficient if periphery outside fiducial volume

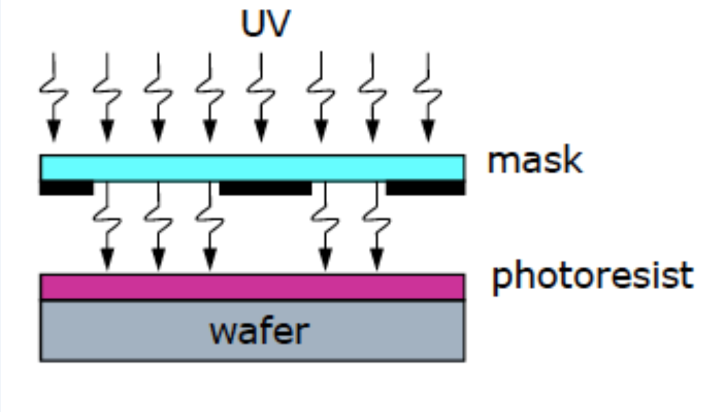
Wafer scale chip

- Chip size is traditionally limited by CMOS manufacturing ("reticle size")
- New option: stitching, i.e. aligned exposures of given parts of a reticle to produce a larger circuit
- Feasible, but needs specific design
- On a with 300 mm wafer (available in 65 nm technology node), a single chip fits **a full half-layer**

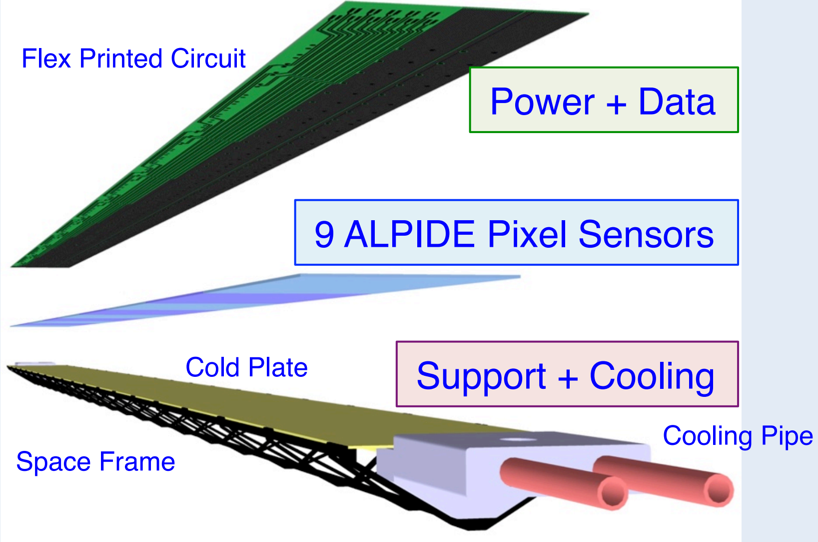
200 mm ALPIDE prototype wafer


0.180 µm TowerJazz

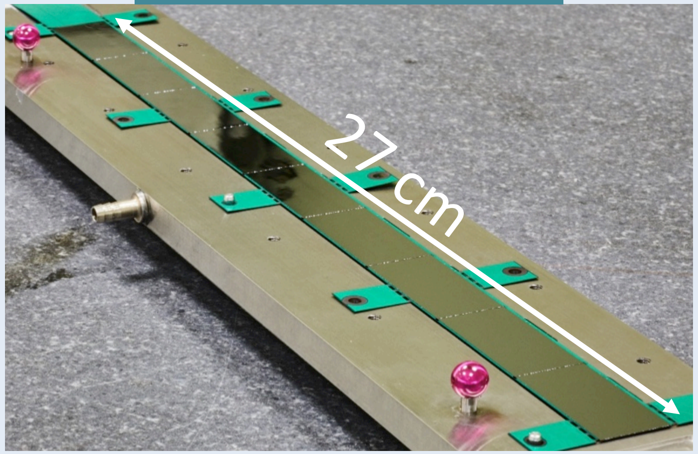
Principle of photolithogrphy



Stave Design

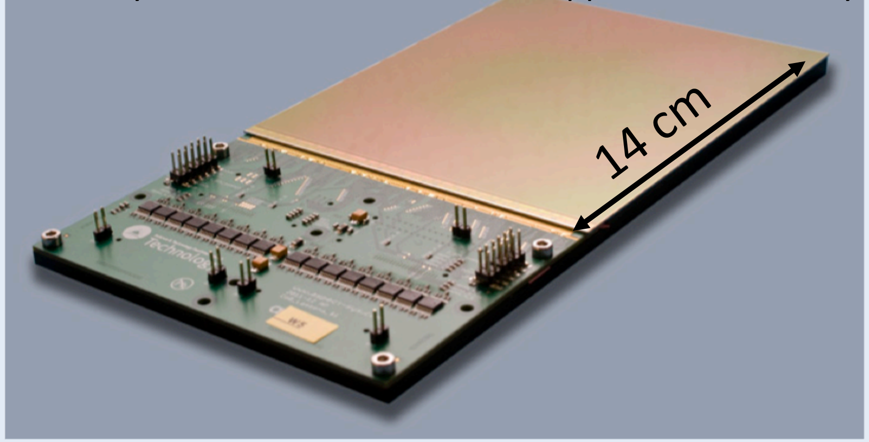


FPC + 9 ALPIDE chips



Wafer-scale sensor

Courtesy: R. Turchetta, Rutherford Appleton Laboratory

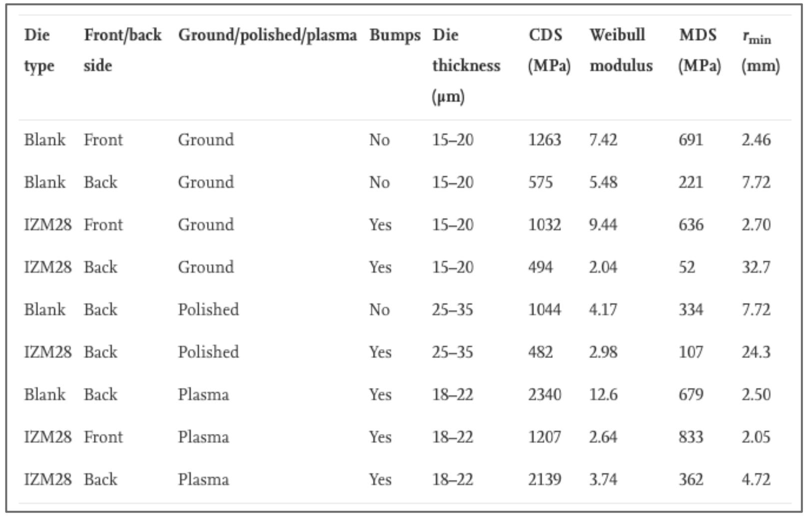


Bending silicon

- Bending Si wafers + circuits is possible!

D.A. van den Ende et al., Microelectronics Reliability, vol. 54, pp 2860-2870, 2014

http://dx.doi.org/10.1016/j.microrel.2014.07.125

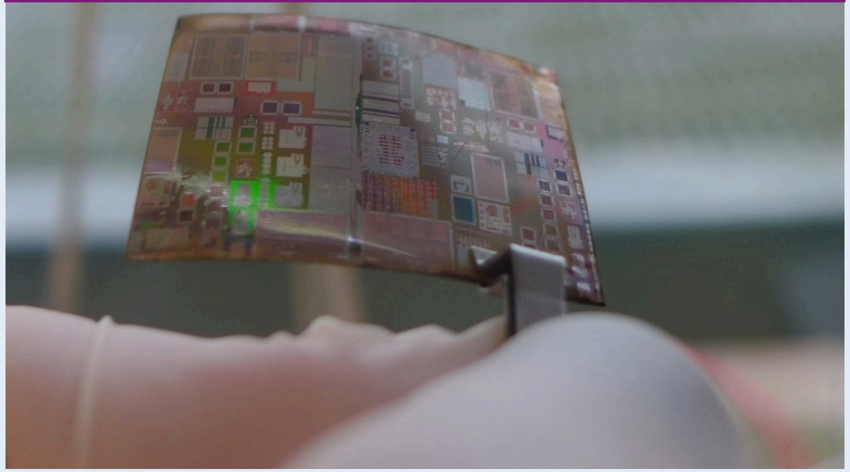


Die type	Front/back side	Ground/polished/plasma	Bumps	Die thickness (μm)	CDS (MPa)	Weibull modulus	MDS (MPa)	r_{min} (mm)
Blank	Front	Ground	No	15–20	1263	7.42	691	2.46
Blank	Back	Ground	No	15–20	575	5.48	221	7.72
IZM28	Front	Ground	Yes	15–20	1032	9.44	636	2.70
IZM28	Back	Ground	Yes	15–20	494	2.04	52	32.7
Blank	Back	Polished	No	25–35	1044	4.17	334	7.72
IZM28	Back	Polished	Yes	25–35	482	2.98	107	24.3
Blank	Back	Plasma	Yes	18–22	2340	12.6	679	2.50
IZM28	Front	Plasma	Yes	18–22	1207	2.64	833	2.05
IZM28	Back	Plasma	Yes	18–22	2139	3.74	362	4.72

- Radii much smaller than our needs are obtained
- Circuit-specific R&D is needed
- R&D contacts with industrial partners have started
- Investigating options to start with existing ALPIDE chips + wafers

Silicon Genesis: 20 micron thick wafer

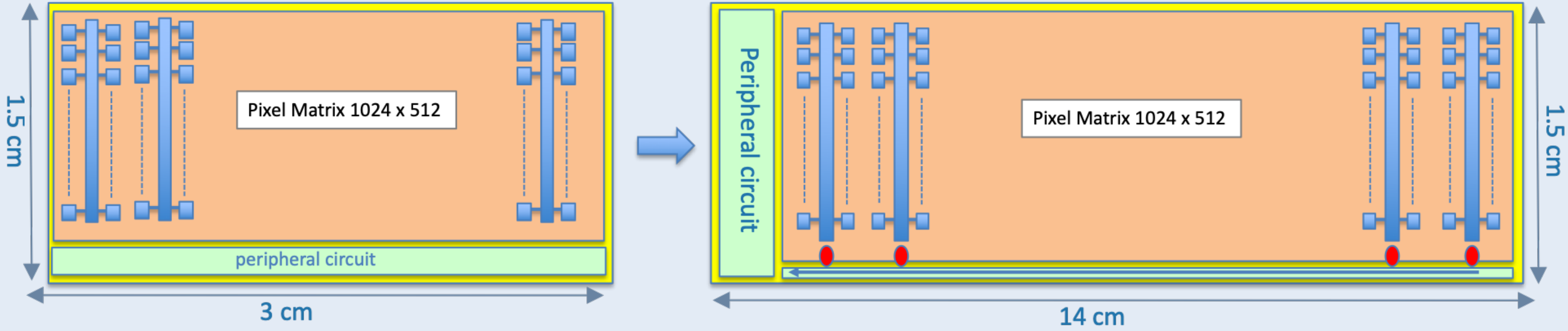
Chipworks: 30μm-thick RF-SOI CMOS



Possible architecture

ALPIDE Chip

1D stitched sensor (z direction)



2D stitched sensor – wafer-scale

By instantiating multiple times the same circuits in the second dimension (ϕ) one can realize the sensors for the different layers. For example

- L0 = 14 cm x 6.0 cm
- L1 = 14 cm x 7.5 cm
- L2 = 14 cm x 9.0 cm

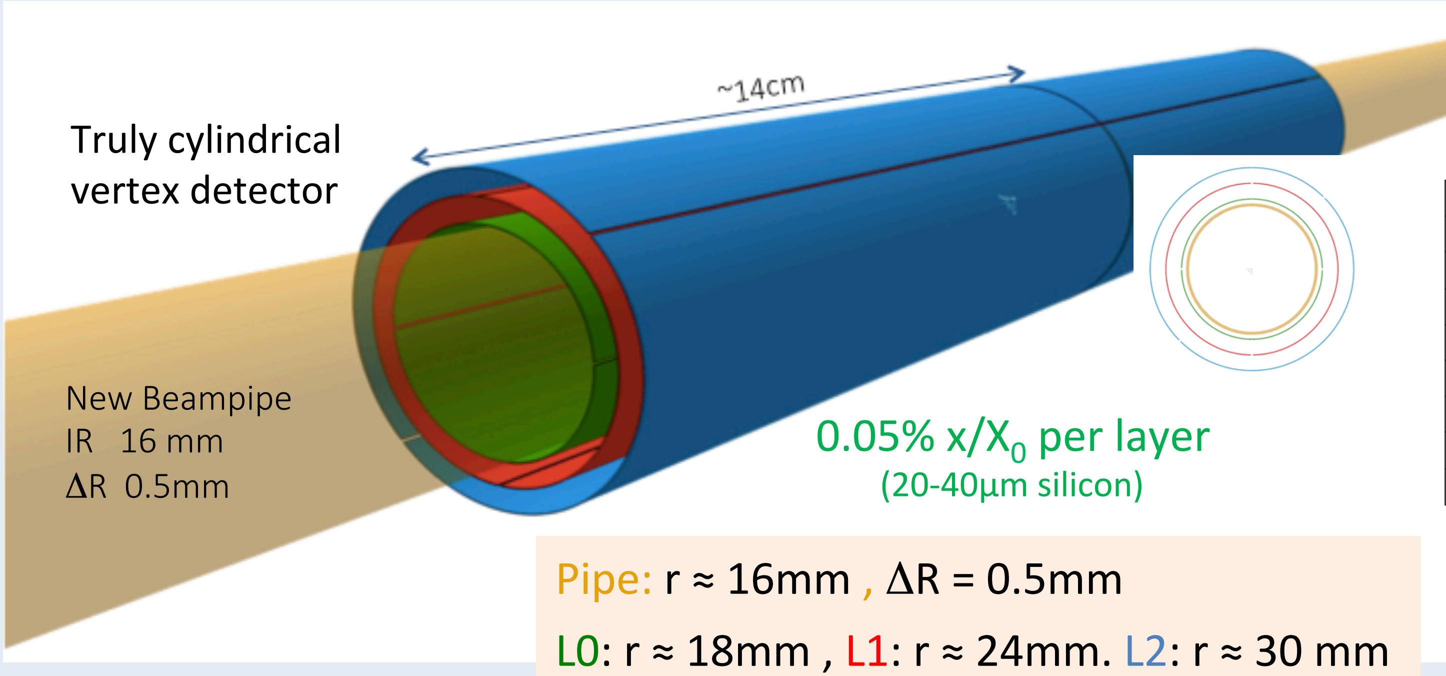
☞ achievable with wafers available in 180 nm technology node (ALPIDE technology)

Vertex Detector (innermost 3 layers) for LS3 Upgrade

EoI for new ultra-light Inner Barrel in LS3 (CDS, ALICE-PUBLIC-2018-013)

Recent silicon technologies (ultra-thin wafer-scale sensors) allow

- Eliminate active cooling ➪ possible for power < 20mW/cm^2
- Eliminate electrical substrate ➪ Possible if sensor covers the full stave length
- Sensors arranged with a perfectly cylindrical shape ➪ sensors thinned to ~30μm can be curved to a radius of 10-20mm



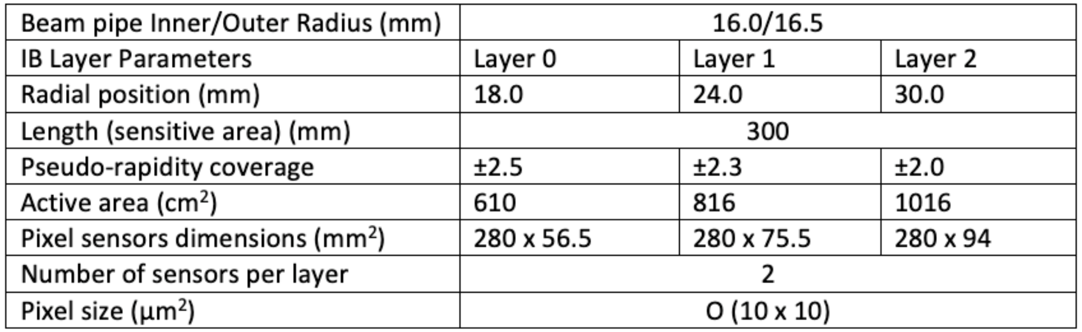
Truly cylindrical vertex detector

New Beampipe
IR 16 mm
ΔR 0.5mm

0.05% x/X_0 per layer
(20-40μm silicon)

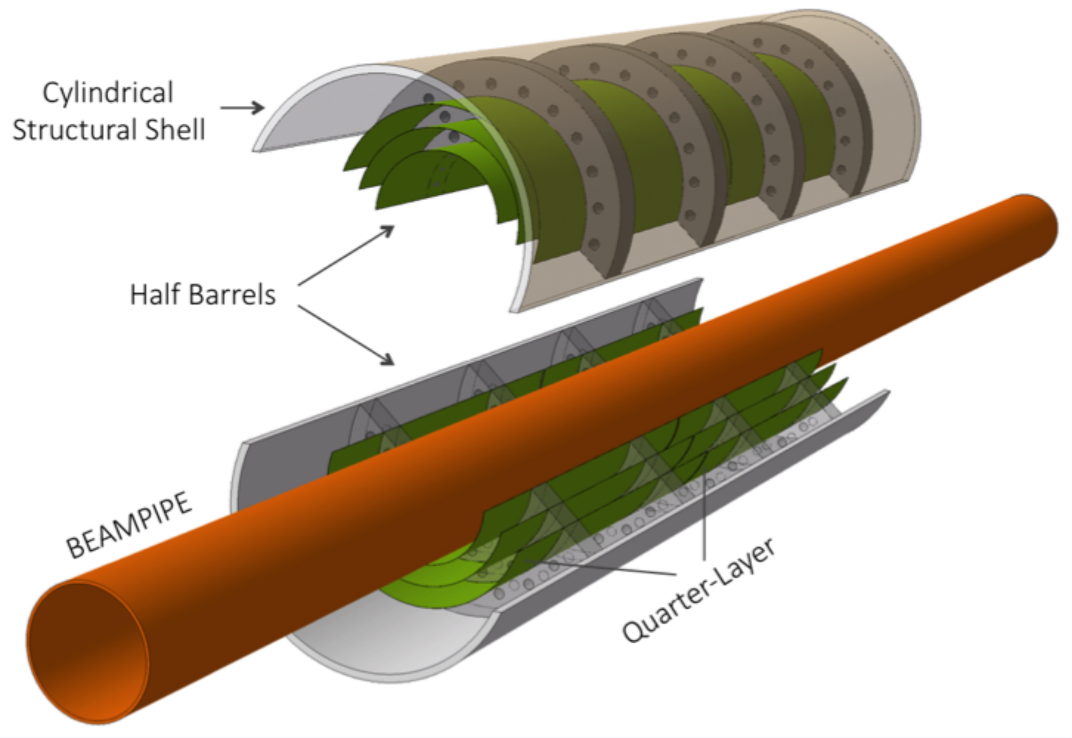
Pipe: r ≈ 16mm , ΔR = 0.5mm

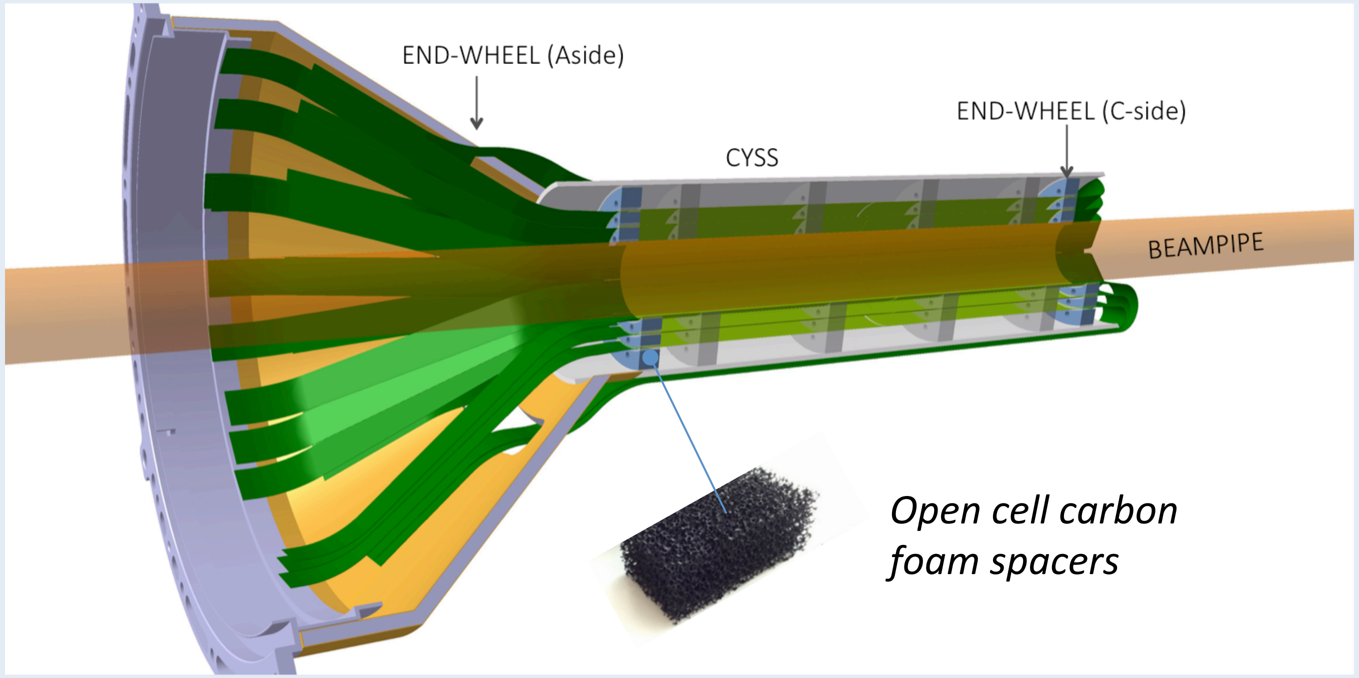
L0: r ≈ 18mm , L1: r ≈ 24mm. L2: r ≈ 30 mm



Beam pipe Inner/Outer Radius (mm)	16.0/16.5		
IB Layer Parameters	Layer 0	Layer 1	Layer 2
Radial position (mm)	18.0	24.0	30.0
Length (sensitive area) (mm)	300		
Pseudo-rapidity coverage	±2.5	±2.3	±2.0
Active area (cm^2)	610	816	1016
Pixel sensors dimensions (mm^2)	280 x 56.5	280 x 75.5	280 x 94
Number of sensors per layer	2		
Pixel size (μm^2)	O (10 x 10)		

Vertex Detector (innermost 3 layers) for LS3 Upgrade

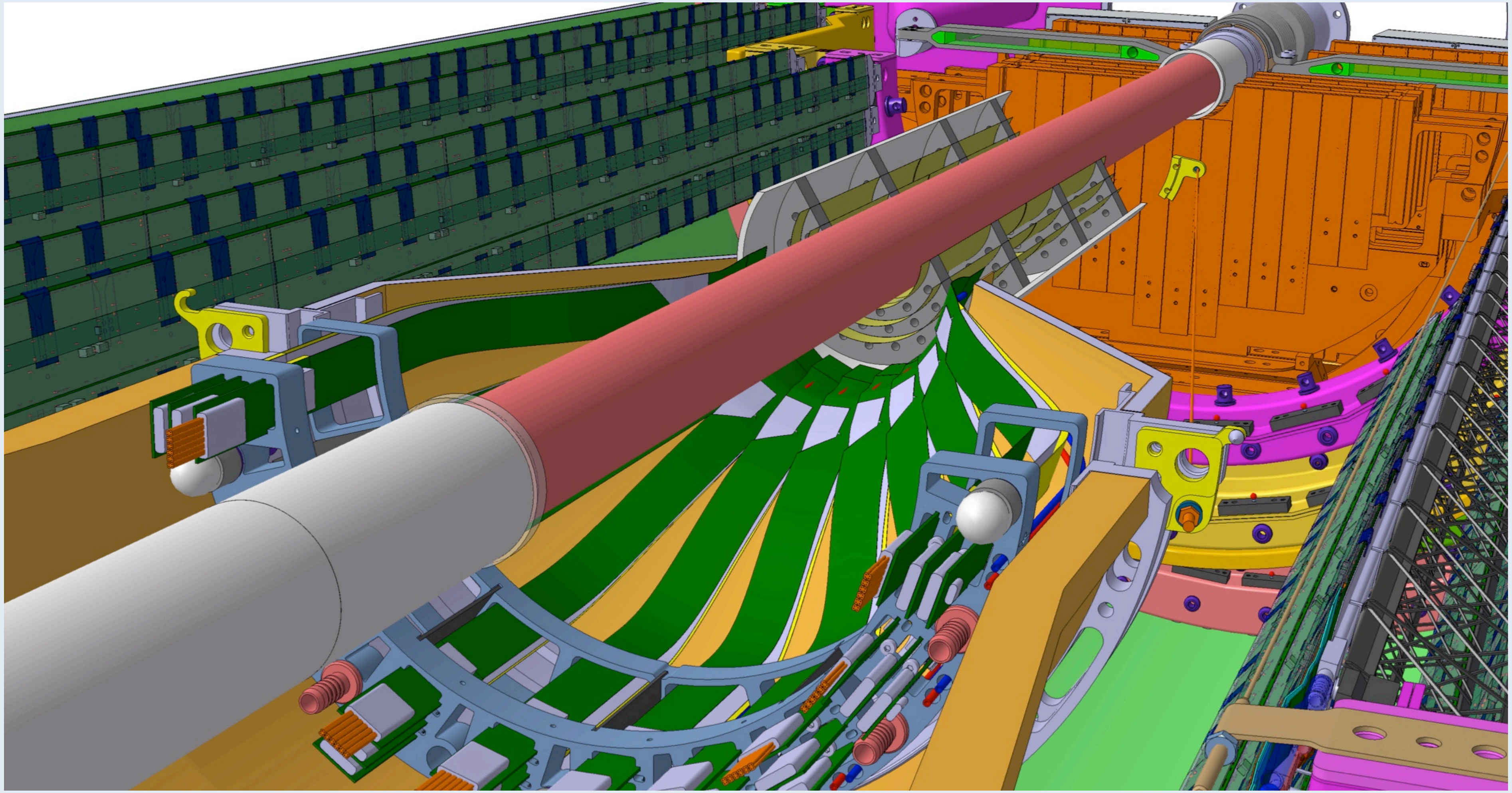




- Possible layout based on air-cooling

  additional cooling at the extremities (chip peripheries)
- Sensors hold in place with low-density carbon foam
- Fixation into the experiment by surrounding support structure, as well as at both ends

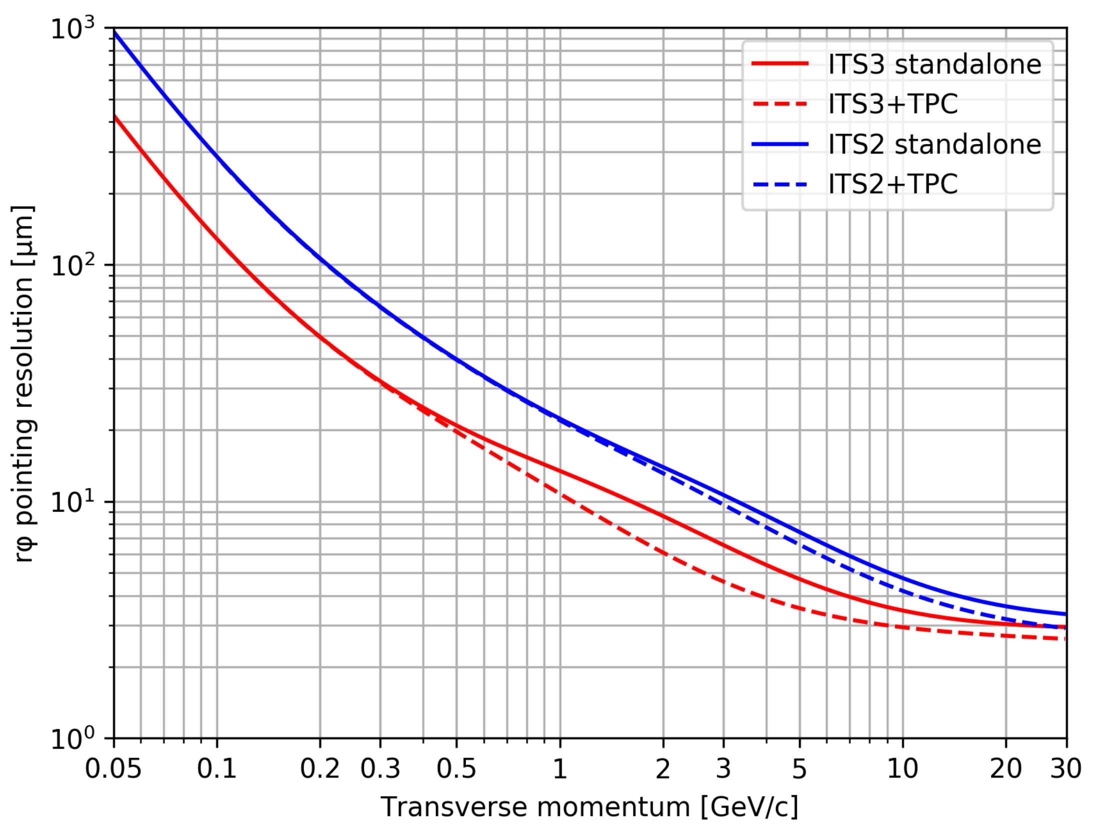
ITS3 Integration



- ☞ Simply replace the Inner Barrel of ITS2
- ☞ Outer Barrel of ITS2 stays in place as is

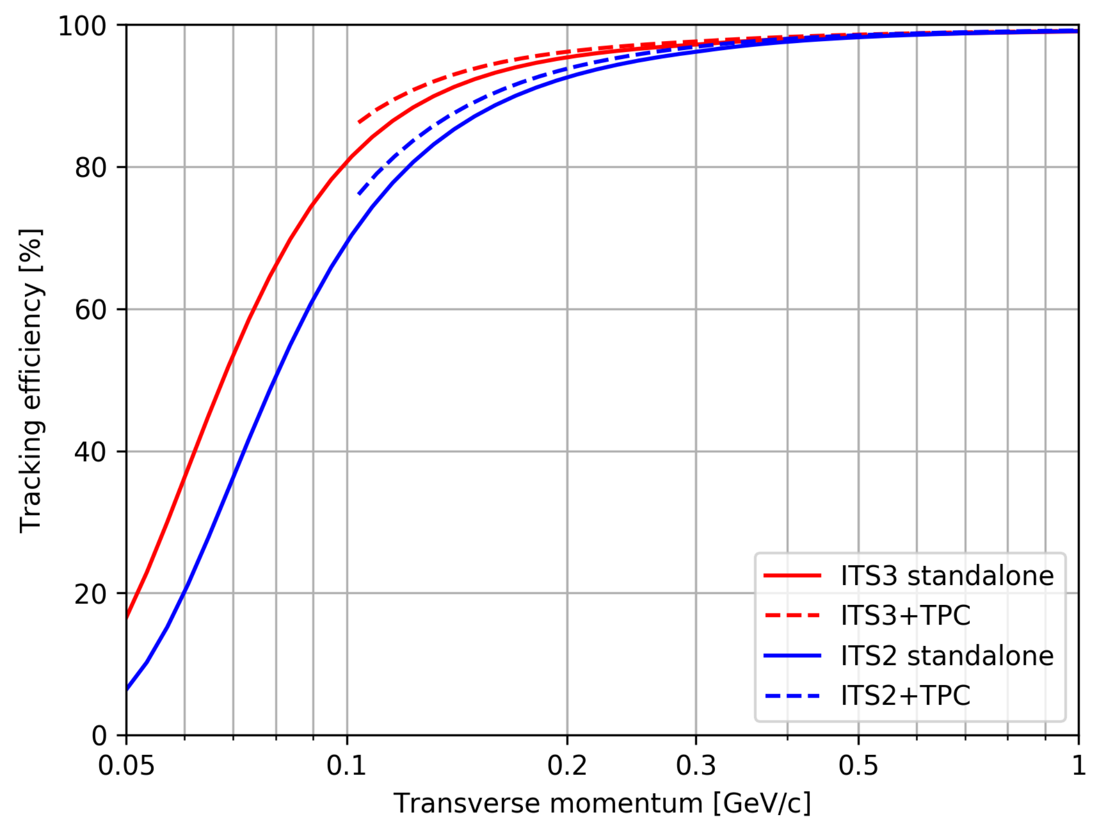
ITS3 perfomance studies

Pointing resolution



Improvement of factor 2 over all momenta

Tracking efficiency



Large improvement for low transverse momenta

Roadmap towards ITS3

R&D 2020-2023

Wafer thinning + bending

- 2019 → Contact to industry
- 2019-2020 → First prototypes with ALPIDE chips and wafers
- 2021 on → Continue with specific prototypes

Stitched sensor development

- 2019-2020 → Technology test structures
- 2020-2022 → Prototyping chips
- 2022-2023 → Full-scale prototype + final chip

Technical Design Report 2022

Construction 2024-2025

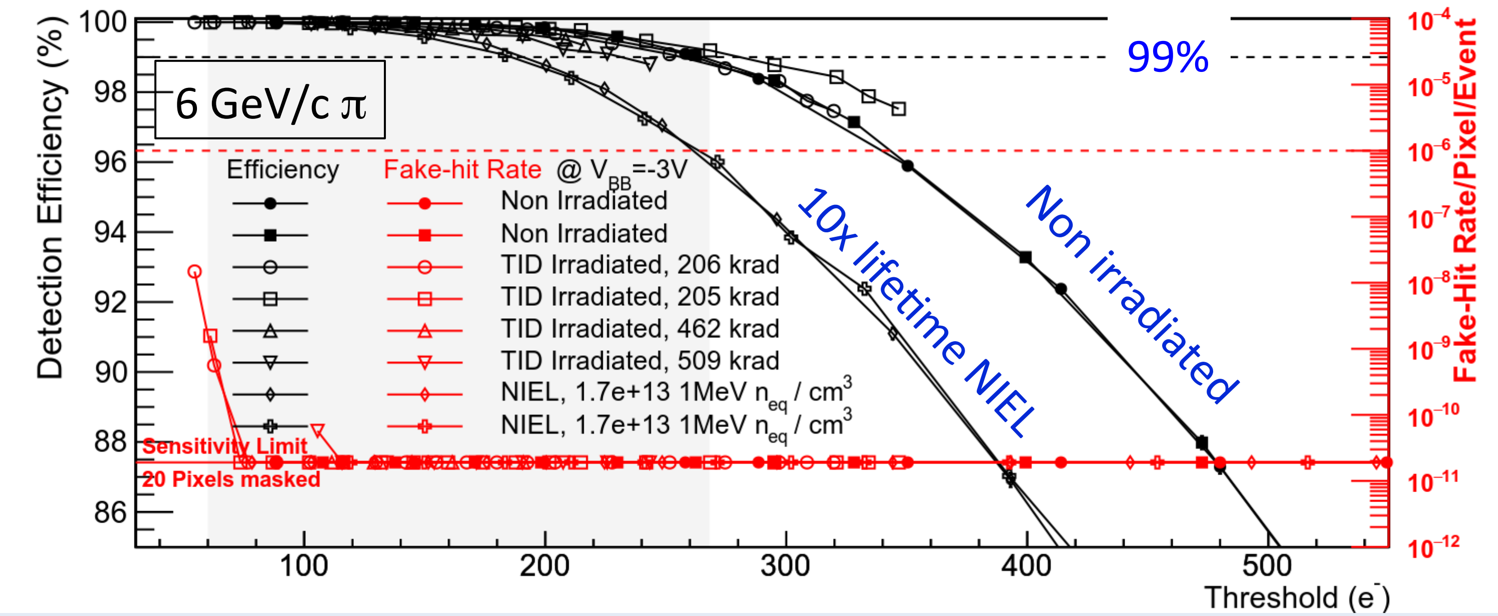
Installation during LS3

Summary

- With the ITS2 upgrade and ALPIDE, ALICE redefined the new state-of-the art in CMOS MAPS technology and its applications in HEP
- The used technology offers further opportunities, stitching, smaller feature size, bending that directly impact the key measurements that highly rely on precise vertexing and low material budget
- A detector conceived for studies of pp, pA and AA collisions at luminosities 50 times higher than possible with the LS2 upgraded ALICE detector
  - Enables rich physics program: from measurements with electromagnetic probes at ultra-low transverse momenta to precision physics in the charm and beauty sector
  - Tracking and vertexing capabilities over a wide momentum range down to a few tens of MeV/c
  - Particle ID via time-of-flight determination with about 20ps resolution. Electron and photon ID identification will be performed in a separate pixel shower detector
  - Unprecedented low material budget for the inner layers of 0.05% X_0, with the innermost layers possibly positioned inside the beam pipe
- ALICE LS3 upgrade: three truly cylindrical inner barrel based on curved wafer-scale ultra-thin CMOS Active Pixel sensors

Thank You

ITS Upgrade in LS2 (ITS2)

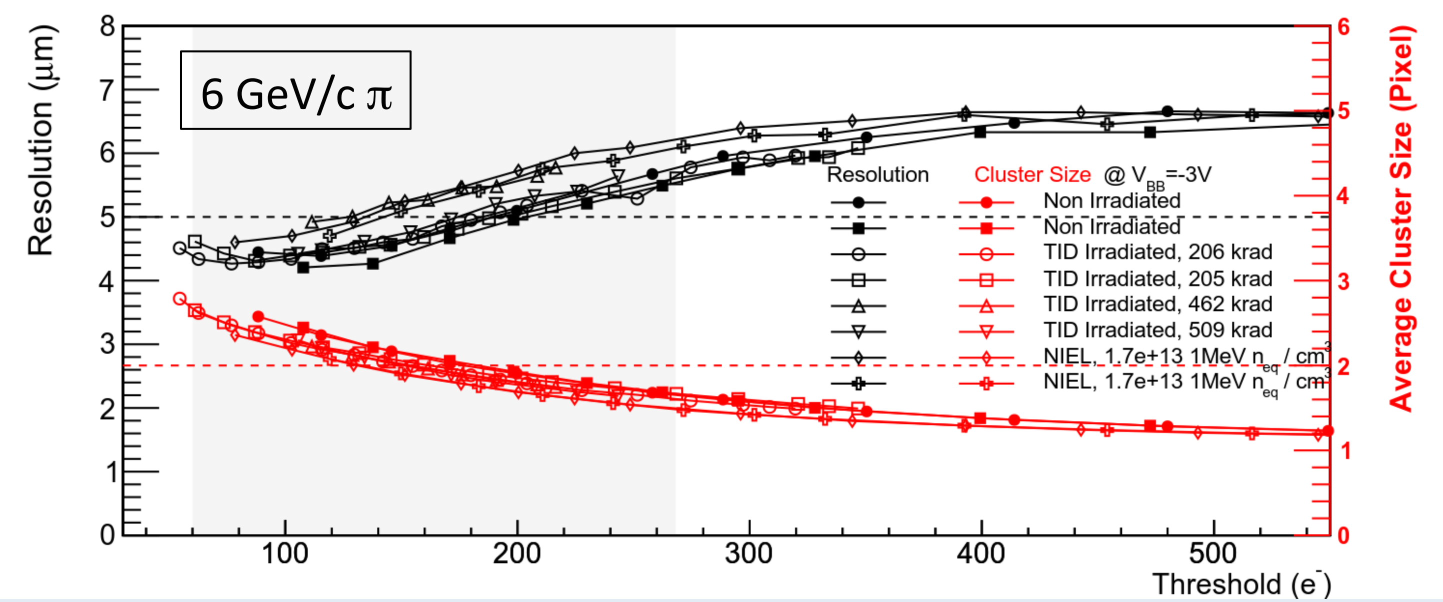


Nucl. Phys. A 967 (2017) 900-903

Large operational margin with only 10 masked pixels (0.002%), fake-hit rate < 2 x 10^{-11} pixel/event

Non irradiated and TID/NIEL chips similar performance

Nucl. Phys. A 967 (2017) 900-903

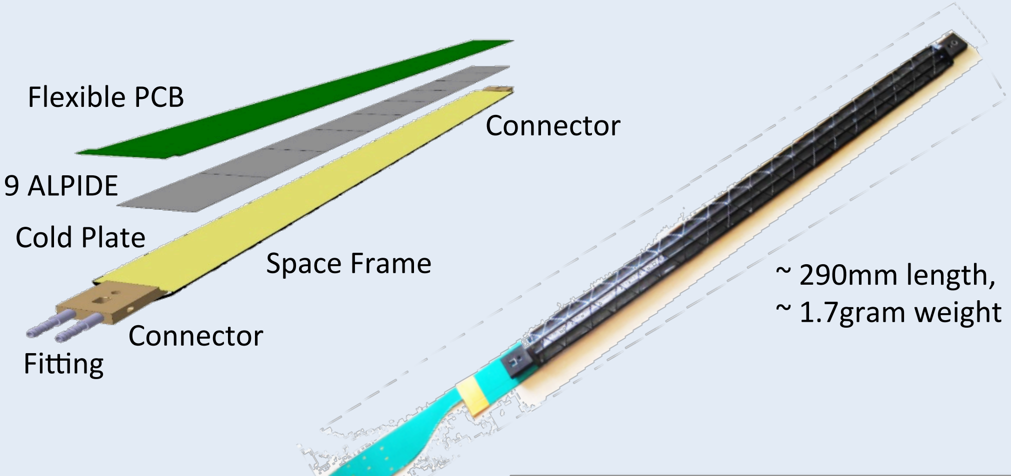


5 μm resolution @200 e⁻ threshold

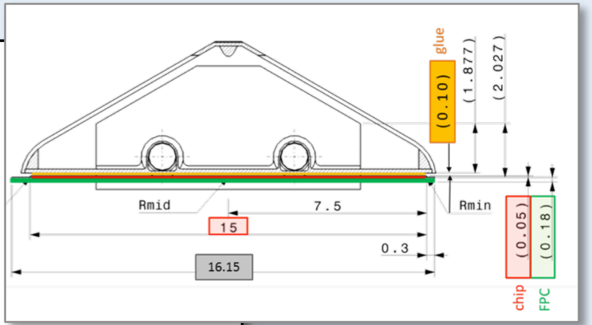
Chip-to-chip negligible fluctuations

ITS Upgrade in LS2 (ITS2)

Inner Barrel Stave



~ 290mm length,
~ 1.7gram weight

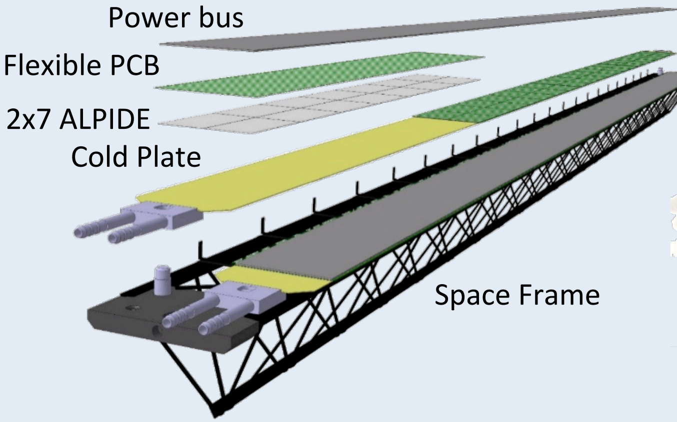


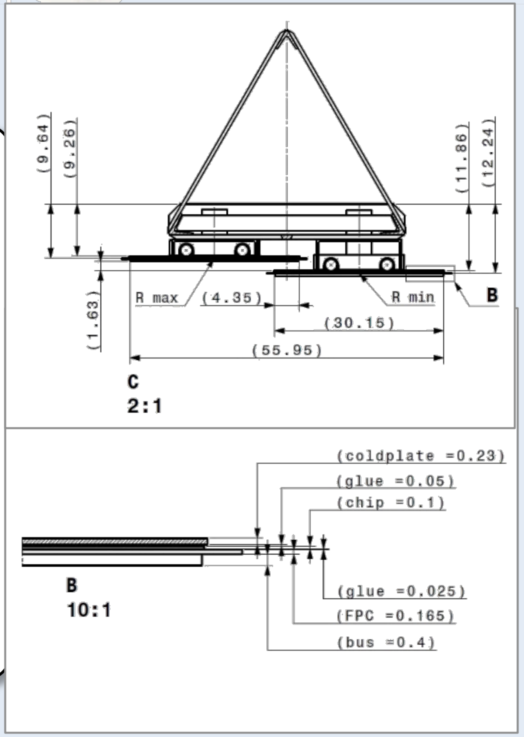
Radius (mm) 23, 31, 39
Nr. Staves: 12, 16, 20
Nr. Chips/ layer: 108, 144, 180

Length in z (mm): 271.2 mm
Nr. chips/ Stave: 9
Material thickness:~0,3% X_0

Coolant Single-phase H_2O leak-less
Pixel operational temperature < 30°C
Pixel max temperature non-uniformity < 5°C
Chip Power dissipation < 50mW/cm^2

Outer Barrel Stave



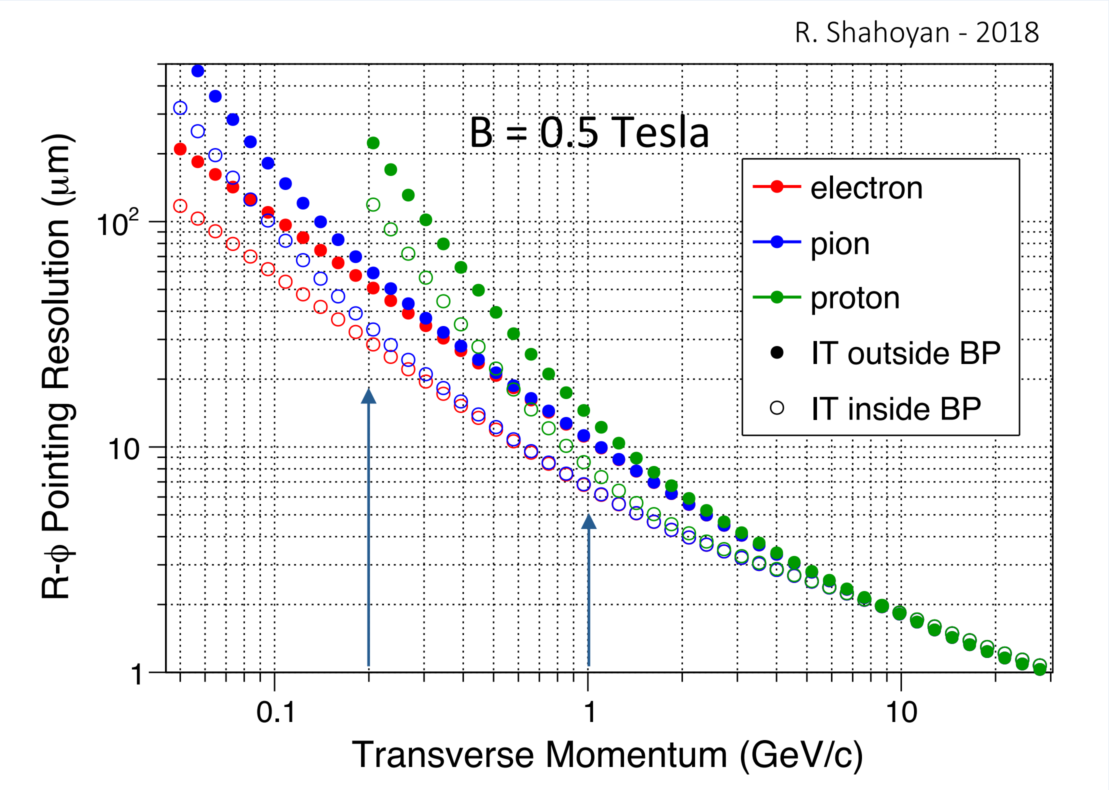


Radius (mm)196, 245.4, 343.8, 393.3
Nr. Staves: 24,30,42,48
Nr. Chips/ module:2x7

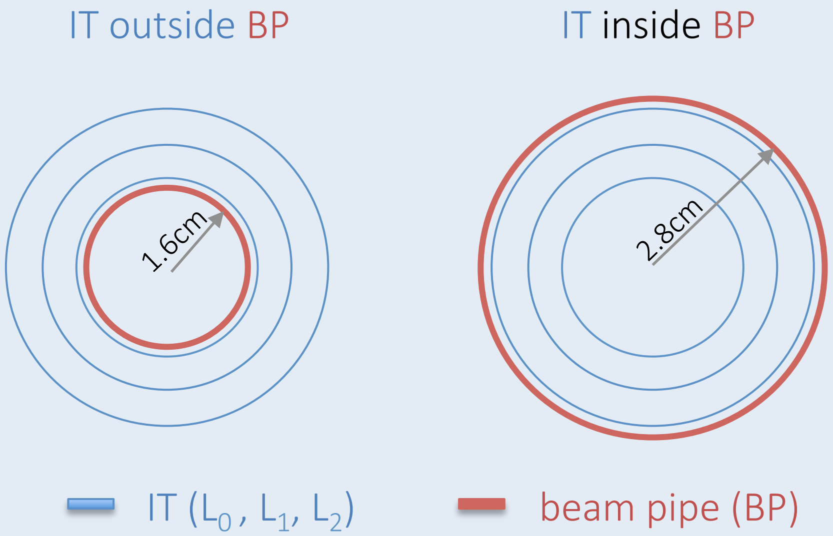
Length in z (mm): 844.2 (ML), 1477.5 mm (OL)
Nr. module/ Stave: 4 (ML), 7(OL)
Material thickness:~1% X0

Coolant Single-phase H_2O leak-less
Pixel operational temperature < 30°C
Pixel max temperature non-uniformity < 5°C
Chip Power dissipation < 40mW/cm^2

Pointing resolution



R. Shahoyan - 2018



Pointing resolution (pions): ≈ 10 μm @ 1 GeV/*c*, <50μm @ 200 MeV/c

It does not depend on B field