HGTD
Altiroc2 Digital

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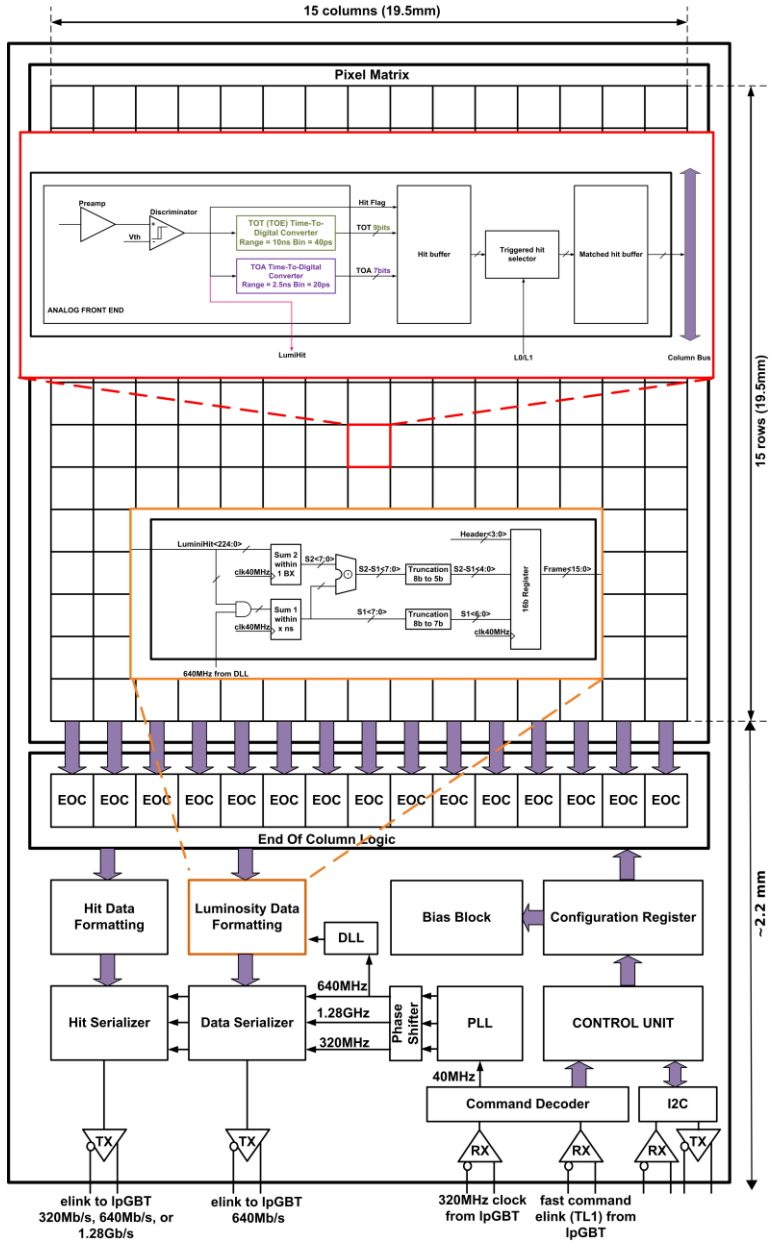
Altiroc2 Chip



Characteristics

- Developped in TSMC 130nm
- Matrix of pixels : 15x15
- Measure of TOA, TOT, luminosity
- Pixel size : 1,3x1,3 mm² => chip size ~2cm x 2cm
- Pixel block : (PreAmp + Discri + 2 TDC + SRAM) + digital block
- Off-pixel modules

Constraints

- High constraint in terms of radiations (500Mrad)
- Skew <100 ps on all the pixels of the matrix
- Timing windows of 3ns to be distributed to all the pixels

Digital On Top flow

DOT Bottom-up Approach

- Synthesis of the RTL sources of the block (for digital blocks)
- Layout of each block independently
- Characterization of the blocks (Timing, pin capacitance)
- Floorplan (Placement of each block)
- Power routing
- Clock Tree Synthesis
- Signal routing
- Checks (DRC, Timing, IR drop, . . .)

Characterization

Characterization step generates a file containing accurate information on the timing and the pin capacitance

For a **digital** block

- The liberty file is generated using a specific command once the block has been layouted and checked

For an **analog** block

- The liberty file is generated using the **Liberate AMS** tool
- This tool is new to us so we need to look into it

All the liberty files are then given to the digital tool so it can achieve the best timing performance

Clock Tree Synthesis

Flow for Altiroc2

- Layout + characterization of one pixel
- Layout of the 15 pixels column + **CTS**
- Layout of the matrix + **CTS**
- Peripheral blocks

Clock Tree Synthesis (CCopt)

- 40 MHz clock distributed over the 15 pixels column