Micro numérique @ IPNL

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Outline

- Technical skill @ IPNL
- Case Study: CIC1 ASIC
- CIC1 physical design
- CIC1 digital flow implementation
  - Synthesis
  - PnR
  - Signoff
- Conclusion

Technical skills @ IPNL

- ***RTL coding in System Verilog language and simulation with ad-hoc testbench***
  - Model writing in System Verilog language
  - Testbench implementation in System Verilog and Python language
  - Simulations using ncsim and Simvision tools
- ***Synthesis (Genus tool):***
  - Multiple clock domains management → writing of SDC constraints; skill limited to data not crossing different clock domains
  - Multiple power domains management → skill not used at this stage
  - Hierarchical synthesis → a preliminary and tentative hierarchical flow has been written but not implemented in the final submission
  - Design for Test (DFT) type SCAN path → introduces complexity at the timing analysis level (not implemented)
  - Low Power → clock gating techniques and utilisation of low-power std cells families (not implemented)
  - Formal verification → Conformal LEC scripts and analysis of the comparison results
  - Mixed environment → black-box (analogue macro) implementation at synthesis level

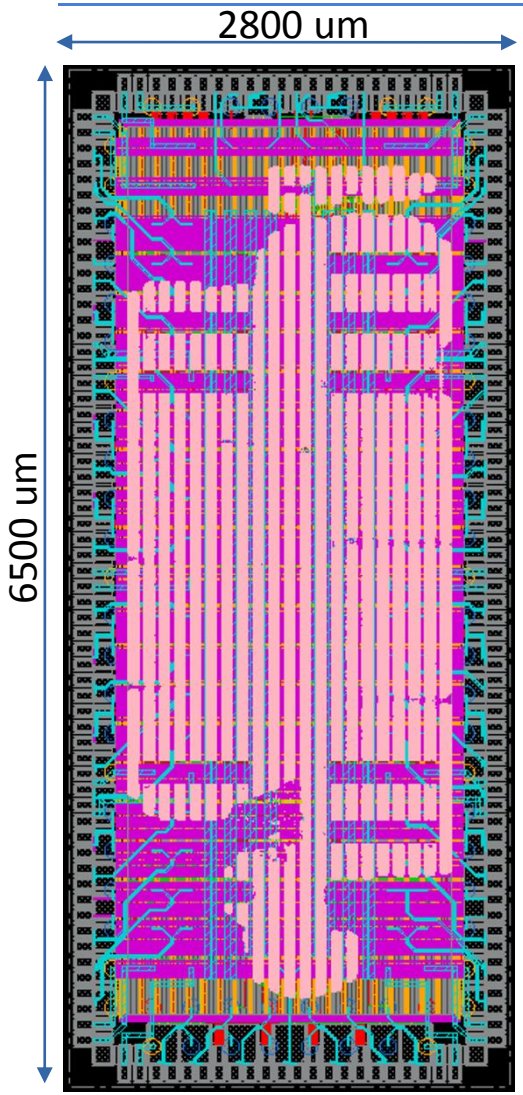
Technical skills @ IPNL

- ***Placement and routing (Innovus tool)***
  - Multiple clock domains management → writing of SDC and CTS-specific constraints
  - Multiple power domains management → implemented in our project
  - Design for Manufacturing (DFM) → already implemented at the flow level (CERN scripts)
  - Power analysis using Voltus tool → static and dynamic analysis; IR drop analysis
  - Formal verification → not implemented at this stage
  - Digital On Top (DOT) → final chip assembly and timing verification performed with Innovus
  - Abstract view generation of analog and digital full custom blocks → implemented in our design for the analog IPs
  - Generation of Verilog model and timing characterization files (.lib) using Liberate tool → skill acquired but not used
  - Timing analysis → Innovus timing analysis and full chip sign-off flow using Tempus scripts
  - Back-annotated simulations → SDF generation and gate level simulations

Case study : CIC1 asic

- The design and implementation is in a **65 nm CMOS** technology
- CIC model written in **System Verilog** language
- Mostly digital functionalities : **digital on top** implementation (DOT)
- **Main functions** :
  - it collects the digital data coming from 8 upstream FE chips (MPA or CBCs)
  - it formats the signal in data packets containing the trigger information from 8 LHC bunch crossings and the raw data from events passing the first trigger level
  - data are transmitted to a lpGBT chip
- Inputs are 48 bit-lines at 320 Mbps using **2 different data formats**
- Outputs are sent through 7 bit-lines at 320/640 Mbps using an **unique data format**
- The core works at **2 different input voltages** : either at 1.0 V or 1.2 V
- A first prototype of the chip has been submitted on September 2018
- The second run of CIC (including SEU hardened design) is foreseen by June 2019

CIC physical design



- **IPs blocks** : **Phase aligner** (SMU univ. and CERN) used at each input data channel incoming from the 6 lines from each MPA/CBC FE. Is required in order to synchronize the signal with the internal clock (320 MHz). **SLVS Drivers and receivers** (INFN and Univ. Bergamo and Pavia), **CMOS I/O pads** and **I2C slave** (CERN), **ESD protections** (SOFICS).
- **CIC-Core** : based on 2 indipendent data paths, working in parallel.
- **SystemManager** : manages the clocks generation (40MHz, 320 MHz, 640MHz), clock gating, reset distribution, command decoding from the fast control frame.
- **SlowControl** : manages the communication via I2C protocol for control and monitoring fo the system. It contains the I2C slave and the internal I2C registers.
- Process **TSMC 65nm LP 1p7m4x1z1u** metal stack.
- **Wire bond** with AP RDL. Bare die, bumped ASIC (**flip chip)** with C4 bumps.
- ~743k standard cells after full flow.

CIC digital flow implementation (1)

- ***RTL coding in System Verilog language and simulation with ad-hoc testbench***
  - Implementation of ad-hoc testbench for simulations at different stages of the flow: behavioral level, synthesized netlist, back-annotated simulation using delay from SDF (Standard Delay Format)
- ***Synthesis (Genus tool):***
  - SDC timing constraints definition
    - Definition of different clocks domains: 320 MHz, 40 MHz, 160 MHz, 640 MHz
    - Design has been constrained for 640 MHz but relevant timing violations persisted (not synthesized)
    - Reset tree is fully asynchronous:
      - Required careful definitions at constraints level
      - Needed definition of multicycle paths in order to relax constraints on reset signal
  - Optimization issues
    - L1Path module presents several long combinatorial paths and this strains the optimizer tool:
      - Required several steps of optimizations
  - Instantiation of IO pads
    - IO pads manually instantiated within the code
    - SLVS drivers/receivers not precisely characterized: .lib file not included in timing analysis
  - Design analysis
    - Debug of failing paths using graphical tools and reports
    - Definition of false-paths, dont_touch and dont_use (reset tree and other critical paths)

CIC digital flow implementation (2)

- ***Placement and Routing (Innovus tool):***
  - Design import and setup
  - Floorplanning (placing analog blocks and bumps, power planning)
    - Design limited by IOs: placement of pads and bumps assignments are constrained by chip dimensions (imposed by the requirements of the hybrid board)
    - Placement of analog blocks (phaseAligners) critical for the timing
  - Placement (add well tap, Tie hi/lo cells, placing std cells, trial route)
  - Clock Tree Synthesis:
    - Definition of a CCOpt spec file taking into account the generation of the multiple clocks domains
    - No timing paths crossing two different clock domains
    - All the clocks are generated from the same 320 MHz clock
    - Generation of CTS simplified due to the presence of only one input clock
      - help received from CERN in specifying the clock tree
  - Routing
    - Router constrained only to the internal metal layers separating main clock and signals

CIC digital flow implementation (3)

- Verification
  - Timing verification performed at this stage required several steps of optimizations
- Abstract view generation of analogue blocks
- Calibre used for final DRC and LVS
- Power and rail analysis using Voltus tool
  - Management of two different power domains (core and periphery) and characterization of CIC core for working at two different voltages (1V and 1.2V)
  - Changes on power planning due to problems of power distribution revealed by static power and IR drop analysis
  - No optimization techniques for low power consumption have been applied
  - Generated VCD (Value Change Dump) information from simulation using the same testbench, for accurately results of static power analysis
  - Generated power reports and VDD/VSS IR drop diagrams (help from VCAD Cadence support)

CIC digital flow implementation (4)

- ***Signoff analysis:***
  - Metal filling
    - Main issue: timing analysis results are impacted
  - Signoff static timing analysis using Tempus tool
    - run MMMC timing analysis with crosstalk analysis (signal integrity) (help received from CERN)
    - signoff ECO fixing (Tempus flow)
  - Gate level simulation
    - setting up simulator to run a gate level simulation
    - run a SDF back annotated gate level simulation with the ad-hoc testbench

Training courses @ IPNL

- “Comprehensive Digital IC implementation and Sign-off” @ Europractice (RAL, UK)
- “Digital Mixed Signal IC Design and Implementation” @ Europractice (RAL, UK)
- TSMC N65 Mixed-signal workshop @ CERN

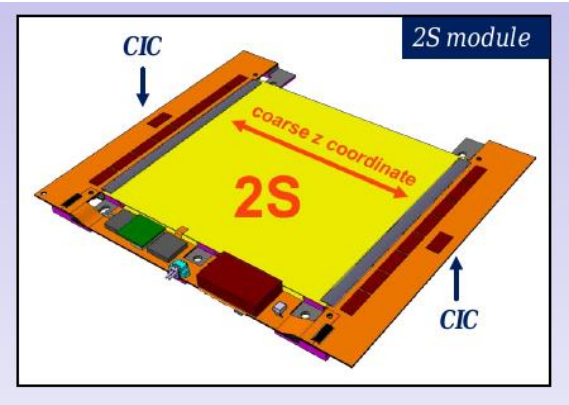
CIC project : lessons learned

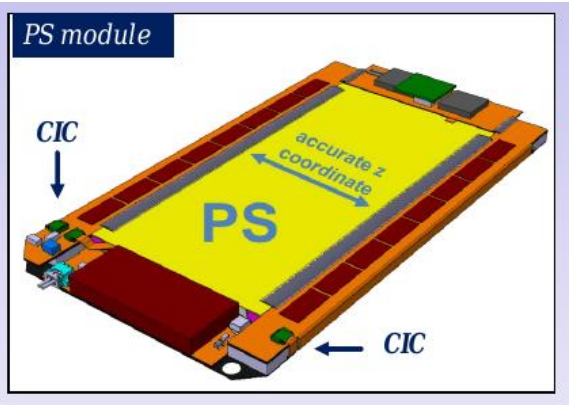
- ***Goal:*** Design of a mostly digital ASIC using Cadence digital-on-top flow
- Starting date: January 2017 (project restart date)
- Submission date : september 2018
- Project planning
  - Plan and schedule was not well documented and lacking details
  - Task assignments required several adjustments mainly due to a lack of previous experience
    - Three engineers and one physicist full time at IPNL
    - Two engineers and one PhD student at CERN
  - Requirements not documented (and changing)
- Project execution
  - important changements occurred in september 2017 (logic triplication, dimensional constraints)
  - the work methodology had been changed/adapted during project development
- Human factors
  - project manager reported punctually to the management without receiving adequate attention and time
  - project team lacked organisation
    - training happened during project development
    - there was no good communication within the project team
- Overall
  - project objectives are still not met
  - circuit will be tested in the following weeks
  - a redesign of large parts is already started

Back up

CIC context

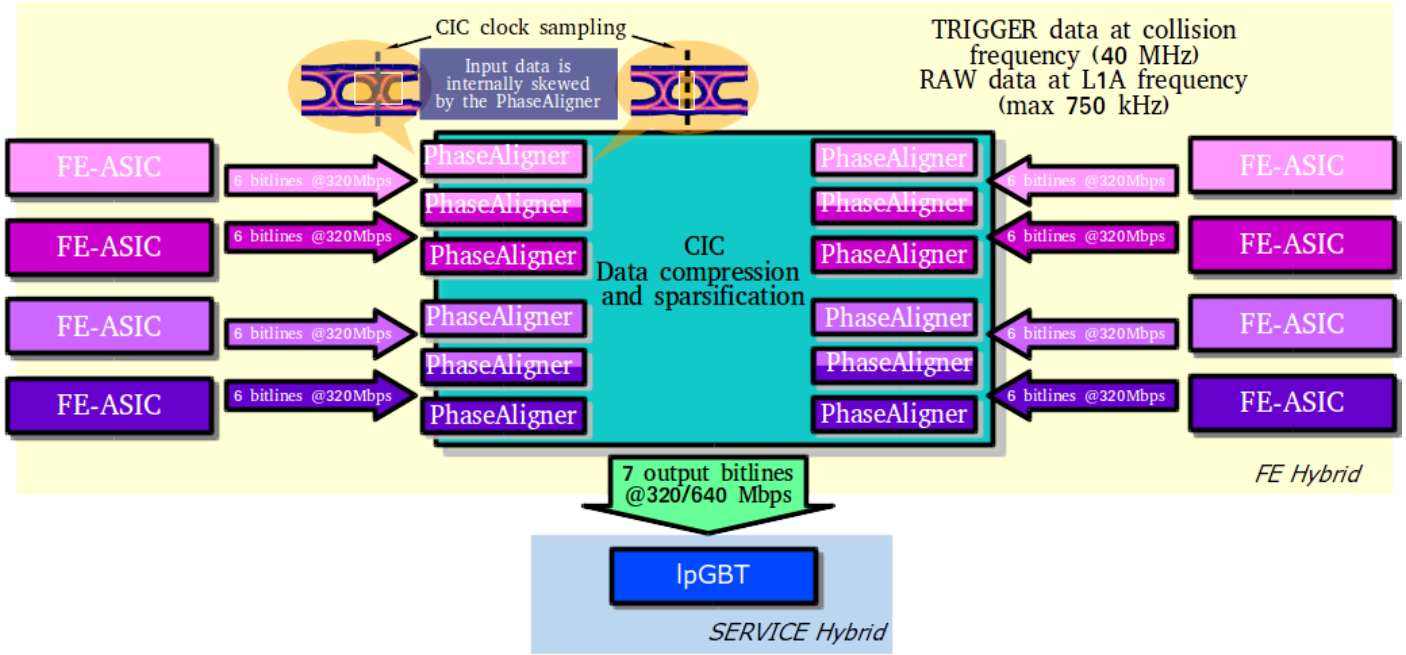
- For High-Luminosity LHC **(HL-LHC),** the CMS experiment will need a completely new tracker detector.
- A new type of detection module, based on *stub* creation, has been designed in order to ensure tracker data extraction at 40 Mhz.
- The future Phase-II CMS Outer Tracker will be populated with 2 pT-module types : **PS (pixel/strips)** and **2S (strips/strips)**.
- The **Concentrator Integrated circuit (CIC)** is a front-end chip common to PS and 2S modules and is the only shared component.





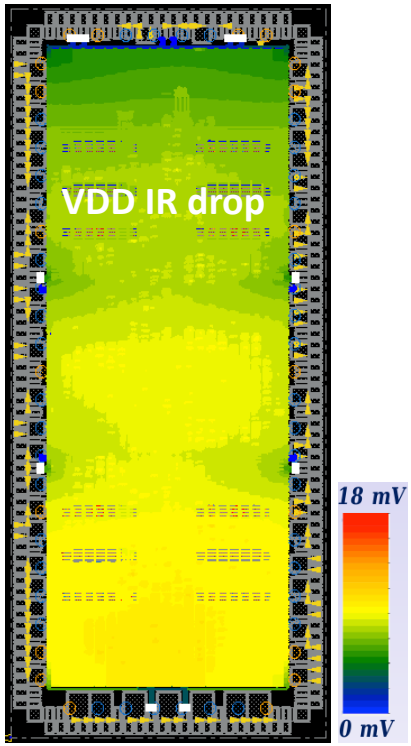
Architecture

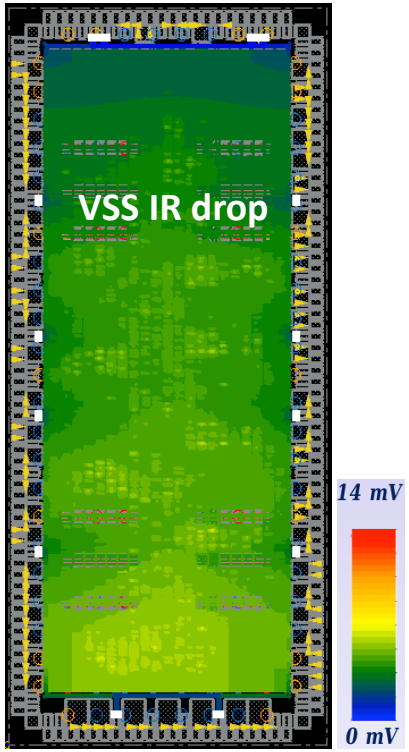
- 2 data streams are generated in the Front-end hybrid for the Back-end: L1 data (stream of frames responding to the L1-accept signal) and Trigger data (sequential stream of 8 BX long blocks where each block contains the trigger data aggregated from 8 FE chip associated to one CIC).
- CIC provides to the readout chain an extra factor 10 of data reduction, by grouping data over time (8 BX blocks) and space (8 input chips).
- CIC ASIC uniforms the data format for the Back-End.

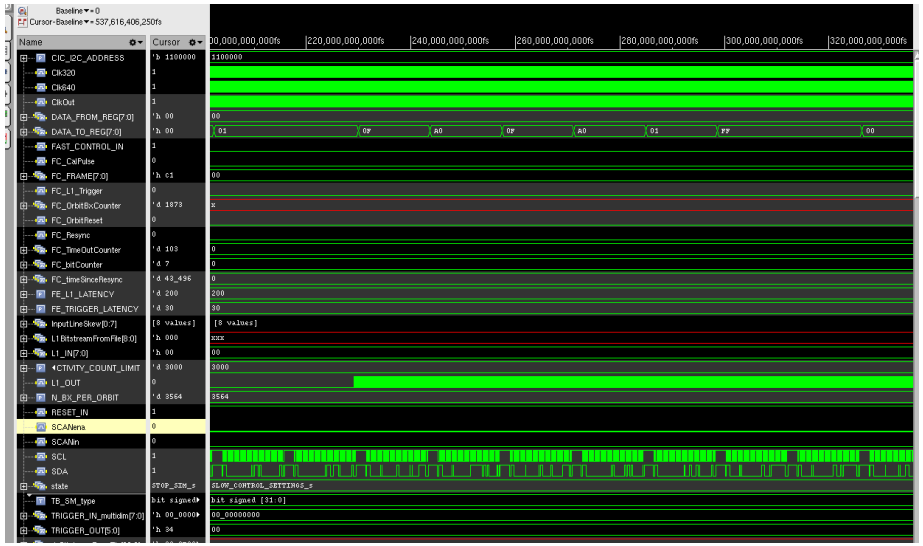


Simulations and power estimation

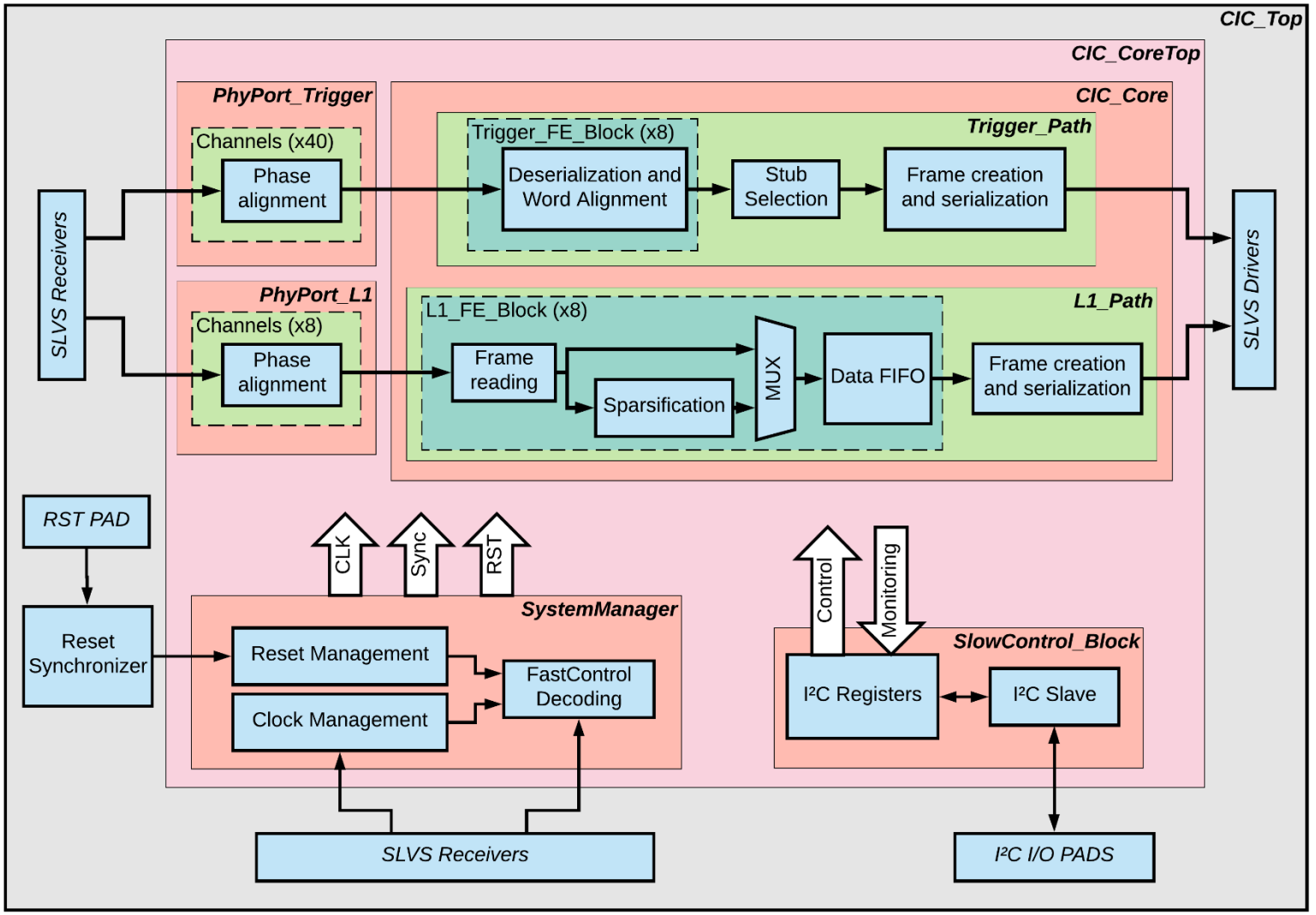
- Power estimation (worst corner) and IR drop analysis using **Voltus tool** (Cadence) :
  PS @ 1.1V : 288 mW. 2S @ 1.32V : 415 mW (during running phase).
- Test design functionalities within a scripts-based framework (python).
- Back-annotated simulations are performed using **Simvision tool** (Cadence) in 3 corners : MAX (ss, 0.9V, -40°C), TYP (tt, 1V, 25°C), MIN (ff, 1.32V, 0°C) and 2 test cases : PS and 2S.
- Results show that all functionalities are met.



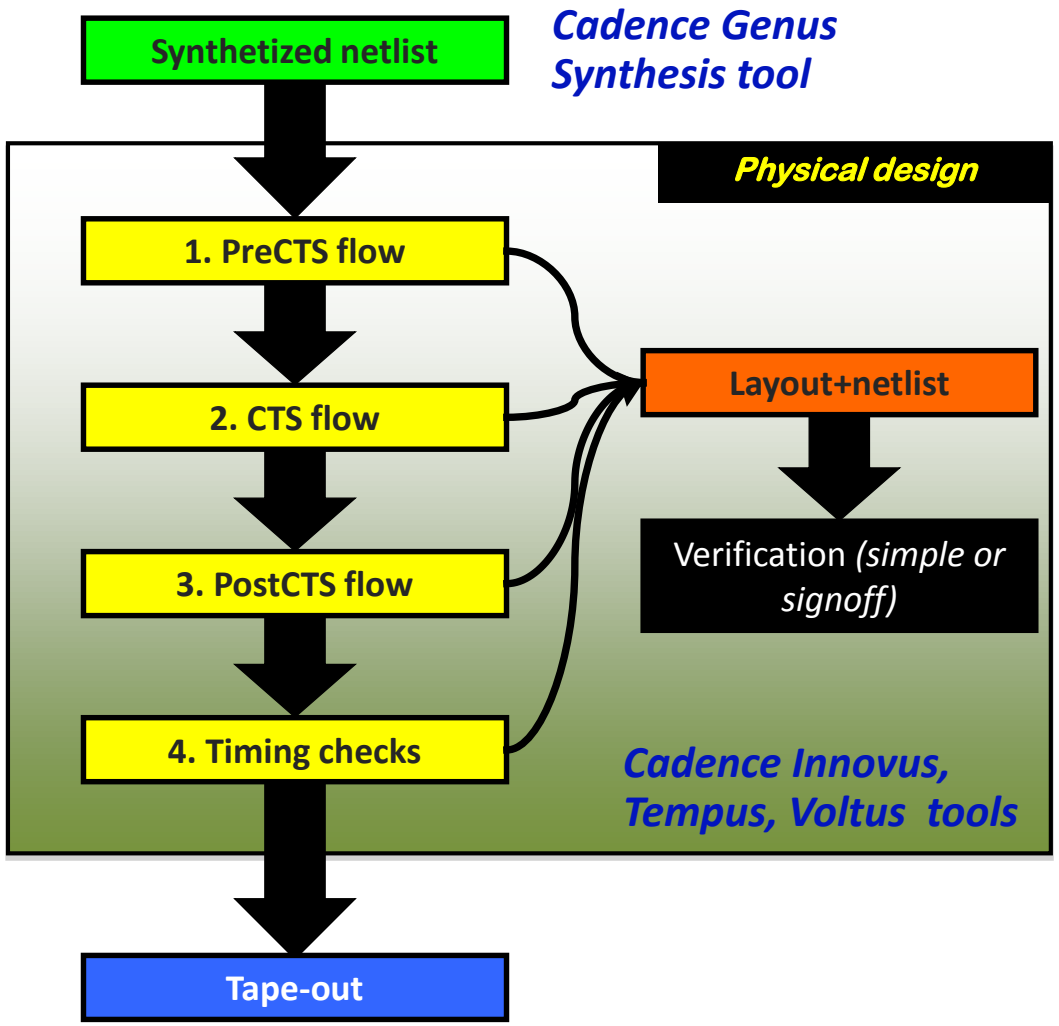




CIC simplified block diagram

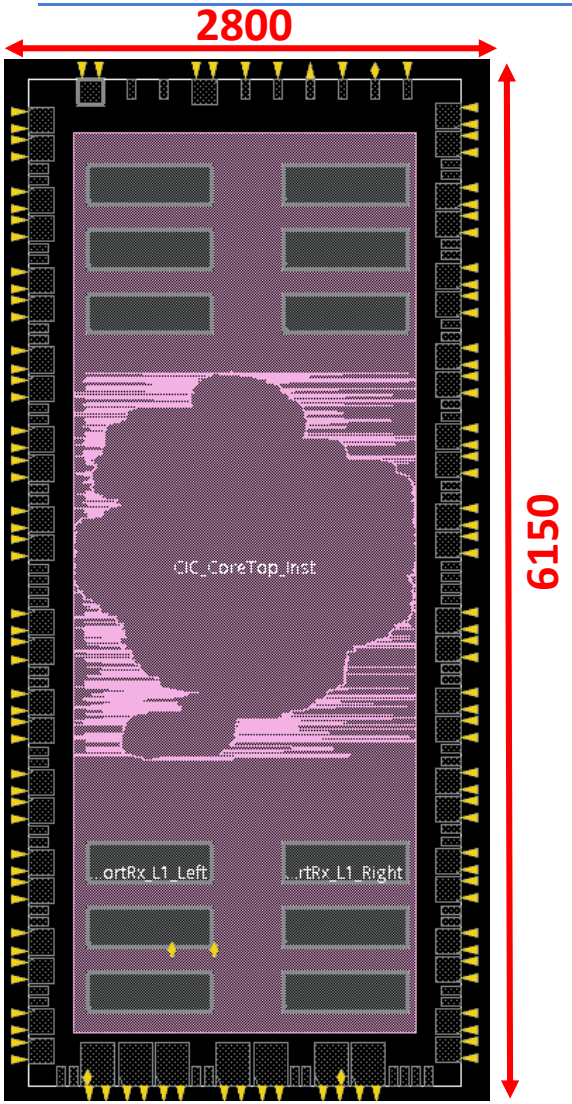


Digital design flow



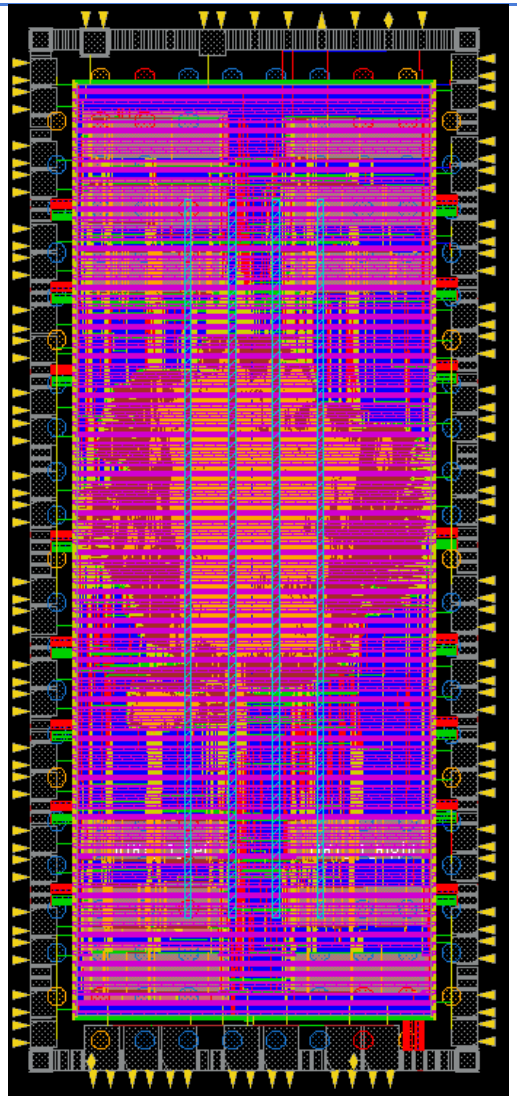
- The digital flow, based on a series of scripts, permits to reach the final file (**GDS**) for the Tape-out phase starting from the behavioral description of the architecture (**RTL**).
- Tape-out phase: final step before the ASIC fabrication.

Physical design



- Digital on Top implementation
- Die dimensions take into account bondable pad + seal ring (not shown in figure)
- Process TSMC 65nm LP 1p7m4x1z1u metal stack
- Wire bond with AP RDL (not shown in figure)
- **Periphery ring:**
  - 48 sLVS RX pads along the left and right sides (core+periphery supplies)
  - 7 sLVS TX pads on the bottom side
  - 2 sLVS RX + 7 CMOS pads on top side
- **PHY-ports:**
  - 2 PHY-port blocks phase-aligns 8 L1_IN bitlines wrt SYS_CLK
  - 10 PHY-port blocks phase-align 40 TRIGGER_IN bitlines wrt SYS_CLK
- **CIC_Core**:
  - Flat synthesis of trigger and L1 data-path, I^2C and Fast control blocks.
  - 8 Front-End blocks each containing a 16 words by 800b FIFO @40 MHz (22,6k cells).
  - **~372k standard cells**

Physical design



- **Top level power routing:**
  - 15 vertical stripes in AP layer
  - 98 horizontal stripes in M7 layer
- **Periphery supply:**
  - The power routing of the periphery supply is being kept separate from the core
  - Radiation tolerant ESD protections (designed by SOFICS): used in periphery ring
- **Clock tree synthesis (CTS):**
  - Clock tree routed using M5 and M6

CIC power estimation

- Power budget @ PS module: **250 mW**
- Power budget @ 2S module: **300 mW**

- Power estimates (in mw) were processed for the complete chip (CIC_top), for the **worst corners** in 2 differents configurations. For the analog Phyport part estimations are used.

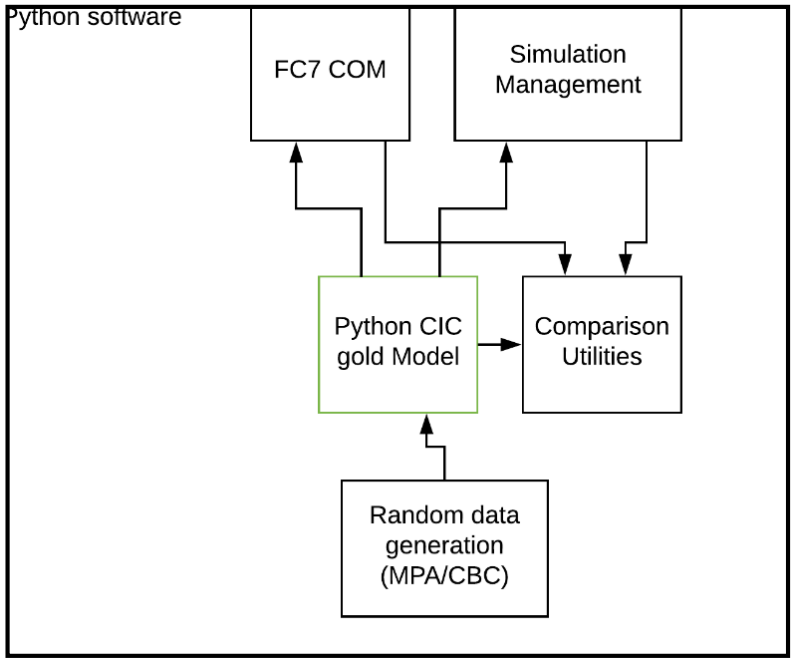
Corner		Startup phase (*PhyPort init,...*)			Running phase (*high input load*)		
		Digital	***Analog***	***Total***	***Digital***	***Analog***	***Total***
PS-like	1.1V/0° C	182	27	**209**	183	16	**199**
2S-like	1.32V/0° C	259	63	**322**	282	56	**338**

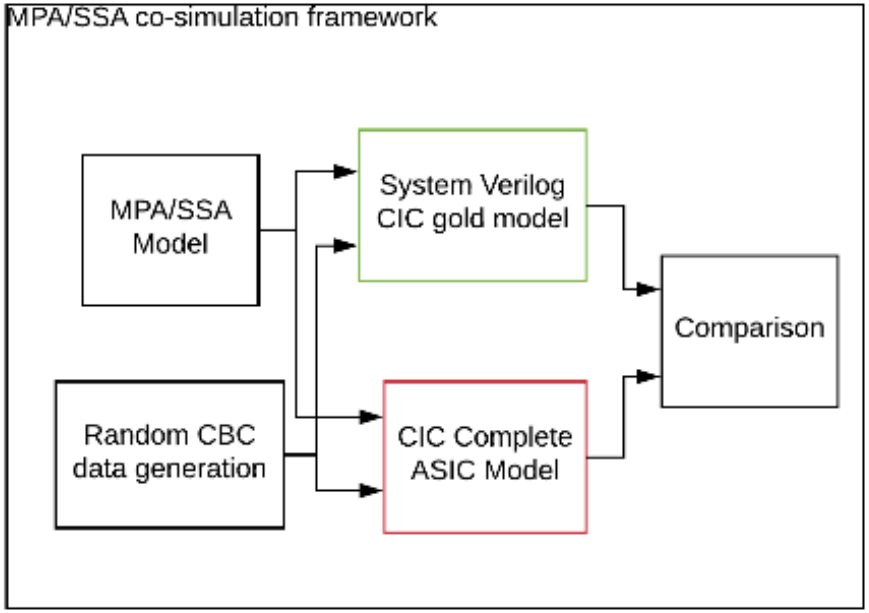
- This is before CTS (expect **30% increase** then), but **without any power-oriented optimization**. We will not further optimize the power budget for the CIC1.

CIC testbench

- A **standalone testbench** has been implemented in order to:
  - Check model functionality
  - Perform the comparison between data stream from CMS simulation environment with the CIC model output after the phase alignment and data treatment.

- **System level Testbench** for the validation of the full acquisition chain, developed at CERN





CIC team

➔ **L. Caponetto (IPNL)**: **technical coordination**, physical design

➔**G. Galbit (IPNL)**: digital design, system test and CIC characterization testbench

➔ **B. Nodari (IPNL)**: block-level synthesis, physical design

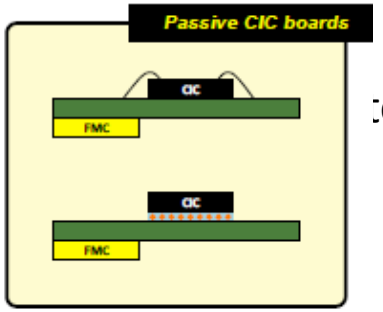
➔**S. Scarfi (CERN)**: system validation

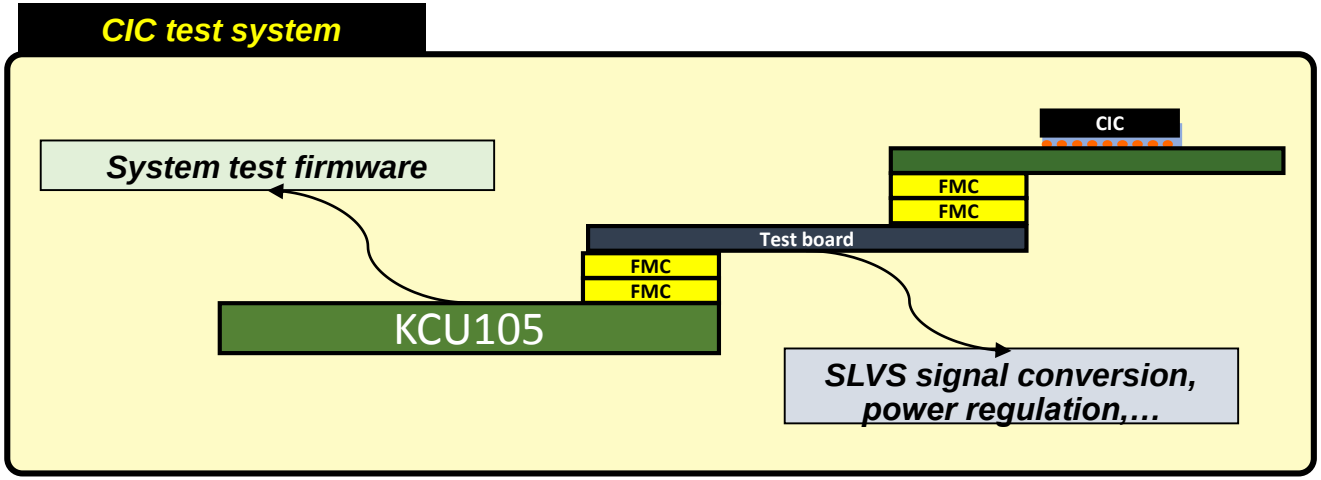
➔**S. Viret (IPNL): scientific coordination**

➔ In addition to that we can now count on the support from the CERN CMS TRACKER IC team, which has gained good experience in the TSMC 65 nm technology.

CIC test system

- CIC prototypes will be soldered on small passive PCBs and will be driven externally.
- 2 PCB flavors will be produced: **wire-bonded** and **soldered** (we will also order bumped CIC1 wafers).
- Necessary tasks are:
  1. Design and routing of the 3 speci test vehicle, test board, converter)
  2. Implementation of the test bench **firmware**
  3. Implementation of the test bench **software**
- The full system will use 3 boards:





➢ **C. Guerin & W.Tromeur** (IPNL) : CIC characterization testbench and boards development