Pierre Auger Observatory

Surface Detector Electronics Upgrade
List of ECR
for UUB Version 3

Abstract:
This document is the reference list of the ECR for the UUB Version 3

Document written by:	P. Stassi Project System engineer	Agreed by:	T. Suomijärvi D. Nitz Task leaders
Date:	14/12/18	Date:	
Local Reference:	n/a	EDMS Reference:	2044429 v.3

Table of Content

ACRONYMS

ADC	Analog to Digital Converter
BOM or BoM	Bill Of Material
BGA	Ball Grid Array
BSRU	Base Station Radio Unit
CR	Configurational Requirement
DAC	Digital to Analog Converter
DC	Direct Current
EA	Engineering Array
EAS	Extensive Air Shower
ECR	Engineering Change Request
EMI	ElectroMagnetic Interference
ER	Environmental Requirement
ESD	ElectroStatic Discharge
FDIR	Failure Detection, Isolation and Recovery
FPGA	Field Programmable Gate Array
FR	Functional Requirements
Fs	Full scale
GPS	Global Positioning System
H/W	HardWare
ICD	Interfaces Control Document
I2C	Inter-Integrated Circuit
IR	Interface Requirements
LED	Light Emitting Diode
LSB	Low Significant Bit
LVDS	Low Voltage Differential Signaling
Msp/s	Mega samples per second
MCU	Micro Controller Unit
n/a	non applicable
NC	Non Conformance
OR	Operational Requirements
OS	Operating System
PAO	Pierre Auger Observatory
PBS	Product Breakdown Structure
PCB	Printed Circuit Board
PMT	PhotoMultiplier Tube
PR	Physical Requirements
QR	Quality Requirements
RD	Reference Document
RDA	Research and Development Array
RF	Radio Frequency
RMS	Root Mean Square
SC	Slow Control
SD	Surface Detector
SDE	Surface Detector Electronics
SDEU	Surface Detector Electronics Upgrade
SMA	SubMiniature version A connector
SR	Support Requirements
S/W	SoftWare
TBC	To Be Confirmed
TBD	To Be Defined
TBW	To Be Written
TPCB	Tank Power Control Board
UB	Unified Board
UC	Upgrade Committee
USB	Universal Serial Bus
USB OTG	USB On-The-Go
UUB	Upgraded Unified Board
UHE	Ultra High Energy
UHECR	Ultra High Energy Cosmic Ray
VM	Verification Matrix
WBS	Work Breakdown Structure
WP	Work Package

DOCUMENT CHANGE RECORD

Issue	Issue Date	Changes Approved by	Modified Pages Numbers, Change Explanations and Status
Draft	23/11/18	P. Stassi	1st DRAFT for approbation
V1	05/15/18	P. Stassi	First Issue
V2	12/12/18	P. Stassi	Before meeting version, updated with received e-mails
V3	14/12/18	SDEU Team	After Orsay Meeting decisions 13-14 December 2018

1 INTRODUCTION

The document defines the complete list of the UUB NC observed in the Version2 retrofitted. The solutions to correct the NC can be ECRs.

ECRs are also proposed for simplification.

The status of all the UUB ECR is defined in the list, their acceptation, and their implementation for the next production phase.

2. NON CONFORMANCES REPORTED BY SDEU TEAM ON UUB VERSION 2 RETROFITTED

2.1 NC Reported from Grenoble (NC-GR)

NC-GR#	Description	Issue	Proposed solution	ECR ?
1	Manufacturing extra PCB part on the front hasn't been removed	Can't be mounted in box	Remove it	NO
2	J1 connector is not in good position (horizontal)	Bad soldering position. Bad fixing on front panel. Front panel cannot be mounted	Modify design to remove PCB behind the fixed connector nut.	YES ECR #12
3	Bad J1 connector footprint (pins 1, 2, 3 & 4)	Difficult to solder	PCB modification	YES ECR#13
4	B1 connector in wrong position	Fuse cable is difficult to connect	Specify strongly to sub-contractor the good	NO
~~5~~	Q5 transistor strange soldering position	Could generate a bad solder	Feedback with sub-contractor	NO
6	uub serial number sticker	Do not correspond to Auger specification	Make new	NO
7	C50, C127, C129, C155 capacitor package. Defined in 0805 but TDK ref is 0603 package	Could generate a solder issue	PCB must be modify for 0603 package or 0805 capacitor ref. must be find.	YES ECR#14
8	C389 capacitor package. Defined in 1206 but it is 1210 package	Could generate a solder issue	PCB must be modify for 1210 package or 1206 capacitor ref. must be find.	YES ECR#15
9	R1_2,R4_1 & R4_2 capacitor package. Bought in 0402 but it is 0603 package in PCB	Could generate a solder issue	Change component in 0603 package	YES ECR#42

NC-GR#	Description	Issue	Proposed solution	ECR ?
10	Q1_1,Q1_3,Q1_4,Q1_5 transistor package. Defined in SOT-23 on PCB but it is SOT-323/SC-70 package.	Could generate a solder issue	PCB must be modify for SOT-323 package (footprint error).	YES ECR#43
11	SMA connector's nut are missing	uub can't be mounted on front panel		NO
12	Main power supply connector's nut is missing	uub can't be mounted on front panel		NO
13	M8 soldered in bad position (orientation)	5V Power Supply falls to 1,119V: USB		NO
14	R424 & R428 resistor value are 8,45 kOhms instead 6,8 kOhms	Slow-Control 3,3V & Analog 3,3V measurement		NO
15	Bad hardware FPGA boot configuration	FPGA can't start	R214 must be removed	YES ECR#1
16	M52 Fanout clock has 2 Pull-up resistor on OE pin (32)	None	Fanout circuit removed, see ECR#17	NO
17	120 MHz Fanout doesn't work for several UUB	3,3V voltage ramp start is too slow and the Slow-control µcontroller generate voltage in 3,3V power supply when it as disable	Fanout circuit removed, see ECR#17	NO

NC-GR#	Description	Issue	Proposed solution	ECR ?
20	Sometime (1/20 around), the Slow-control stays frozen after a switch, radio resets or Watchdog. UUB must be restart by a turn off	During a UUB Reset, Watchdog, or Radio Reset, the components on Slow-Control Micro-Controller I2C interface are still	To have the 3.3V switchable for the I2C slaves from the MCU	YES ECR#36
21	R339 resistor has bad value.	Could generate a "Reset loop" when the Radio is tuned OFF	It must be changed from 2,49 k Ohms to 24 k Ohms	YES ECR#18
22	Bad Vref voltage for the front-end	The R27_3 resistor has been mounted	Remove R27_3 Resistor	NO
23	Clock frequency swing dynamic is too small	U42 Voltage reference component is a REF3318 (1,8V)	Canceled by ECR#29	NO
24	For several UUB, FPGA frozen during its start if there no PC connected on its USB terminal	USB Port not usable for maintenance	See ECR#20	YES ECR#20
25	Slow-Control 3,3V power is not connected to M38 pin 4	Risk of issue	Modify the schematic to realize the connection.	YES ECR#21
26	Fan-out "Software" configuration I2C in 3,3V is connected to the FPGA bank 501 in 1,8V	Fan-out can't be programmed by software	Canceled by ECR#17	
28	Sometime bad data sent to FPGA from ADC. The AD9628 crash sometime. Bad initialization	Sometime, ADC AD9628 crash	ADC 1,8V power switched by a transistor for each, 5 transistors but with a same enable	YES ECR#3

NC-GR#	Description	Issue	Proposed solution	ECR ?
29	No 10V power measurement value on the Slow-control	The connection between 10V power and R244 is not present	Modify in schematic and layout	YES ECR#24
31	Wrong (negative) baseline for all high gain channels.	R164 soldered with wrong value 24k (probably by SITAEL retrofit).	R164 replaced with value 2.4k. This solved the problem.	NO
32	Current limiter switched off power despite input voltage range okay.	Diode D1 (DDZ9702T) was mounted in wrong direction (by SITAEL).	Diode D1 replaced, mounted with correct polarity.	NO
33	Traco modifications (document by E.L.) show unwanted side-effects.	problems with reboot, -3.3V can't be turned off	Implement solution with reed relay	YES ECR#26
34	Wrong (negative) baseline for ADC channels #9.	R35_2 soldered with wrong value 330R (probably by SITAEL retrofit).	R35_2 replaced with value 270R. This solved the problem.	NO
35	Wrong (negative) baseline for ADC channels #6.	R10_5 soldered with wrong value 274R (probably by SITAEL retrofit).	R10_5 replaced with 430R(closest to nom. 442R)--> problem solved.	NO
37	When the UUB is integrated in the box the uub can't start	The front panel push the Reset switch	Move J1 on PCB	YES ECR#27
38	For PMT & Tank the signals are attenuated by ESD components	Value expected does not correspond. Error in schematics	Make correction in schematic	YES ECR#28

NC-GR#	Description	Issue	Proposed solution	ECR ?
41	Sometime UUB in the field restarts itself	Unknown	See ECR#44	YES ECR#44
42	Communication between FPGA and Slow-control is loosed	I2C configuration		

2.2 NC Reported from Lecce (NC-LE)

NC-LE#	Description	Issue	Proposed solution	ECR ?
1	Wrong input signal polarity to ADC	Wrong offset after inverting the lines on PCB. The offset has not been consequently inverted	Invert offset polarity	YES ECR#39
2	ADC get stuck at initialization. Only way to reset is to power down ADCs	Problem when VADD, VDDD and clock are started all together Idem NC-GR28 and NC-MA02	ADC 1,8V power switched by a transistor for each, 5 transistors but with a same enable line	YES ECR#3
3	Spikes on channel 9 Idem NC-MA7	Very little spikes present on UUB in Malargue and Grenoble. Not present on board in Lecce where the TRACO has	Solved, no ECR needed. Come from the Traco position on the prototype version.	NO
4	Switch S1 (RS1)	Not used	Remove RS1	YES ECR#41

2.3 NC Reported from Wuppertal (NC-WU)

NC-WU#	Description	Issue	Proposed solution	ECR ?
1	It is possible, that in case of a reset of the micro controller, the I2C bus was stuck due to a I2C slave is holding low the data line.	This affects only the I2C bus between the MCU and its slaves, not the bus between the Zynq and MCU. (= NC-GR20)	To have the 3.3V switchable for the I2C slaves from the MCU	YES ECR#36

2.4 NC Reported from Malargue (NC-MA)

NC-MA#	Description	Issue	Proposed solution	ECR ?
1	I2C communication issue with Zynq and slow control	Identical to NC-GR42	See ECR#44	YES ECR#44
2	ADC start problem (ADCs which stuck with one particular value)	Identical to NC-LE02, NC-GR28	See ECR#3	YES ECR#3
3	the electrostatic protections which are removed	Identical to NC-GR38	See ECR#28	YES ECR#28
4	The protection USB terminal (of zynq)	Identical to NC-GR24	See ECR#20	YES ECR#20
5	GPS antenna or its cables sometimes get in short circuit.	Damage the GPS receiver	Add fuse on GPS power supply	YES
6	Reset button is too close to the front panel and sometimes it is pressed constantly.	Identical to NC-GR37	Move J1 on PCB	YES ECR#27
7	ADC channels of SSD are quite noisy. This particular noisy looks be related with the PCB design.	Identical to NC-LE03 and NC-MA07	Solved, no ECR needed. Come from the Traco position on the prototype version.	NO
8	Clock FanOut problems	Identical to NC-GR17	See ECR#17	YES ECR#17

2.5 NC Reported from Karlsruhe, Prague or Siegen testing facilities or MTU (NC-TE)

NC-TE#	Description	Issue	Proposed solution	ECR ?
1	Traco modifications show unwanted by-effects.	Identical to NC-GR33	See ECR#26	YES ECR#26
2	Digital Flat cable to be shielded (TBC)	Risk of emitted noise (60MHz). To be investigate	See ECR#37	YES ECR#37

3 LIST OF DEFINED ECR FOR UUB VERSION 3

Items in blue are related to **loose parts**

#	Issue	Motivation, source	ECR	Accepted and implemented?
1	FPGA Can't Start, bad H/W config.	Error in schematics	R214 must be removed	▣ YES ☐ NO
2	Set in Flash Reset without Transistor	Simplification	Remove Q6, R224 & add R223, R227	▣ YES ☐ NO
3	1,8V power supply analog and digital, separated for the ADCs	Sometime ADCs are not initialized NC-LE02, NC-GR28	ADC 1,8V power switched by a transistor for each, 5 transistors but with a same enable line	▣ YES ☐ NO
4	FPGA Done pin to Slow-control	fan out issue NC-GR17	Disconnect FPGA Done signal on Slow-control and resistor R343.	▣ YES ☐ NO
5	ADCs DCO in clock twin wires length aren't the same between AD9628 ADCs	Data-stream read issue	All ADCs clock wire must have the same length	▣ YES ☐ NO
6	Current limit provided by Extension connectors	Radio Project request	Add 200mA resettable fuse	▣ YES ☐ NO
7	Extension connector buffer power Enable/Disable (3,3V)	Use less power consumption when not used (w/o AMIGA)	Add a jumper or zero ohms resistor on both channel	▣ YES ☐ NO
8	GPS antenna cable is too long	Simplification	Remove 1 or 2 cm. This must be validated with the new front-panel. The SMA connector will be higher for the Front-panel version 3	▣ YES ☐ NO
9	PMT cable are too long	During integration the cable could be broken	Remove 0,5 cm	▣ YES ☐ NO

#	Issue	Motivation, source	ECR	Accepted and implemented?
10	GPS antenna or its cables sometimes get in short circuit.	GPS Receivers can be damaged	Add fuse on 5V pin on GPS connector	☒ YES ☐ NO
11	UUB generates noise on tank 24 Volts	Radio project adaptation	Add BNX002 Murata EMI filters on 24v after J1 Reference confirmed by the radio project team	☒ YES ☐ NO
12	J1 connector is not in good position (horizontal)	front panel can't be mounted – NC-GR02	Modify design to remove PCB behind the fixed connector nut.	☒ YES ☐ NO
13	Bad J1 connector footprint (pins 1, 2, 3 & 4)	Difficult to solder NC-GR03	PCB modification	☒ YES ☐ NO
14	C50,C127,C129,C155 capacitor package. Defined in 0805 but TDK ref is 0603 package	Could generate a solder issue NC-GR 07	PCB must be modify for 0603 package or 0805 capacitor ref. must be find. The BOM component specification error must be corrected (CAP-054)	☒ YES ☐ NO
15	C389 capacitor package defined in 1206 but it is 1210 package	Could generate a solder issue – NC-GR08	PCB must be modify for 1210 package or 1206 capacitor ref. must be find. The BOM component specification error must be corrected (CAP-056)	☒ YES ☐ NO
16	M52 Fanout clock has 2 Pull-up resistor on OE pin (32)	NC-GR16	~~R294 remove in schematic and layout~~ Not an ECR anymore, see ECR#17	
17	120 MHz Fanout doesn't work for several UUB	3,3V voltage ramp start is too slow and the Slow-control µcontroller generate voltage in 3,3V power supply when it as disable NC-GR17	- Exchange present fan-out component with Jitter Cleaner used in the UUB Version 1, (this will add 300mW on power consumption)	☒ YES ☐ NO

#	Issue	Motivation, source	ECR	Accepted and implemented?
18	R339 resistor has bad value.	Could generate a "Reset loop" when the Radio is tuned OFF – NC-GR21	It must be changed from 2,49 k Ohms to 24 k Ohms	☒ YES ☐ NO
19	Clock frequency swing dynamic is too small	U42 Voltage reference component is a REF3318 (1,8V) – NC-GR23	Canceled by ECR#29	
20	For several UUB, FPGA frozen during its start if there no PC connected on its USB terminal	NC-GR24 and NC-MA04	- Add diodes (see schematics in annex) Temporary baseline solution (to be validated on more than one UUB) - Add buffer on Rx/Tx additionally (FPGA protection) - Study a new U-BOOT configuration (S/W) - Test the design proposed by the Malargüe team TO BE DECIDED end of Jan 2019	☐ YES ☐ NO
21	Slow-Control 3,3V power is not connected to M38 pin 4	NC-GR25	Modify the schematic to make the connection	☒ YES ☐ NO
22	Fan-out "Software" configuration I2C in 3,3V is connected to the FPGA bank 501 in 1,8V	Fan-out can't be programmed by software NC-GR 26	Canceled by ECR#17	
23	Identical to ECR#3			
24	No 10V power measurement value on the Slow-control	The connection between 10V power and R244 is not present – NC-GR29	Modify in schematic and layout	☒ YES ☐ NO

#	Issue	Motivation, source	ECR	Accepted and implemented?
25			Not an ECR	
26	Traco modifications show unwanted by-effects.	problems with reboot, -3.3V can't be turned off	Implement solution with reed relay.	▣ YES ☐ NO
27	When the UUB is integrated in the box the UUB can't start	The front panel push the Reset switch NC-GR37	Move J1 on PCB	▣ YES ☐ NO
28	For PMT & Tank the signals are attenuated by ESD components	Value expected doesn't correspond – NC-GR38	Make correction in schematic	▣ YES ☐ NO
29	120 MHz clock tuned by DAC	Is it really needed and used?	Remove DAC component and add resistor bridge but keep the foot print on the layout	▣ YES ☐ NO
30	Covering solution for USBs connectors on front panel	Protection from dust	Use 3D printed plastic cover panel proposed by Malargue team, but study a conductive material of conductive coating for shielding. TO BE DECIDED during Q1 2019	☐ YES ☐ NO
31	The USB connector of slow control is on the Front Panel	Never used in the fields. To have it on FP is useless	Modify the position of USB connector of slow control from the Front Panel to the middle of the board. Change connector model (the front panel type is already procured, 0.46 EUR)	▣ YES ☐ NO
32	Additional test point to measure DAC signal	It is difficult to measure the ramp signal of DAC 7551 and DAC 5694	Add test points (3x) for easy measurement with scope probe (a list should be provided by KIT)	▣ YES ☐ NO

#	Issue	Motivation, source	ECR	Accepted and implemented?
33	Unique MCU software (SC): select field/test version with a jumper	Maintain common MCU software: select "test mode" with a jumper	- Provide on the layout a static signal via jumper to MCU; a low level (default) boots the software in "field" mode; a high level boots software in "test" mode with all supply voltages turned off. - Modify the SC S/W for the 2 modes	☒ YES ☐ NO
34	Radio reset out can generated issue	Risk of loss of control of the logic. Signal not used.	~~Put a 0 Ohm resistor on the signal on the PCB~~ REJECTED ECR	☐ YES ☒ NO
35	Assemble already programmed flash memory chips	Programming of flash takes a lot (too much) time	Assemble already programmed flash chips, implications to be checked (not really an ECR but more a fabrication spec.)	☒ YES ☐ NO
36	It is possible, that in case of a reset of the micro controller, the I2C bus was stuck due to an I2C slave is holding low the data line. This affects only the I2C bus between the MCU (SC) and its slaves, not the bus between the FPGA and MCU	Risk of lock of the I2C MCU Slave bus	Have the 3.3V switchable for the I2C slaves from the MCU	☒ YES ☐ NO
37	Digital Flat cables to be shielded?	Risk of emitted noise (60MHz), issue for Radio project	Change internal cables and connectors for shielded versions (PCB modifications) TO BE CONFIRMED BY Radio project Team	☐ YES ☐ NO
38	Isolate FPGA/Slow-control connections	FPGA protection	Add buffer for I2C and remove it from the “Done” signals	☒ YES ☐ NO
39	Wrong offset after inverting the lines on PCB. The offset has not been consequently inverted	Wrong input signal polarity to ADC – NC-LE01	Invert offset polarity CRITICAL. The new design should be verified carefully	☒ YES ☐ NO

#	Issue	Motivation, source	ECR	Accepted and implemented?
40	Spikes on channel 9	NC-LE3, NC-MA7	Solved, no ECR needed. Come from the Traco position on the prototype version.	
41	Switch S1 (RS1) not used	Simplification	Remove RS1	☒ YES ☐ NO
42	R1_2,R4_1 & R4_2 capacitor package. Bought in 0402 but it is 0603 package in PCB	NC-GR09	Make correction on the BOM	☒ YES ☐ NO
43	Q1_1,Q1_3,Q1_4,Q1_5 transistor package. Defined in SOT-23 on PCB but it is SOT-323/SC-70 package.	NC-GR10	PCB must be modify for SOT-323 package footprint	☒ YES ☐ NO
44	Sometime UUB in the field restarts itself	NC-GR41 NV-GR42	- Use the SC MCU to control the LED controller DAC (temporary baseline solution) - Use SC MCU DAC channels for the LED Controller - Add another I2C port on the FPGA to control the LED controller DAC - Understand the FPGA I2C ports behavior TO BE DECIDED end of Jan 2019	☐ YES ☐ NO
45	Communication between FPGA and Slow-control is loosed	NC-GR42	Idem ECR#44	
46	Protection of the FPGA	Risk of problem with the FPGA	Idem ECR#38	

#	Issue	Motivation, source	ECR	Accepted and implemented?
47	RFI noise maybe conducted through the digital connectors 24 V power supply	Radio Project	Add EMI filters on 24 V of the digital connectors, component to be specified by Radio project team	▣ YES ☐ NO
48	RFI noise can be conducted through all non-shielded (non-coax) interface connectors	Radio Project	- Add filters on non-coax connectors signal - Use shielded connectors and cables for non-coax cables - Add DC/DC coil shielding on PCB Solution to be studied by Radio project Team	☐ YES ☐ NO
49	Use 2 DAC channels of the SC to drive the LED Controller	Simplification	Idem ECR#44	
50	8 channels switches not used	Useless. Can free FPGA lines	Change the PCB and the F/W (use more test points)	▣ YES ☐ NO
51	Digital connectors model on board, J8 and J9, 24 pins, does not allow to find OTS low cost cables	Changing J8 and J9 by 0.1 in pitch, 26 pins, IDC connectors, allow using standard PC cable. Radio project	Change J8 and J9 with this TBD reference (this connector was already changed between V1 and V2, ECR#5.18, ECR list V1) Solution to be studied by Radio project Team	☐ YES ☐ NO
52	PMTs power supplies can be in short circuit	To avoid losing all PMTs channels because of one short circuit	Add resettable fuses on each 12v of PMT (12V) all the PMTs (range to be proposed by Malargue team)	▣ YES ☐ NO
53	Change the front panel digital connector	ECR #51 Radio project	Change for 2-rows 25-pin Sub-D connector Solution to be studied by Radio project Team	☐ YES ☐ NO

4 ECR ACTIONS LIST

For the ECR#: **1, 2, 4, 5, 6, 7, 8, 9, 10, 12, 13, 14, 16, 17, 18, 21, 24, 26, 27, 28, 31, 32, 33, 36, 38, 39, 41, 42, 43, 50, 52**

Actions to do:

- **A- Update the schematics, the BoM and after the Layout by integrating all these ECR.**
- **B- Verification and validation of schematics and after, the layout**

Responsibility:

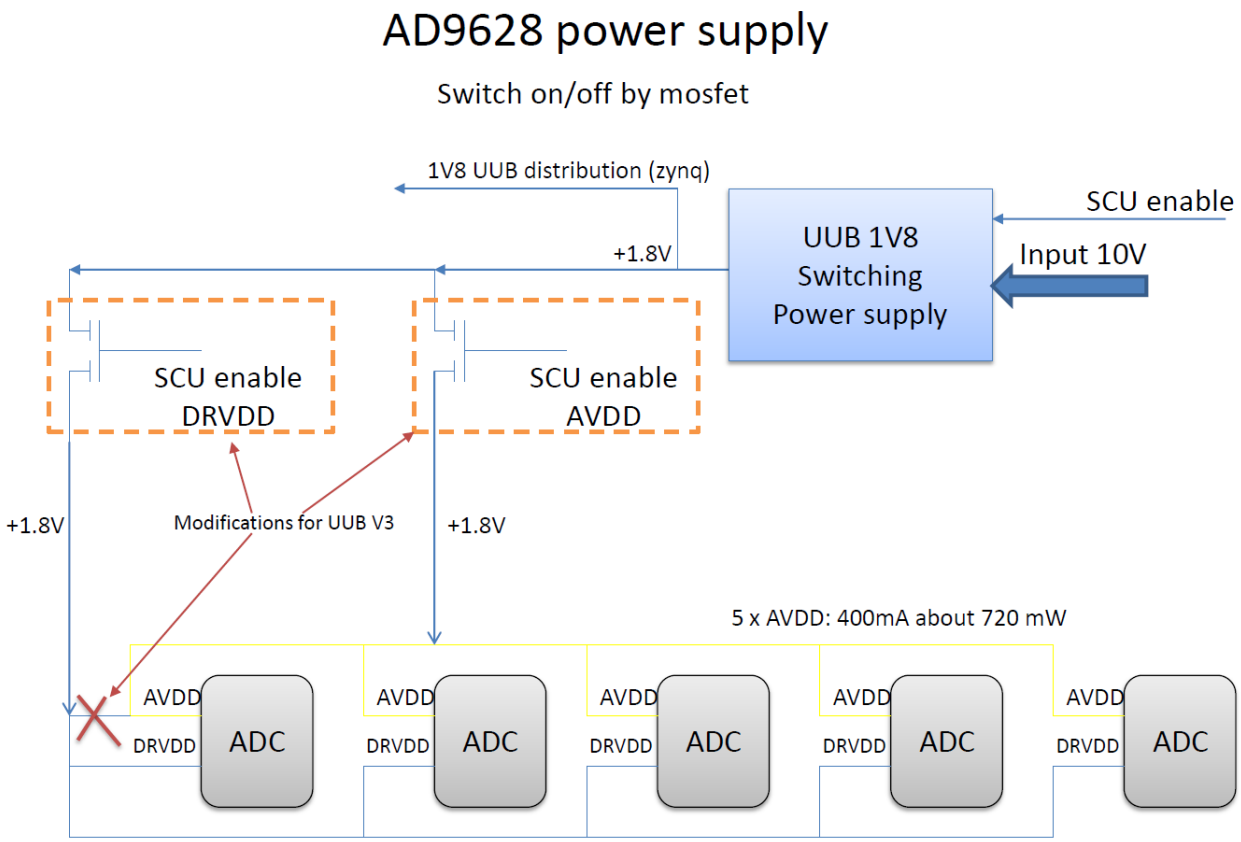
- **A- Grenoble**
- **B- Lecce and Wuppertal**

ECR#	Short Description	ACTIONS	RESPONSIBLES
3	ADC initialization issue	Confirm the solution with 5 transistors for each power line	Lecce
20	USB issue	Study the S/W solution (U-BOOT)	Lecce
		Test the Malargue solution	Grenoble
29	Clock adjustment	Update the BoM	Grenoble
32	Test points	Provide the list of needed test points	KIT
33	Two SC S/W modes	Adapt the SC S/W	Wuppertal
36	3.3V switch for I2C slaves	Adapt the SC S/W	Wuppertal
39	Polarity inversion issue	Verify and valid	ALL
44	I2C issue	Test the SC DAC solution	Grenoble, Wuppertal
		Implement and test the 2nd I2C port	Lecce
		To understand the FPGA I2C ports behavior	ALL
11	RFI Filters on main 24V	Confirm the reference of the component	Radio Group
47	RFI Filters on Dig. Con.	Propose a reference of component	Radio Group
48	Radio Project requests	Investigate the best configuration adapted and to send components references	Radio Group
		Investigate coil shielding possibility on PCB	Grenoble
37	Radio Project requests	Investigate the best configuration adapted and to send components references	Radio Group
53	Radio Project requests	Investigate the best configuration adapted and to send components references	Radio Group
52	Fuse on PMTs power	Define the range	Malargue
30	Front panel dust cover	Investigate conductive material or coating	Malargue

5 ANNEX - VIEWGRAPHS

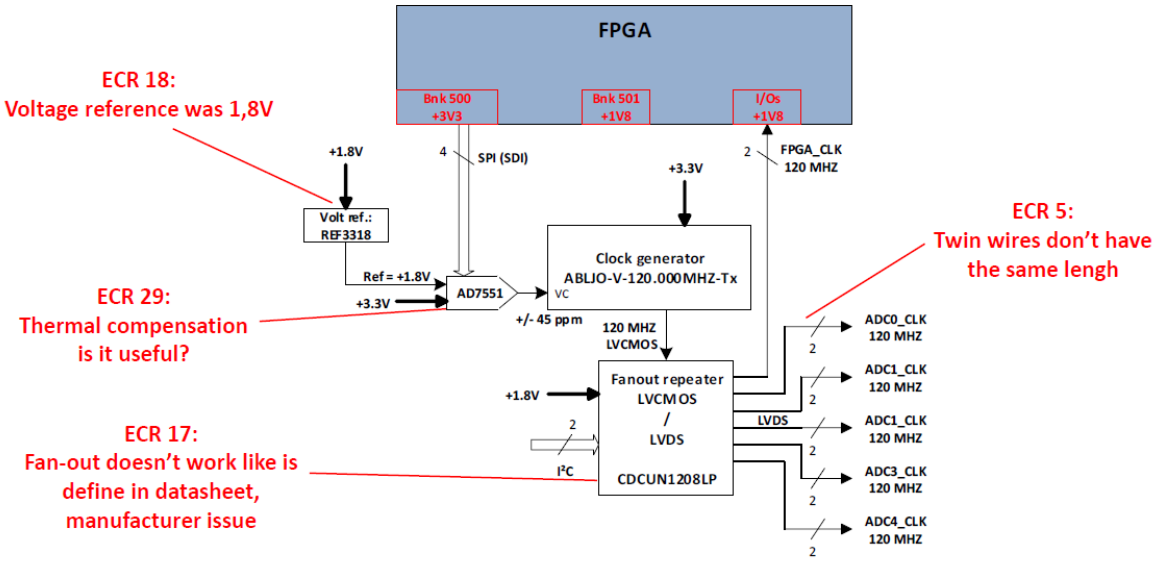
The following viewgraph add more information about some critical ECRs.

ECR 3:

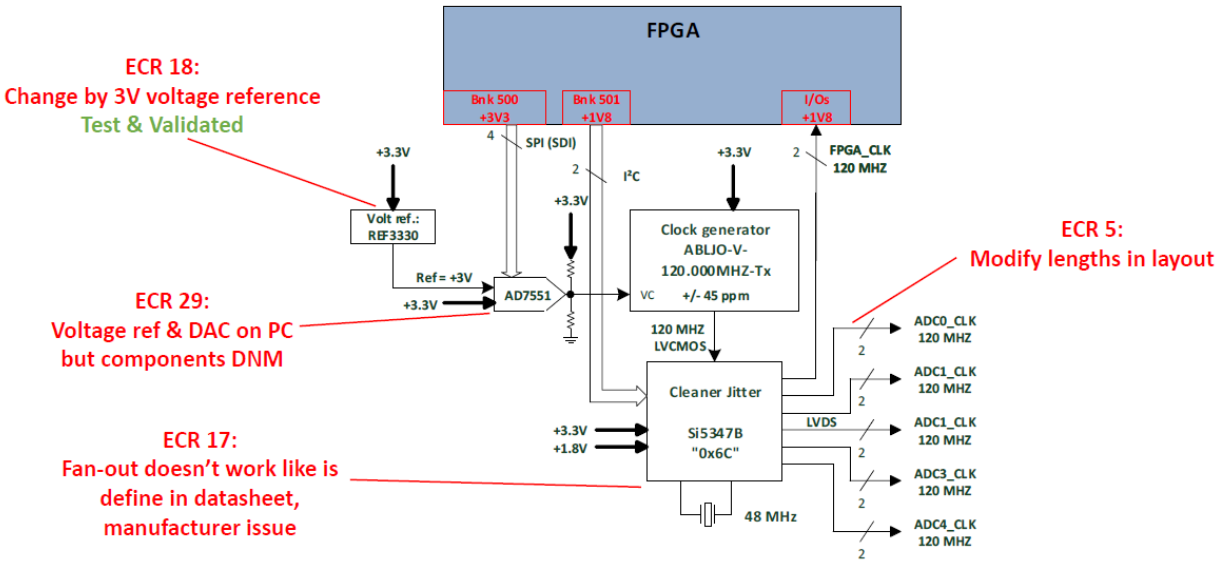


ECRs 17 & 29:

Present V2.0 Schematic:

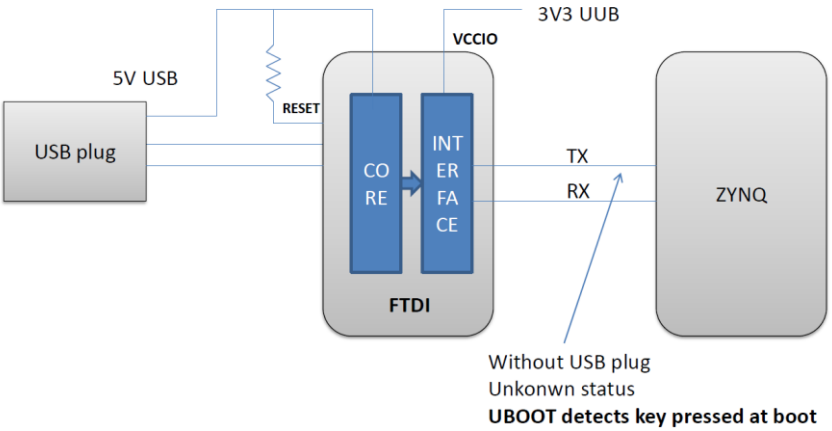


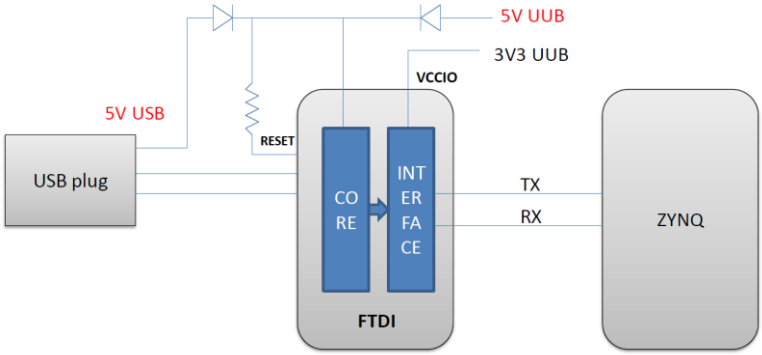
Next V3.0 Schematic:

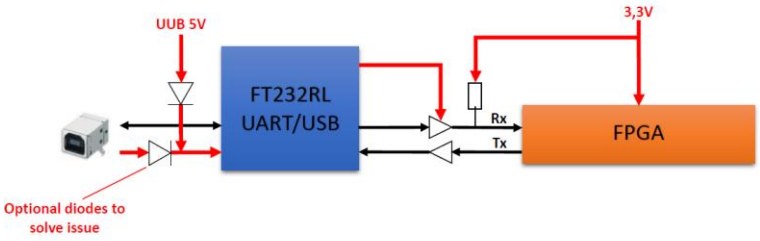


- The Fan-out is changed by a solution already test and validated: **Jitter Cleaner**
- Thermal frequency compensation useless: Time tagging function already integrated -/+ 45ppm tolerance

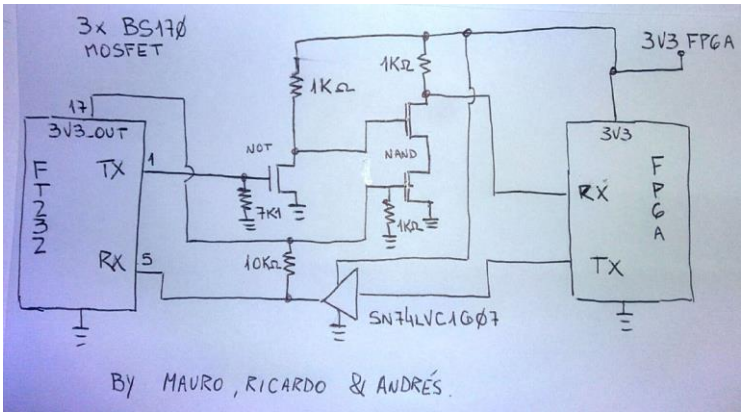
ECR 20:





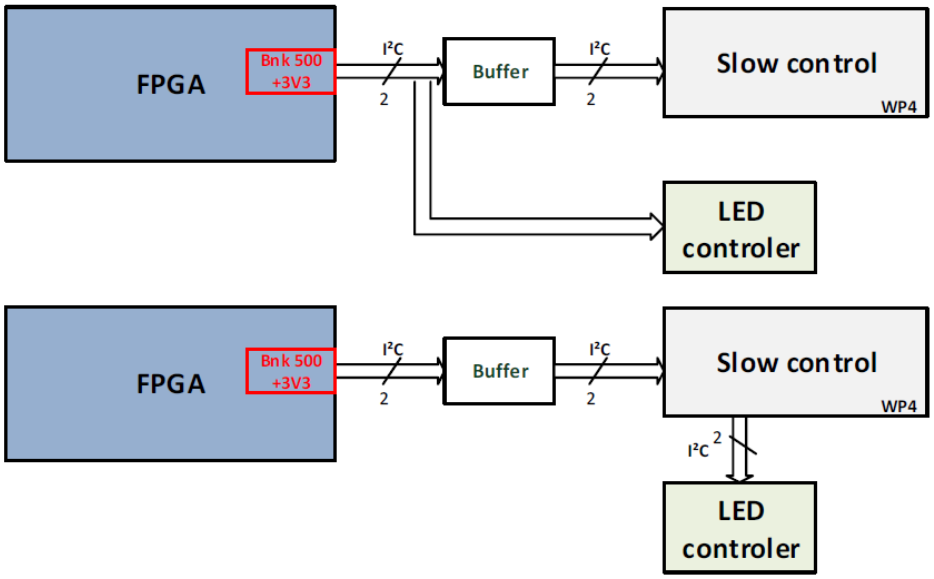


Buffer open-drain must be added for FPGA protection. VCCIO pin powered by UUB 3,3V, it's not enough.



ECR 44:

I²C communication with LED DAC problem generates Watchdog restarts the UUB



2 available channel in Slow-control could be used for LED-controller