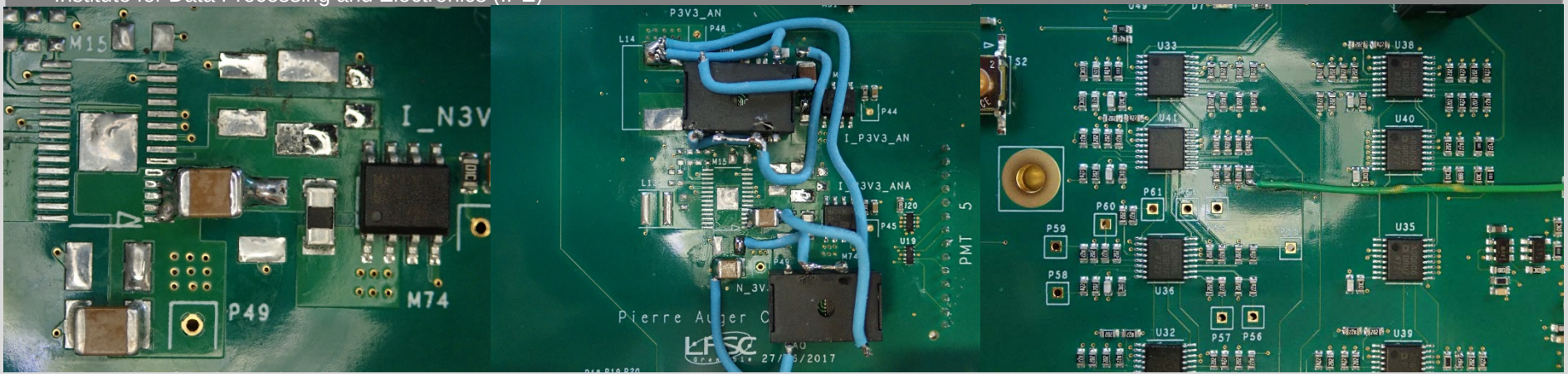
Production Test: changes for UUB V3

Matthias Kleifges and Fridtjof Feldbusch
prepared for SDEU meeting, Orsay 13-14 December, 2018

Institute for Data Processing and Electronics (IPE)



Important changes in HW for UUB V3:

- Mount preprogrammed flash memory IC
  - agreed that it will be done, ECR # 35
  - Eric / Patrick check with distributor of flash IC
  - preprogramming of MSP430 not required, but might be helpful
- Common MSP code (for “test” and “field” mode)
  - agreement on jumper (closed for “test” / open for “field” mode), ECR # 33
  - solution can be verified by K.H.B. by simple modification of UUB V2
- Test points for scope measurement of saw tooth signals from DAC
  - agreed, ECR # 32
  - DAC in future under MSP control? → program of saw tooth changes
  - simple procedure to generate saw tooth for LED DAC(s)

Changes of test procedure UUB V3:

- automatic verification of over/under voltage limiter by Python script
  - already tested with 2 types of power supplies
- automatic recording of DVM values through serial interface
  - implanted & tested for several type of Digital Voltmeters (DVM)
- test also radio interface via Rx/Tx loop-back adapter
  - need test software (similar to GPS) (provided by Fabio?)
- include interface to TPCB in test procedure
  - need discussion with K.H.B. how to do adapter
- include test of digital interfaces (separate)
  - similar code like Dave, simple yes/no decision
- verify “reset” functionality with push button and from radio reset

Proposal to change scope server

- buttons to display Low gain or High gain channels
- calculation of offset and noise from pre-signal window
- “save” button to record noise & offset & trace into database

■ HG ■ LG ■ Save data

New buttons

Chn:	offset	/	noise	/	max	okay
# 2 :	150	/	2.5		2753	yes / yes /yes
# 4 :	200	/	1.5		2745	No / yes /yes
# 6 :	100	/	1.5		2761	yes /yes / yes
# 10:	153	/	3.5		2748	yes / No / yes

System at the manufacturer:

- KIT procures components for 3 test systems:
  - 2 systems at manufacturer, 1 @ KIT
- Systems comprises of:
  - Lecce box & cable → provided
  - test jig and adapters → provided
  - Power supply → might be provided
  - DVM → needs to be agreed on
  - PC with software → provided
  - PC screen → by manufacturer
  - programming cables, etc → provided

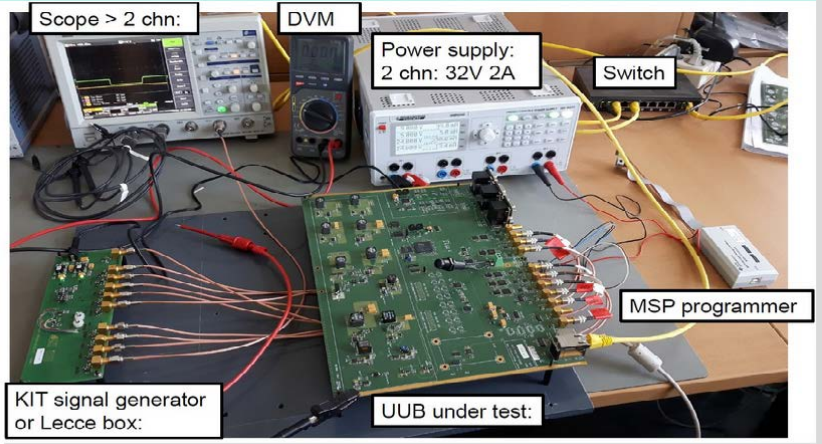


Fig. 1: Test set-up

Other test issues:

- Prague test with climate chamber:
  - important to give a few V3 board to Prague to verify procedure
  - decision on coating the V3 boards
  - decision on gluing heat sink in Malargüe / type of glue
- Siegen test system
  - 1x system at Malargüe for end test before deployment
  - 1x system at Prague for possibility of detailed investigation
  - 1x system at Malargüe for error tracking / repair
- We need to gain more experience with these other systems

Backup slides

web based test procedure: step 1

Karlsruhe Institute of Technology

AUGER PRIME UUBS | UUBs | Tests | History | Dokuments | Staff | Institutes | Manufacturer

Board no 0061

1. Optical inspection of solder points and correct position of components

Optical inspection not done

2. Mount fuse holder
3. Check for short circuits against ground with voltmeter (DVM) at the following test points (see Fig. 2)

Test point 1, P36 (1 V)	not done
Test point 2, P41 (1.2 V)	not done
Test point 3, P42 (1.8 V)	not done
Test point 4, P36 (3.3 V)	not done
Test point 5, P48 (+3.3 V)	not done
Test point 6, P34 (3.3 V SC)	not done
Test point 7, P49 (-3.3 V)	not done
Test point 8, P35 (5 V)	not done
Test point 9, P27 (12 V Radio)	not done
Test point 10, P29 (12 V PMT)	not done
Test point 15, P30 (10 V)	not done
Test point 16, P7 (3 V)	not done

4. Plug in loop-back adaptors at backside (see figure 5)
5. Plug in power connector (24V, current limit initially at 50mA, when all voltages OK, increase to 550mA)

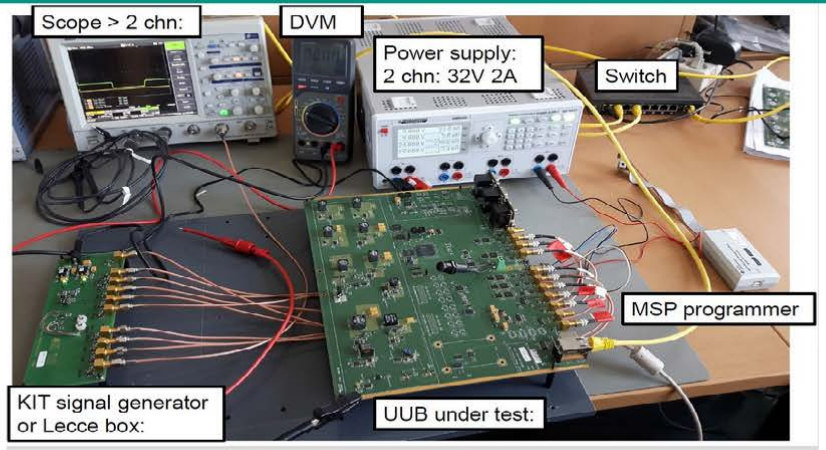
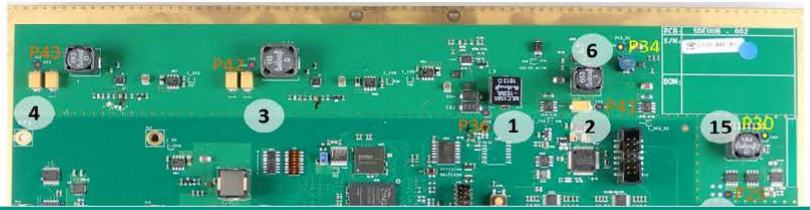


Fig. 1: Test set-up



AUGER PRIME UUBS UUBs Tests History Dokuments Staff Institutes Manufacturer

5. Plug in power connector (24V, current limit initially at 50mA, when all voltages OK, increase to 550mA)
6. Check voltages with voltmeter (DVM)

After having used the AutoTestUUB program, paste content of the clipboard into the text field below

```
Power measurements
3.3V   3.298 V
10V    10.22 V
24V    23,95 V
24V LED 23,95 V
SwitchOffMin 19.154 V
SwitchOnMin  19.953 V
SwitchOffMax 30.053 V
SwitchOnMax  29.804 V
```

Press the button to sort the values within the text into the form fields

Transfer voltage values

Values of AutoTestUUB:

3.3 V slow control voltage at test point 6, P34	3.298
10 V intermediate voltage at test point 15 P 30	10.22
24 Vin input voltage at test point 13, P25	23,95
24 V LED voltage at test point 14, P26	23,95

6. Test Battery Protection (switch-off voltages):
   - power consumption: ~20 mA
   - vary voltage range to switch-off voltage (turns off at ~19V and ~30V)

Switch off min [V]	19.154
Switch on after min [V]	19.953
Switch off max [V]	30.053
Switch on after max [V]	29.804

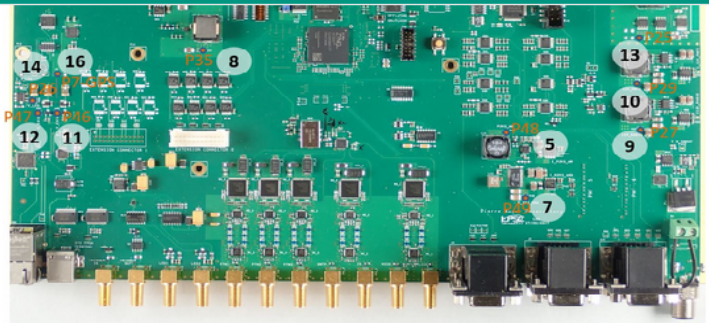


Fig. 2: Test points for voltage measurements (click to enlarge)

New:

- readout of DVM values via RS232 interface
- software controlled PS to verify battery limits

Step 2:

- verify supply voltage
- test battery protection

8. Connect the MSP-programmer MSP-FET430UIF to USB-Debug-Interface at Port J11
9. Program the MSP430
   - Execute Sde_sc_2V2_test.bat to program the MSP with a test version of the slow control, where all voltages initialliy are switched off.
   - When successful, turn off UUB, unplug MSP-FET430UIF, plug in USB at lower J8
   - Turn on UUB
   - Open Tera Term terminal or equivalent (baud rate 9600)
   - Turn on voltages in order, check voltages in display. Error messages for voltages that are either off or with a deviation of >5%. (see p commands in Tab. 1)

Copy and paste output of slow conhtrol command 'a' below

Paste slow control output here ...

Press the button to sort the values within the text into the form fields

Transfer voltage and current values

Values of command 'a' measured by MSP430:

1.0 V power in mV	
1.2 V power in mV	
1.8 V power in mV	
3.3 V power in mV	
+3.3 V power in mV	
-3.3 V power in mV (without sign)	
5.0 V power in mV	

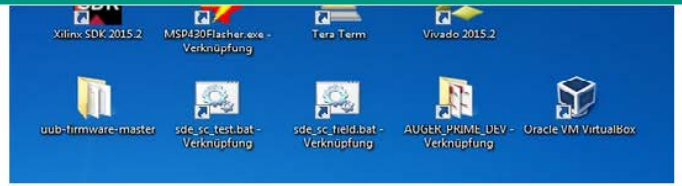


Fig. 3: Required software tools on the PC

Fig. 4: Test connectors for the photo multiplier tubes at the front (PMT)

Karlsruhe Institute of Technology

Step 3:

- program MSP µ-controller
- verify supply voltage
- test external interfaces

Setup Zynq-FPGA

12. Program the Zynq-FPGA:
    - Connect USB-JTAG programming cable (Digilent) on J10
    - Connect USB cable on upper port at "SYS FPGA Terminal"
    - Connect Ethernet cable on CO1
    - Jumper (S3) must be OPEN
    - On your PC open Oracle VM VirtualBox, start Petalinux (pw: auger2016) Home -> tftboot contains all files required. The file permission must be set to readable for everyone
    - Turn on UUB
    - Launch Xilinx SDK and select "Program flash" from Xilinx Tools menu
    - Check uboot.bin is selected (see Fig. 6). You could also program uub.bin directly but this takes 45 min
    - Click "Program" to store file into flash
    - Turn off UUB and turn on UUB again: U-boot will start from flash
    - Open Tera Term (baud rate 115200)
    - Check if Petalinux is running on terminal and type the following commands at prompt U-Boot-PetaLinux>:
        - **`set serverip 192.168.1.4`**
        - **`set ipaddr 192.168.1.5`**
        - **`run flash-uub`** (a custom command under u-boot to update the flash memory partitions).
    - Uub.bin is stored into the flash memory. Turn off/on UUB
    - Login as "root", password: root
    - Write: **`makeflash`** and await response, when finished, reboot the UUB (makeflash creates the flash volume in MTD3)
    - Check if D_4 Diode is on (FPGA flash done)

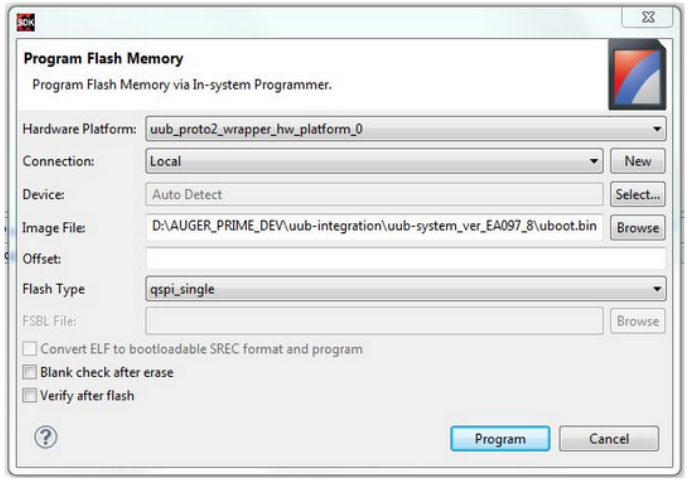


Fig. 6: SDK for programming 'uboot.bin'

```
Load address: 0x1000000
Loading: ##################################################################
##################################################################
##################################################################
##################################################################
946.3 KiB/s
done
Bytes transferred = 33554432 (3000000 hex)
device 0 offset 0x0, size 0x3000000
18481152 bytes written, 15073280 bytes skipped in 59.551s, speed 578524 B/s
U-Boot-PetaLinux>
```

Fig. 7: Peta-Linux after "flash-uub"

Karlsruhe Institute of Technology

Step 4: Program Flash memory

a. boot loader
b. final code

This step lasts 25 min or more.

AUGER PRIME UUBS

UUBs Tests History Dokuments Staff Institutes Manufacturer

13. FPGA-Tests

- Connect USB cable on upper port at "SYS FPGA Terminal"
- Connect Ethernet cable on CO1
- Jumper (S3) must be OPEN
- Insert GPS-adapter (see Fig. 10)
- Use a SMA cable and connect it to IN and OUT Trigger connectors
- Open the main menu of the UUB web server with 192.168.1.5/ in a new web broser window (see Fig.X)
- Choose icon "UUB Test" to open the test tools (see Fig. 9)

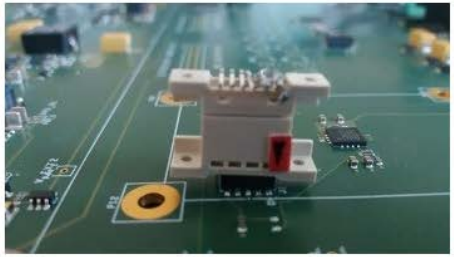
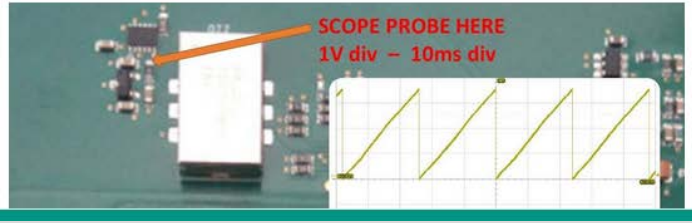


Fig. 10: GPS-Adapter

UART GPS loop OK? not done

- Select 'Test DAC7551 Clock DAC' in Test tools menu
- Use the scope (1V/div, 10ms/div) and check there is ramp signal (see Fig. 11).



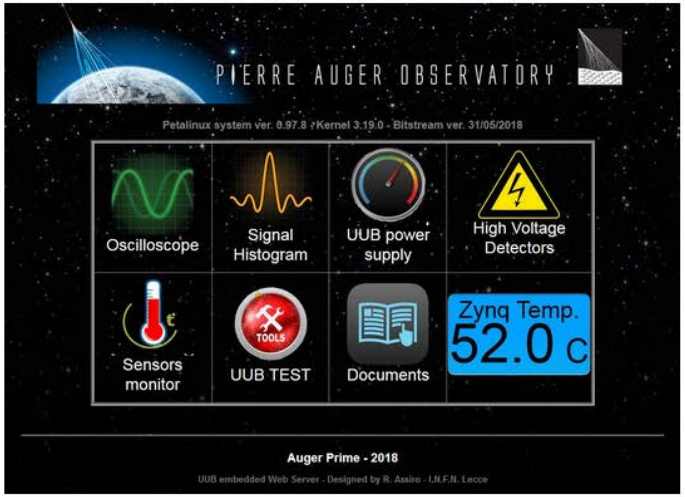
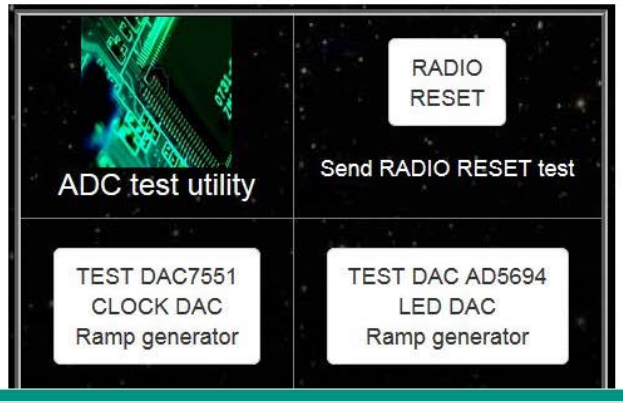


Fig. 8: Web server menu



Karlsruhe Institute of Technology

Step 5: Zync & FPGA

- GPS socket
- different DACs generate ramps
- LED flasher

14. Checks with the LLECCE box
    - Connect Ethernet cable on C01
    - Connect SMA cables from Lecce box
    - Turn on Lecce Box (15V power supply)
    - Turn on UUB
    - Start Browser and enter 192.168.1.5
    - Open 'Oscilloscope' in Web server menu and select FPGA Trigger in Trigger Mode Window
    - The switch at the LECCE-Box must be in down position (high pulses)
    - Turn off all channels and switch on one channel at a time to see whether the pulse exists (see figure 13)
    - Change the switch at the LECCE-Box into up position (low pulses)
    - Switch on all high channels and change trigger mode to 'AUTO internal + LED'
    - In 'Twins LED-Pulser' type '2000' into 'Amplitude 1' (see figure 14)
    - By plugging the LED-wire of the LECCE box once into LED1 connector and once into the LED2 connector you may check whether the LED output works.

LECCE test OK? not done

15. Press Reset-button of the UUB (button above the power connector)
    - The MSP begins to restart the board (LED D7 blinks faster)
    - After a while check whether LED D4 turns on

Reset test OK? not done

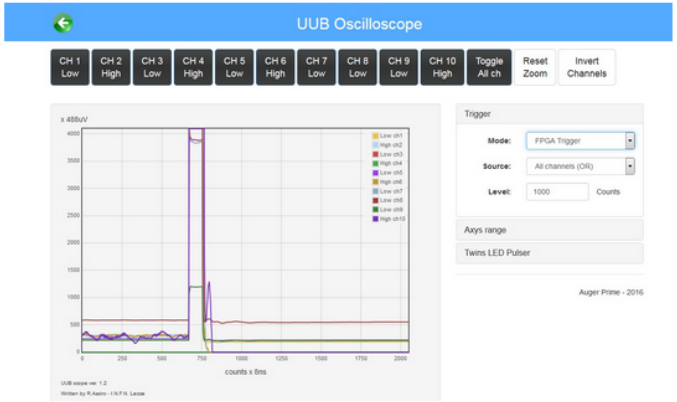


Fig. 13: The Web-Oscilloscope showing the test pulses of the Lecce-Box on different channels

Fig. 14: The Web-Oscilloscope showing the LED pulses on different channels

Karlsruhe Institute of Technology

Step 6: Frontend with UUB scope

- Low gain chn.
- High gain chn.
- LED flasher

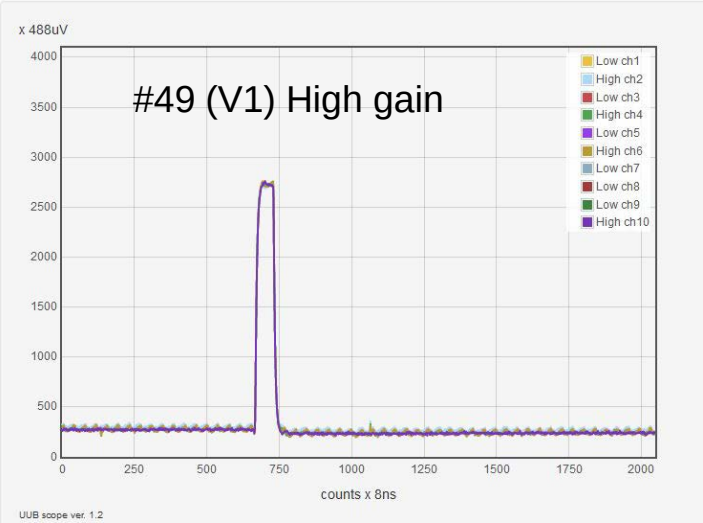
- verify gain, pedestal and noise
- check reset/restart

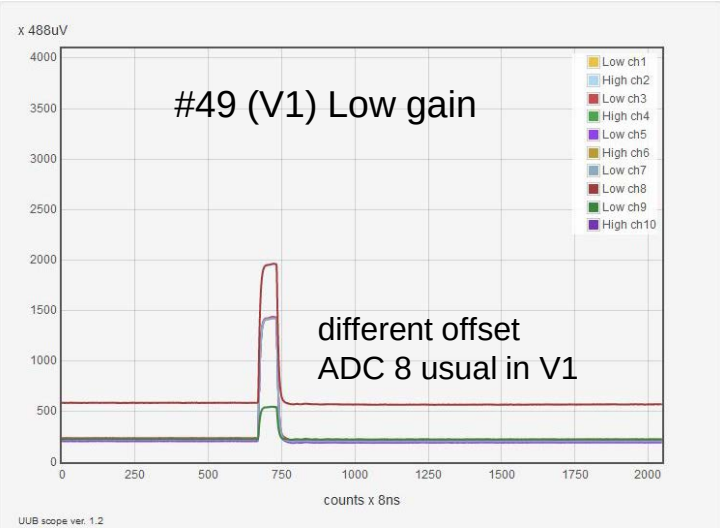
Proposals for Optimization and changes for V3

- Optimize duration of production test: goal 20-30 min/board
  - mount (already) programmed flash memories
  - automate the procedure (no manual reading of data) as much as possible
  - simplify some parts, avoid mouse clicks
- Production test with V3:
  - preparation of 2 test benches for test at manufacturer
  - apply procedure to “preproduction UUBs” (30 pcs?), fine tune details
- Documentation
  - current procedure described in *UUB-V2-Testprocedure.pdf*
  - more generic definition for production tender needed

Short test of UUB #49 (as of Aug. 1st, 2018)

- all ADC okay





Additional notes:

- cold start okay, board seems to be okay.

Gluing of heat sink

For comparison we have 3 options of gluing the heat sink:

- by acrylic adhesive that comes with the heat sink
  - UUB # 48, # 49, # 64
  - needs no curing time, no “dangerous good” problem with shipping
- by (2-compount) TBS20 glue from Electrolube
  - UUB # 65, # 66, # 67
  - needs 2 days of curing
- glued by glue from RS part # 725-9993
  - UUB # 68, #69, #70
  - needs few minutes days of curing