

UUB Test System Report

Auger Collaboration Meeting
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Bundesministerium
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Introduction

Tasks:

- Generate PMT signals and analyse the UUB high and low gain signals
- Receive and monitor PMT voltage signals associated with the slow control

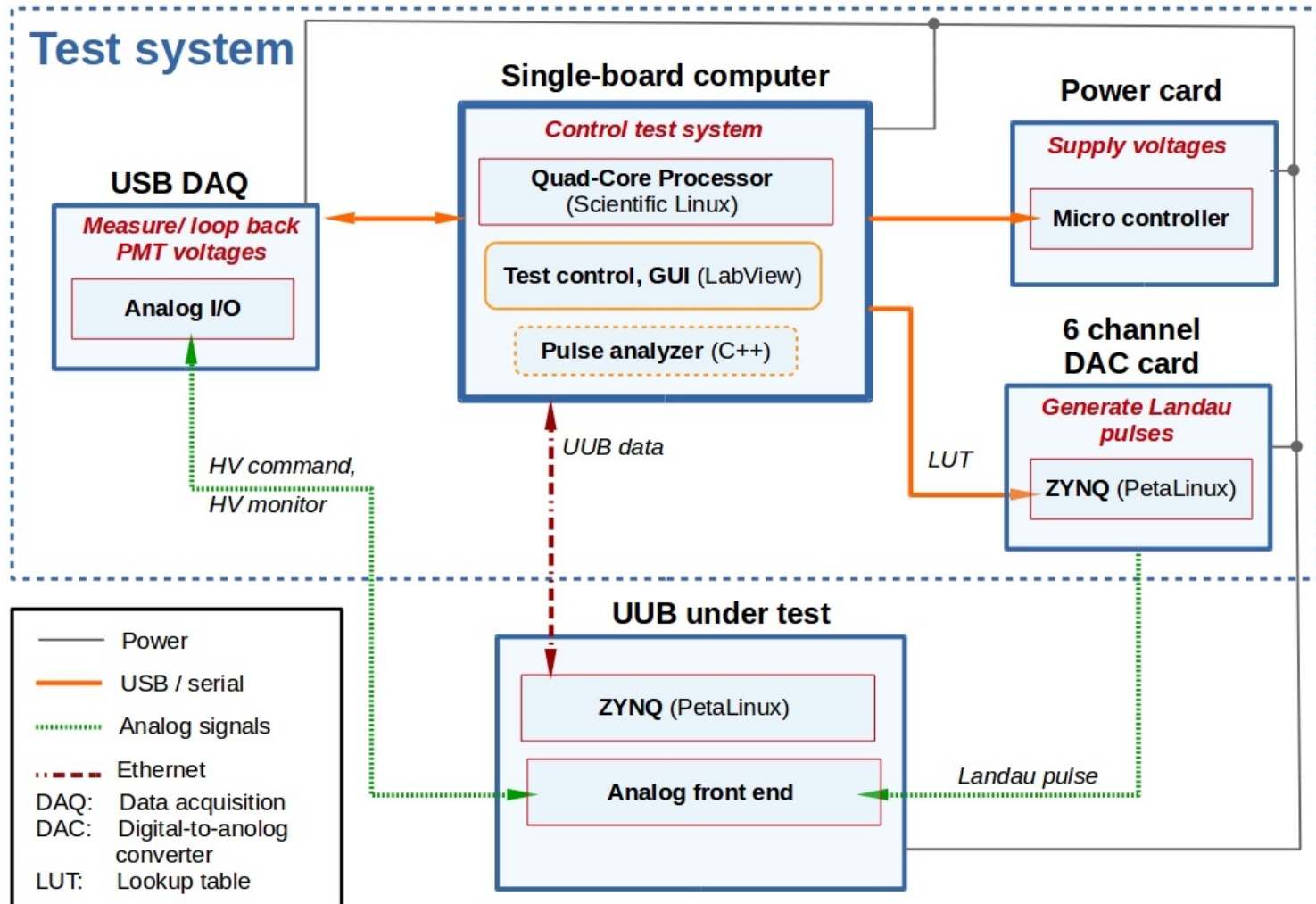
Concept:

- High speed DAC which allows to generate arbitrary pulse shapes

Test system runs with minimal lab infrastructure. Prerequisites:

- Monitor
- Mouse
- Keyboard

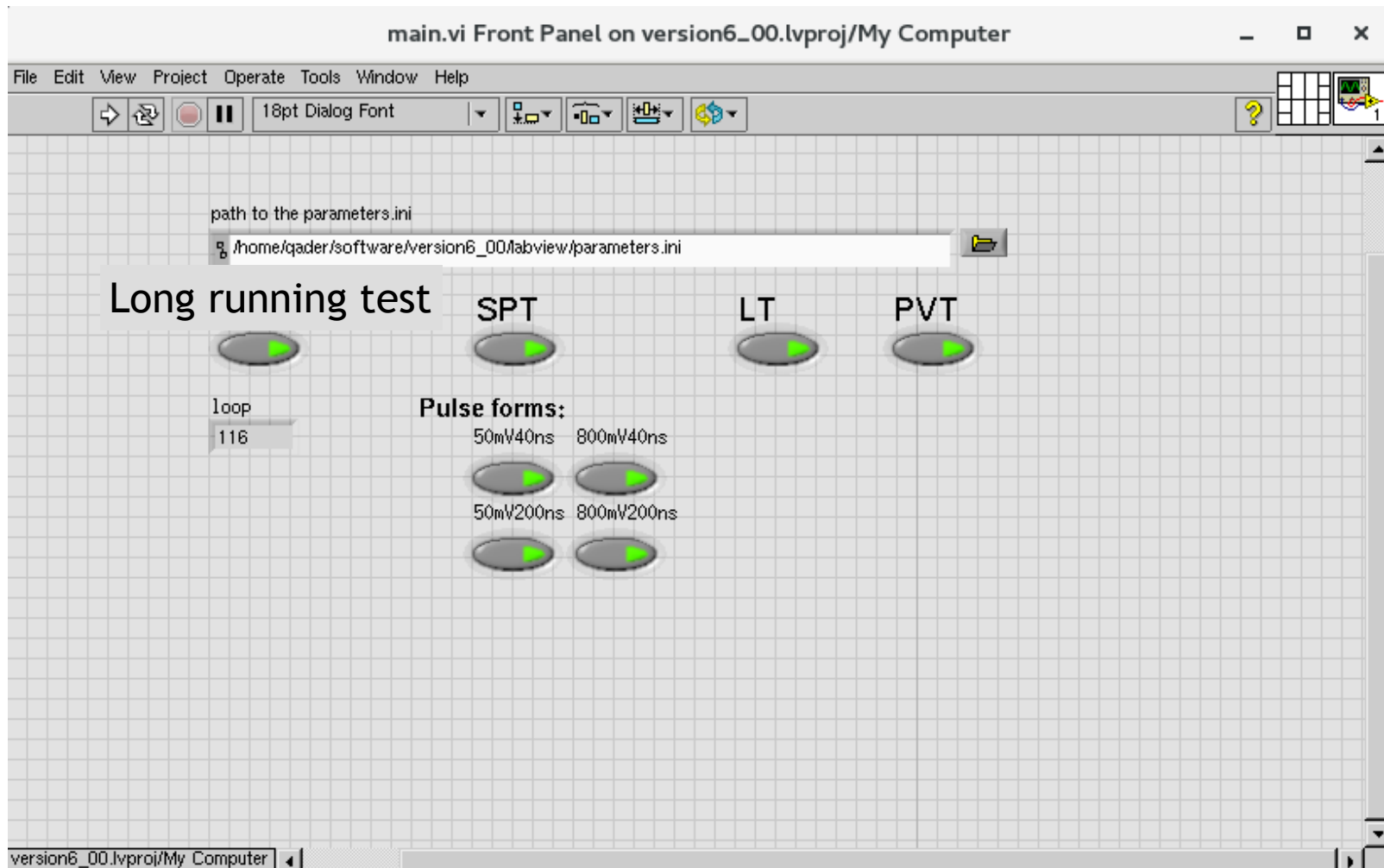
Design concept



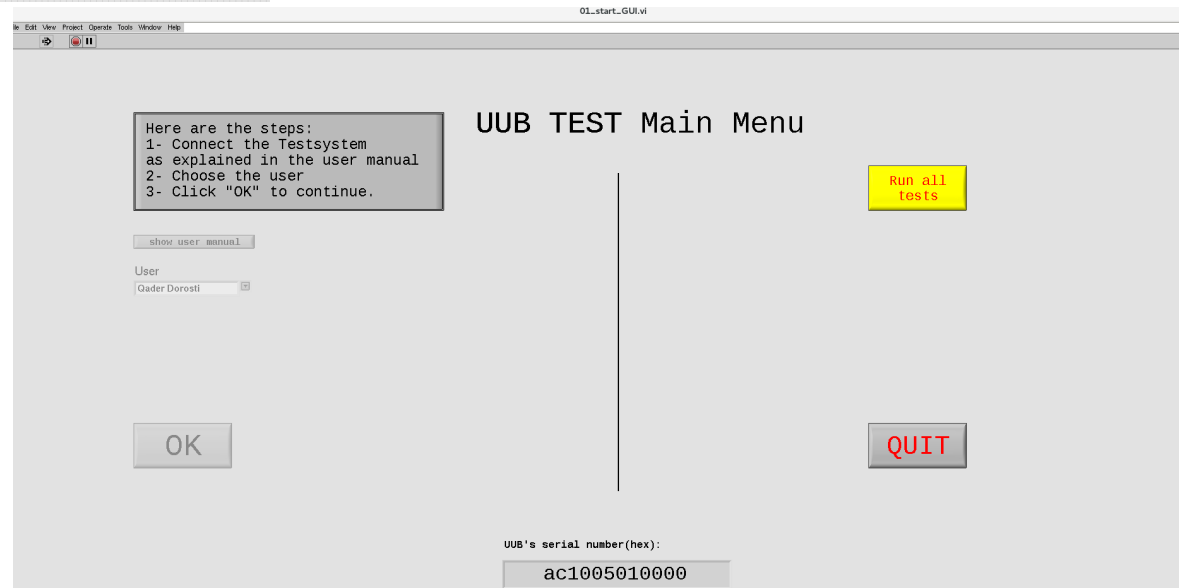
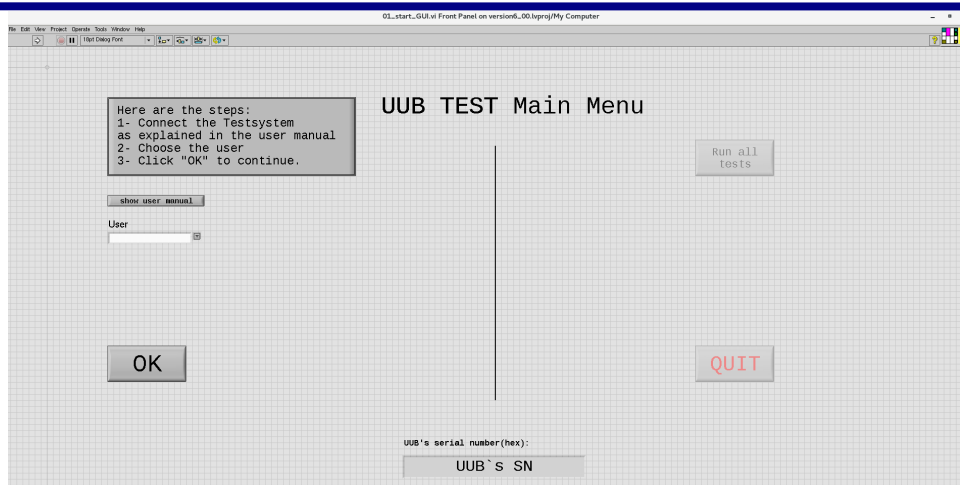
Test system



Main menu



Start GUI



The start GUI briefly instructs the user how to run the tests

Test system - single pulse test (SPT)

Test System Output (UUB Input):

- Landau shaped pulse, defined by a lookup table

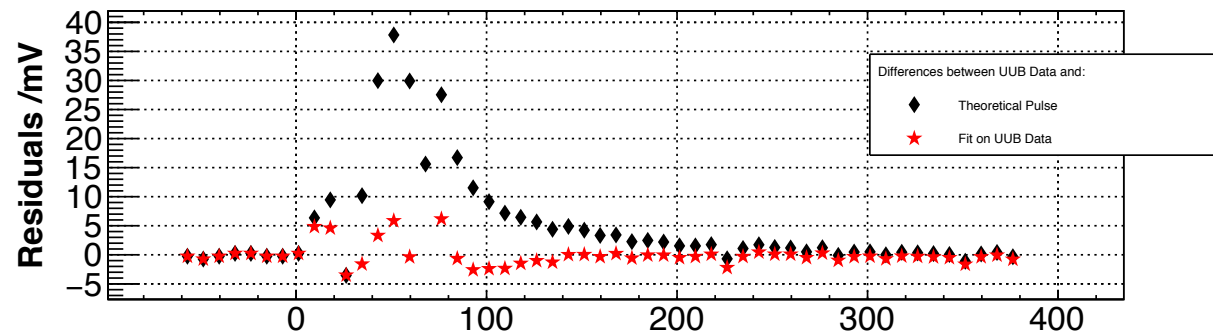
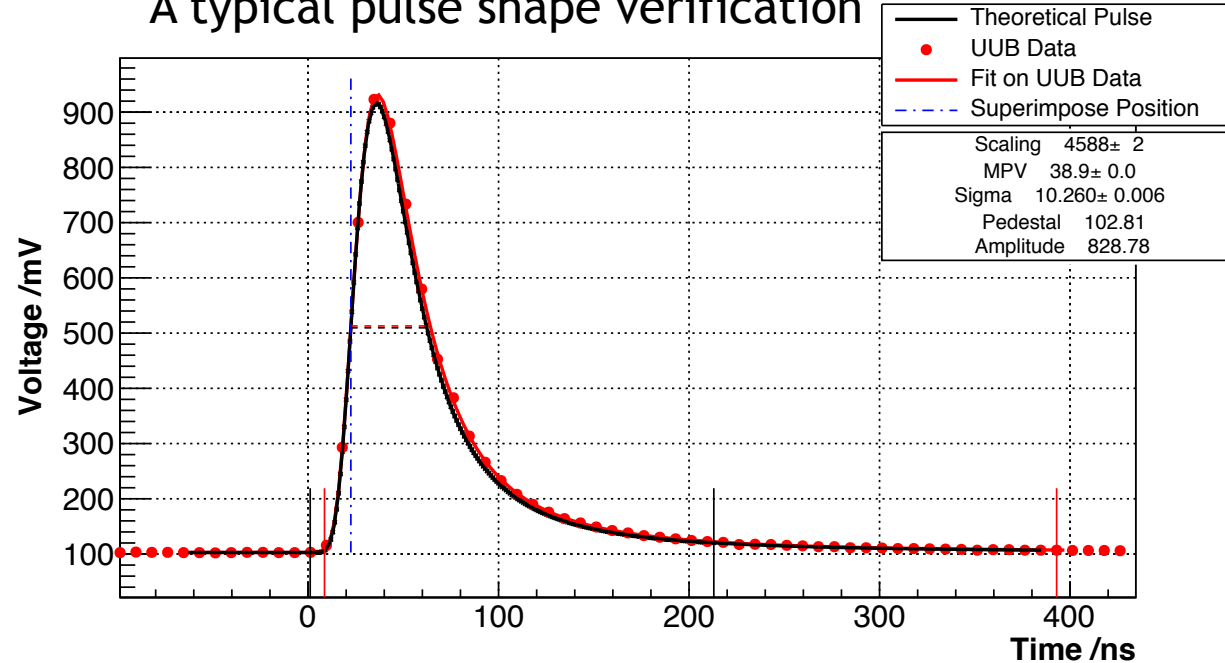
UUB Output:

- Read out by test system and automatically compared with original test system output

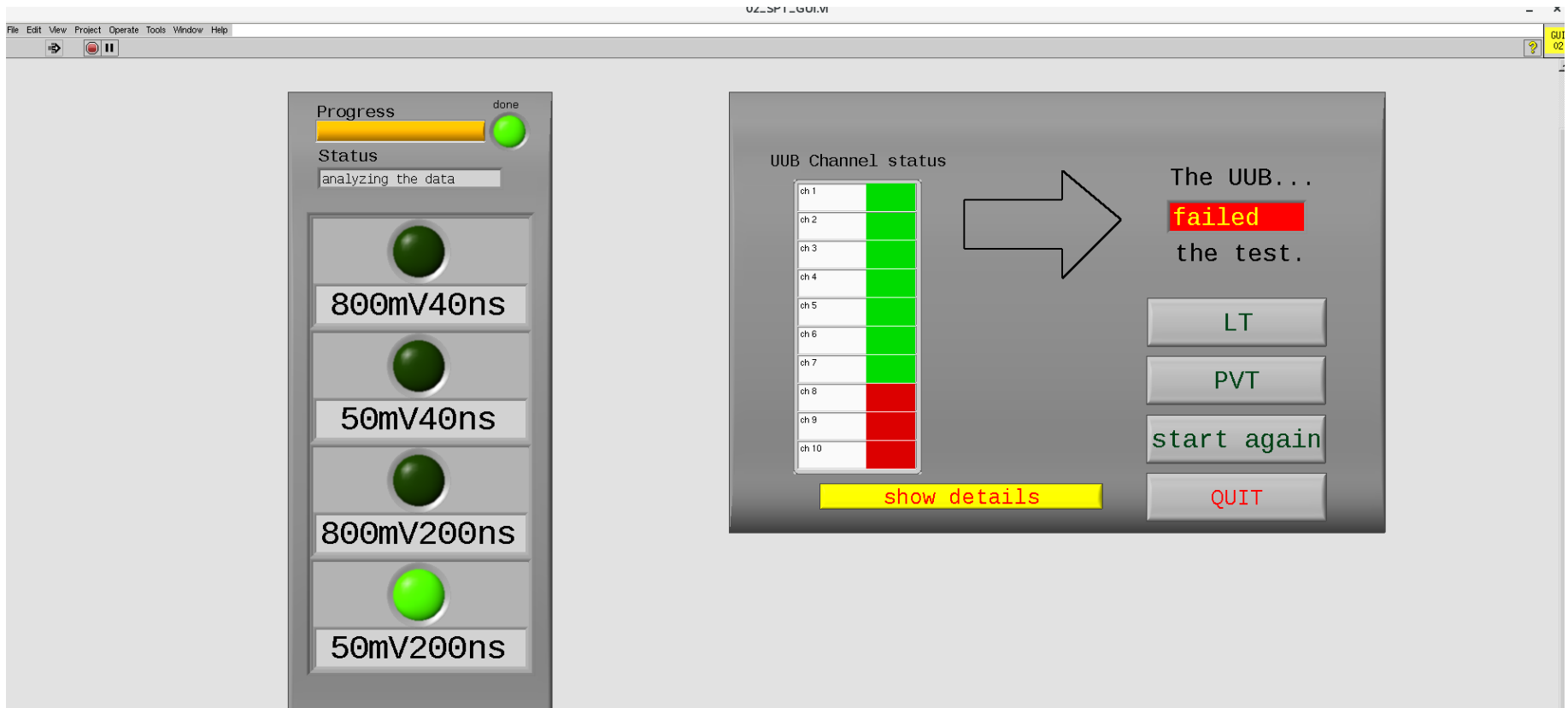
Pulse forms:

Amplitude (mV)	FWHM (ns)
800	40
50	40
800	200
50	200

A typical pulse shape verification

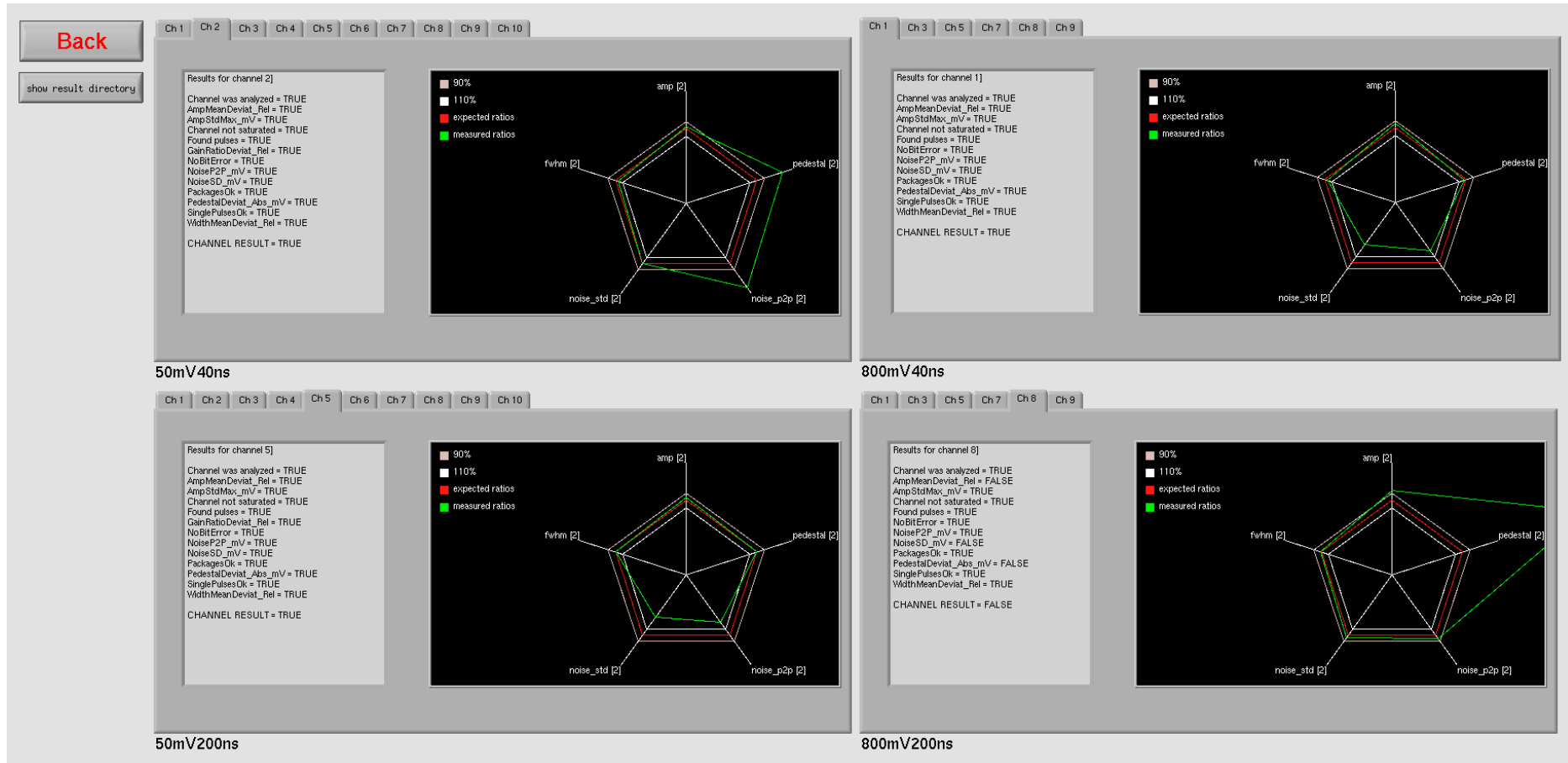


SPT GUI



The GUI indicates the SPT test result with LEDs

Detail GUI



- Detail GUI provides the user with spider plots
- All details are stored on the hard drive, that could be accessed during the test or later

PMT voltage test (PVT)

03_PVT_GUI.vi

File Edit View Project Operate Tools Window Help

instructions

Important! Before starting the test you have to follow the instructions below, in order to indicate whether PMT base voltages are available or not:
1- check the status of the LEIS on the front panel of the Testsystem
2- turn the LED status of the PMT Base voltage of this GUI accordingly, by clicking on each of them
3- push the start button

PMT 1 Base Voltage

PMT 2 Base Voltage

PMT 3 Base Voltage

PMT 4 Base Voltage

Start

done

PMT 1

500 1000 1500 2000

PMT 2

500 1000 1500 2000

PMT 3

500 1000 1500 2000

PMT 4

500 1000 1500 2000

Final PMT result

show details

start next test cycle

QUIT

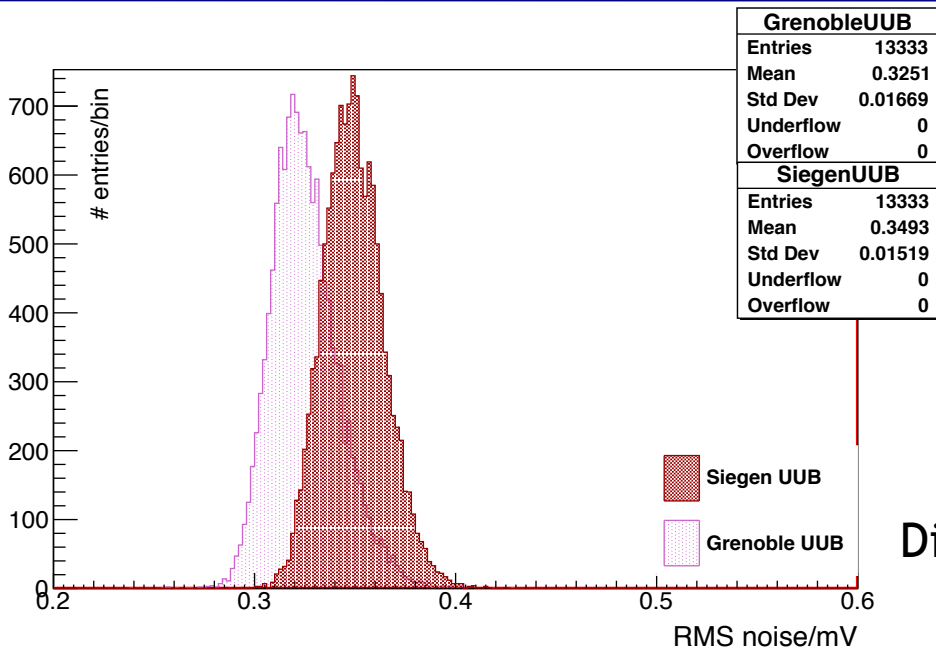
PVT tests the PMT base voltages and PMT high voltage command and high voltage monitor pins of the UUB PMT connectors

Some measurements with an UUB version 2 (Grenoble)

- The version 2 UUB was tested with the Siegen test system in Grenoble
- The UUB had a problem with clock fanout
 - some ADC channels missing some times, difficulty with booting FPGA
- Long running Single pulse tests (12 hours in a row), each 100 times, were performed on the UUB
- The pulses were Landau pulses of the following forms:

Amplitude (mV)	FWHM (ns)
800	40
50	40
800	200
50	200

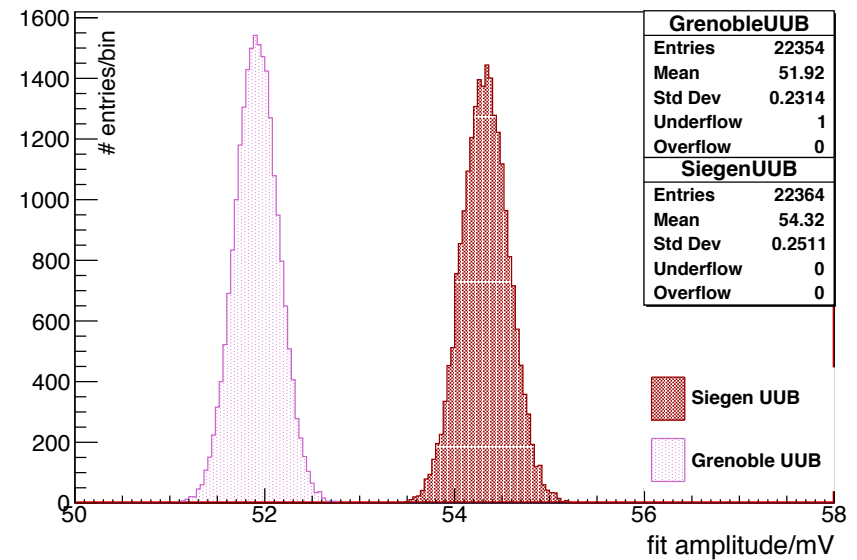
some comparisons between V1 & V2 UUBs



Preliminary

Siegen UUB: V1
Grenoble UUB: V2

Distribution of the pulse amplitudes



Test results (Preliminary)

Input pulse: 800 mV 40 ns

Distribution	Grenoble UUB (22368)		Siegen UUB (22388 pulses)	
	Mean	RMS	Mean	RMS
Ch1				
Fit amp/mV	829	0,24	875,7	0,52
FWHM/ns	41,3	0,024	38,36	0,045
Noise rms/mV	0,32	0,018	0,35	0,017

Input pulse: 50 mV 40 ns

Distribution	Grenoble UUB (22368)		Siegen UUB (53490 pulses)	
	Mean	std	Mean	std
Ch1				
Fit amp/mV	51,9	0,24	54,3	0,25
FWHM/ns	40,3	0,37	38,1	0,29
Noise rms/mV	0,32	0,016	0,35	0,015
Ch2				
Fit amp/mV	1656	3	1687	3,3
FWHM/ns	40,3	0,11	38,16	0,12
Noise rms/mV	5,1	0,7	5,4	0,43

The measurement suggests that the pulse overshooting problem has been suppressed

Summary

- The test system performs the following tests:
 - Generate PMT signals for all 3 PMTs and the small PMTs and SSD, and analyse the UUB high and low gain signals for each PMT
 - Generate wide range power supply voltages for the UUB
 - Receive and analyse PMT high voltage control and monitoring signals of the UUB

(For more detail, refer to **WP5-SIEGEN-01A** document)

- One test system is in Grenoble

Outlook

- An amplifier card has been produced to generate up to 8 V pulse amplitudes for SSD channel

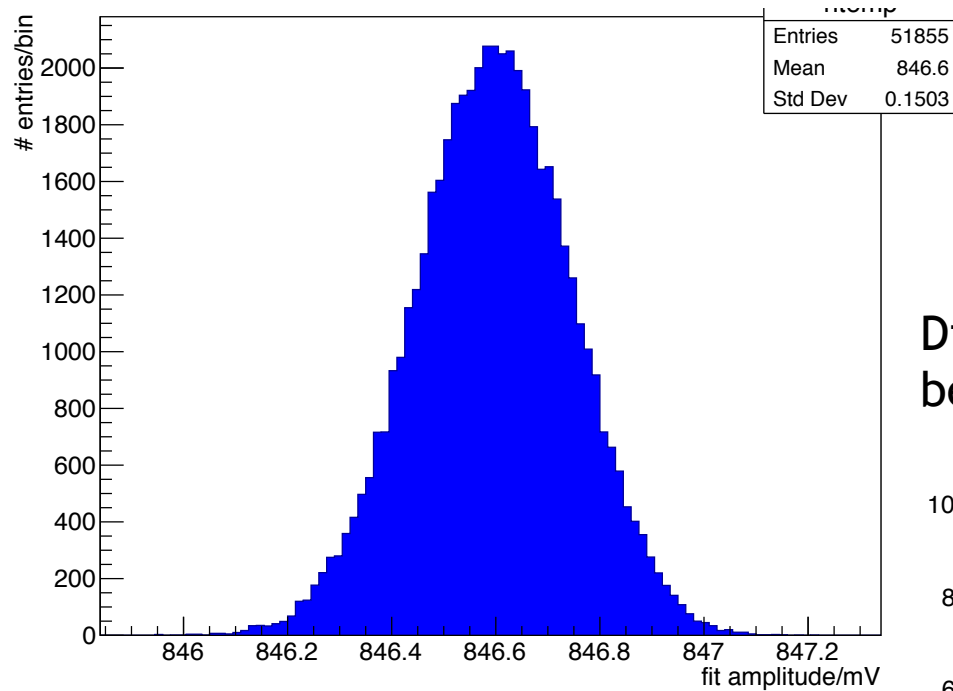
- Test system is in the mass production phase:
 - 4 test systems have been assembled
 - 2 more test system will be assembled by the end of this year

- The test system will be commissioned first in German labs (KIT/Wuppertal)

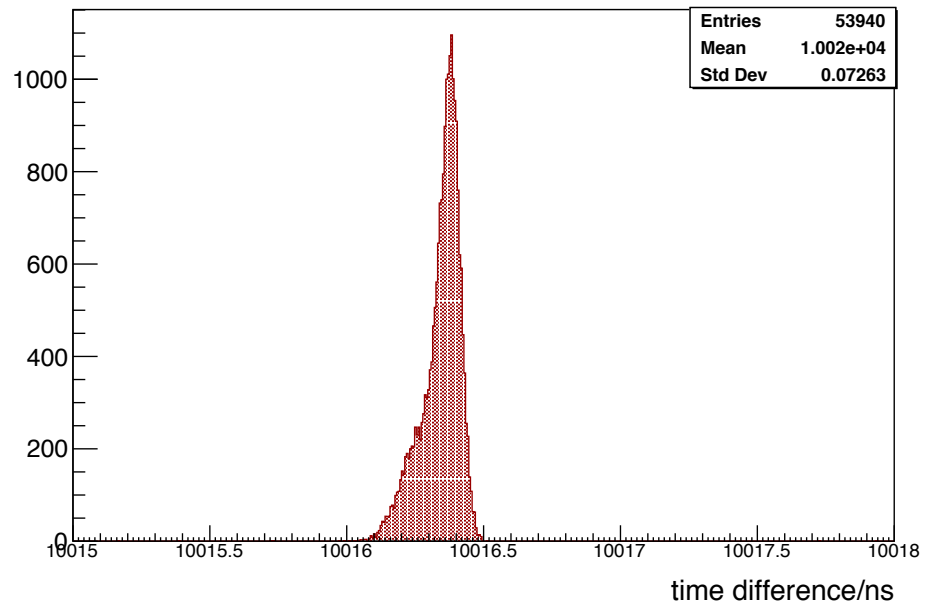
Backup slides

Distributions

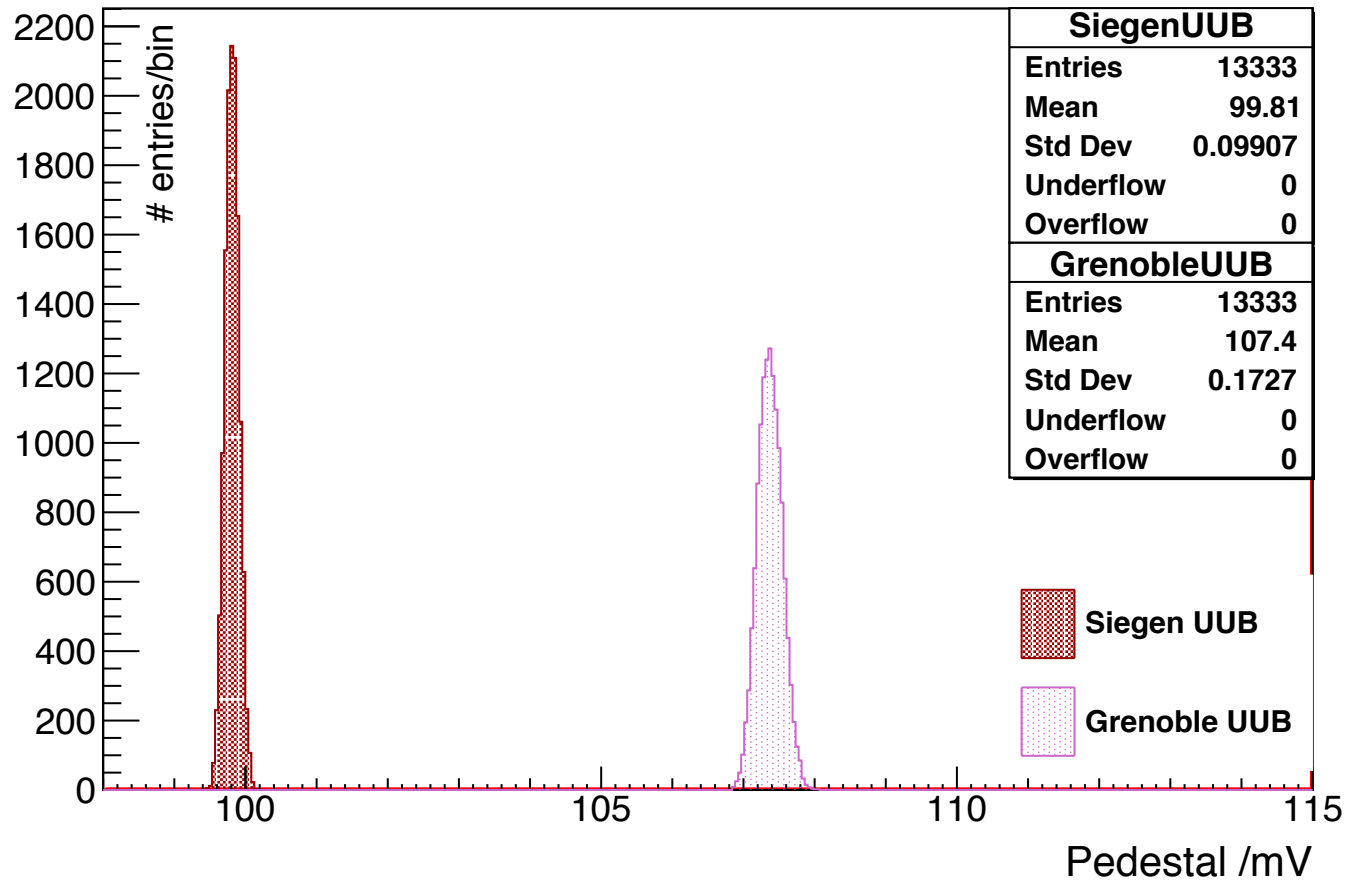
Measured pulse amplitude distribution for 800mV40ns pulses



Distribution of the measured time differences between consecutive pulses

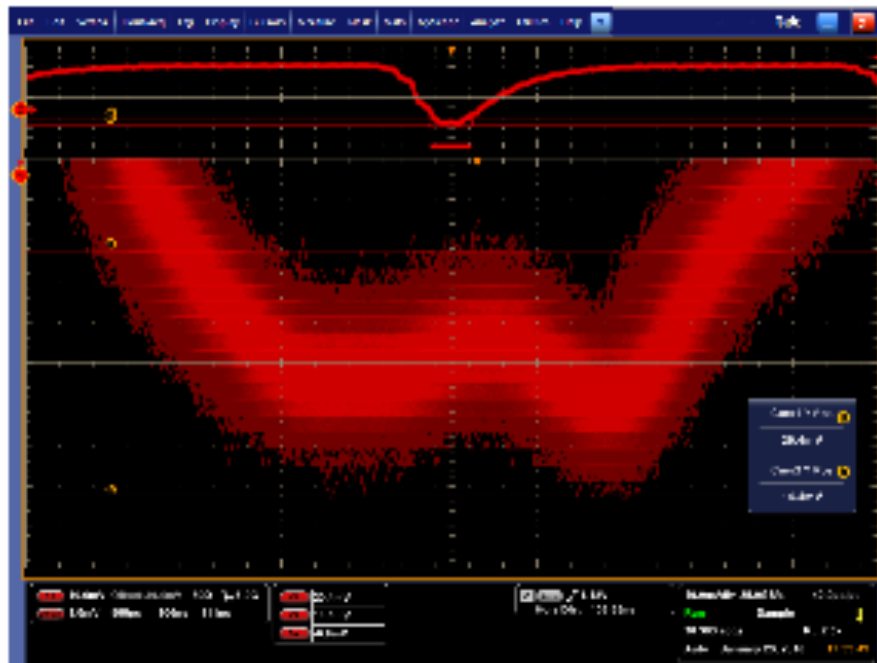


UUB pedestal comparison

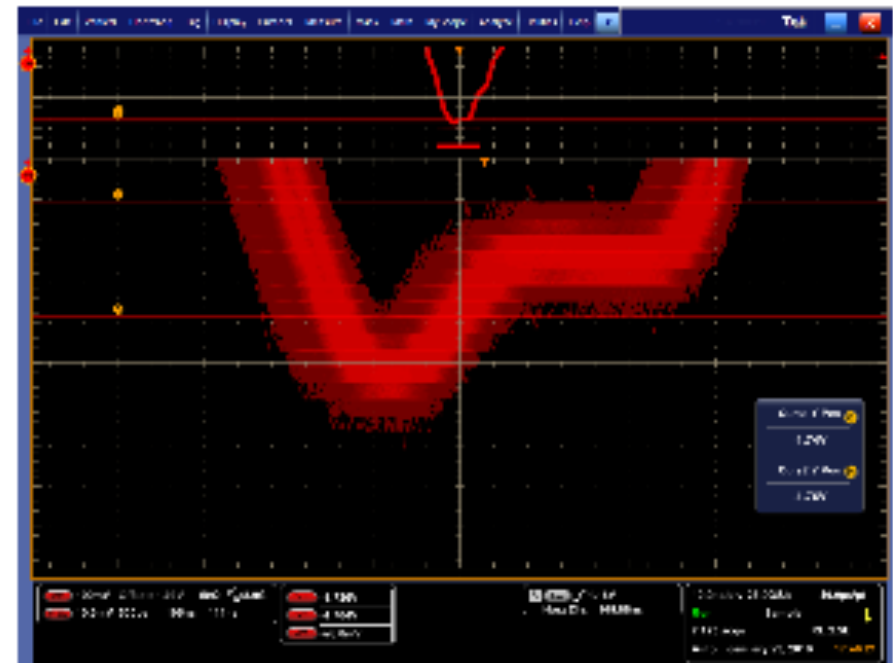


Test system - DAC noise

Several thousand two-peak-structure pulses with a width of 10 ns have been analyzed



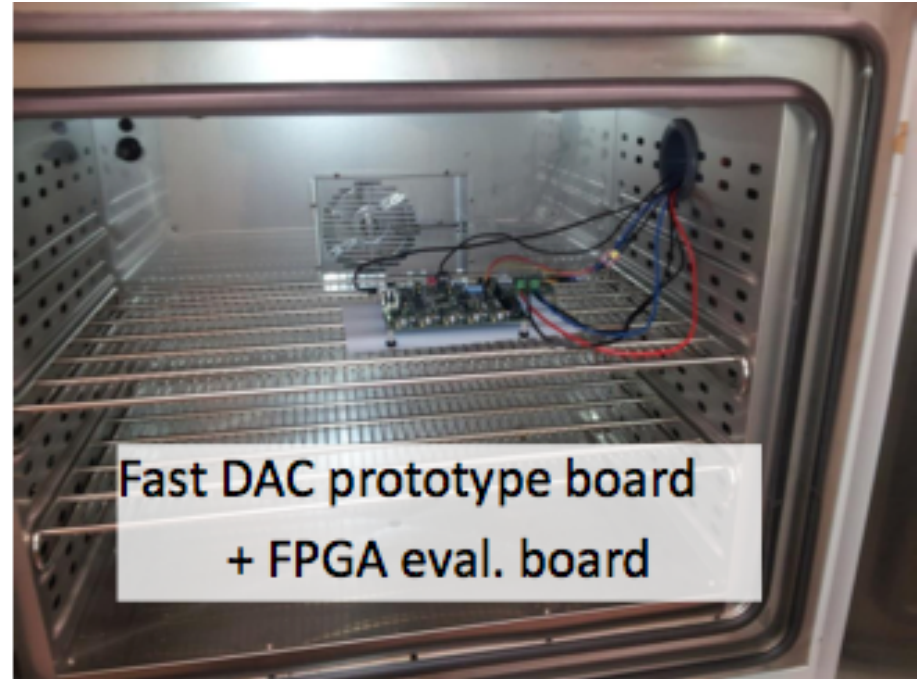
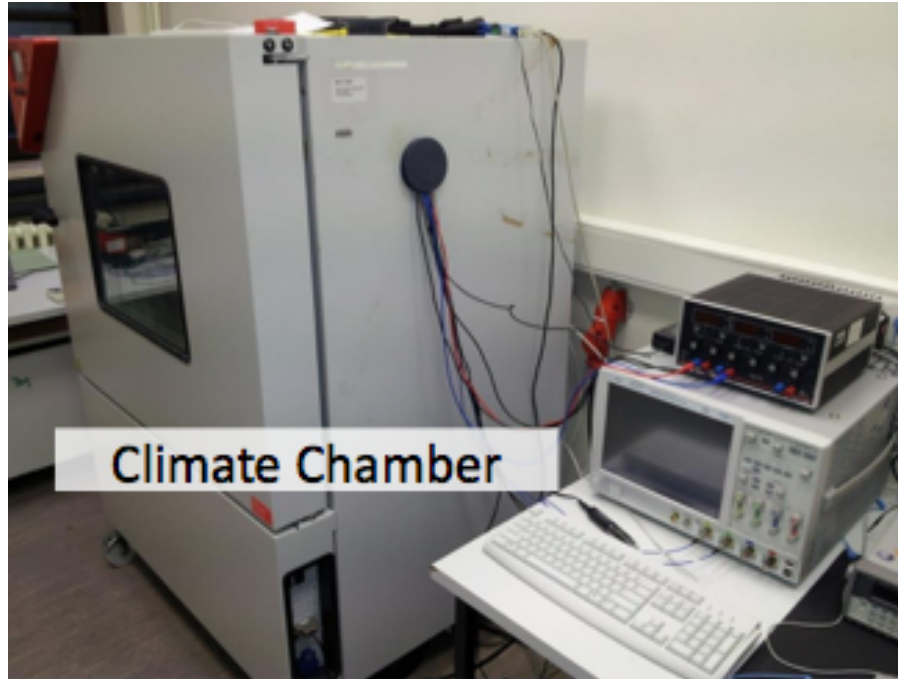
Peak voltage: 60 mV



Peak voltage: 1800 mV

Amplitude/mV	Noise (peak-peak)/mV	Noise RMS/mV
60	4.8	0.8
1800	28	4.7

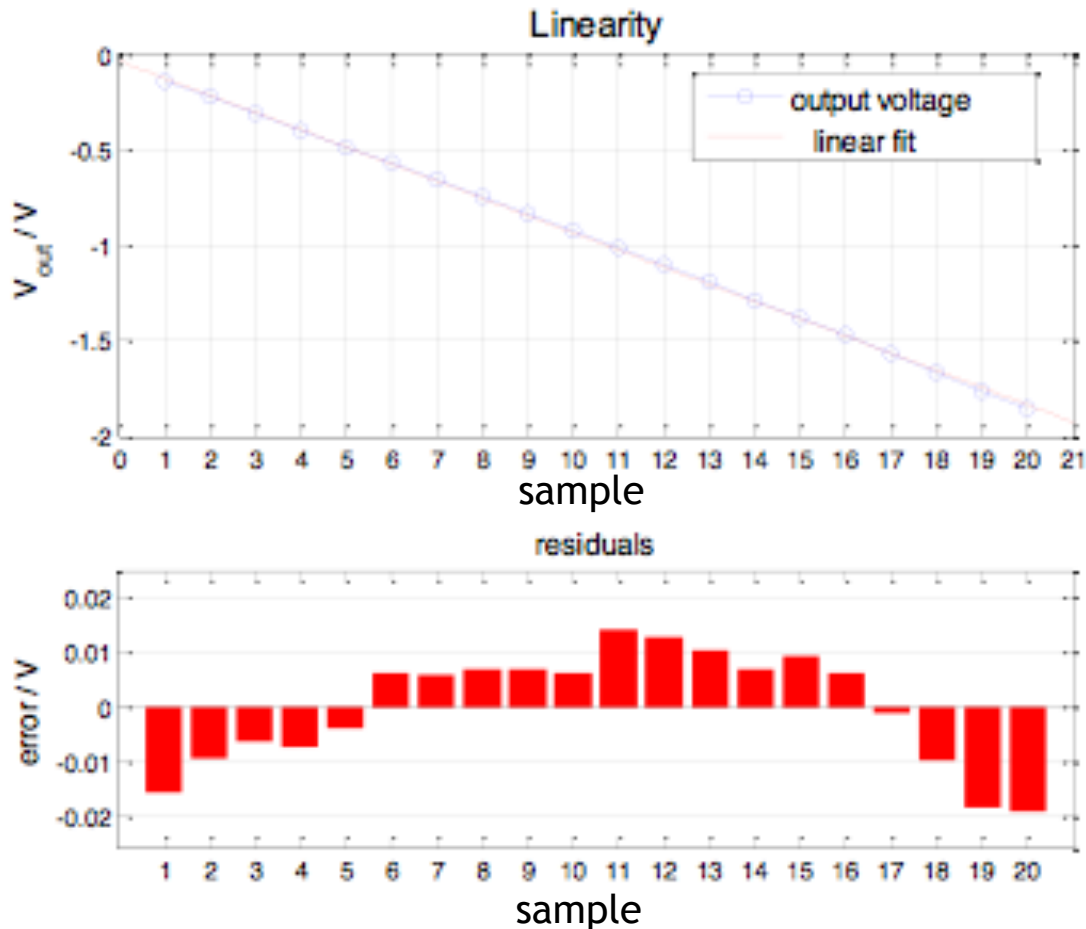
Test system - DAC temperature stability



Variation of the pulse shape at various temperatures (17°C , 27°C and 37°C)

→ a variation of the amplitudes of less than **0.5%** per 10°C

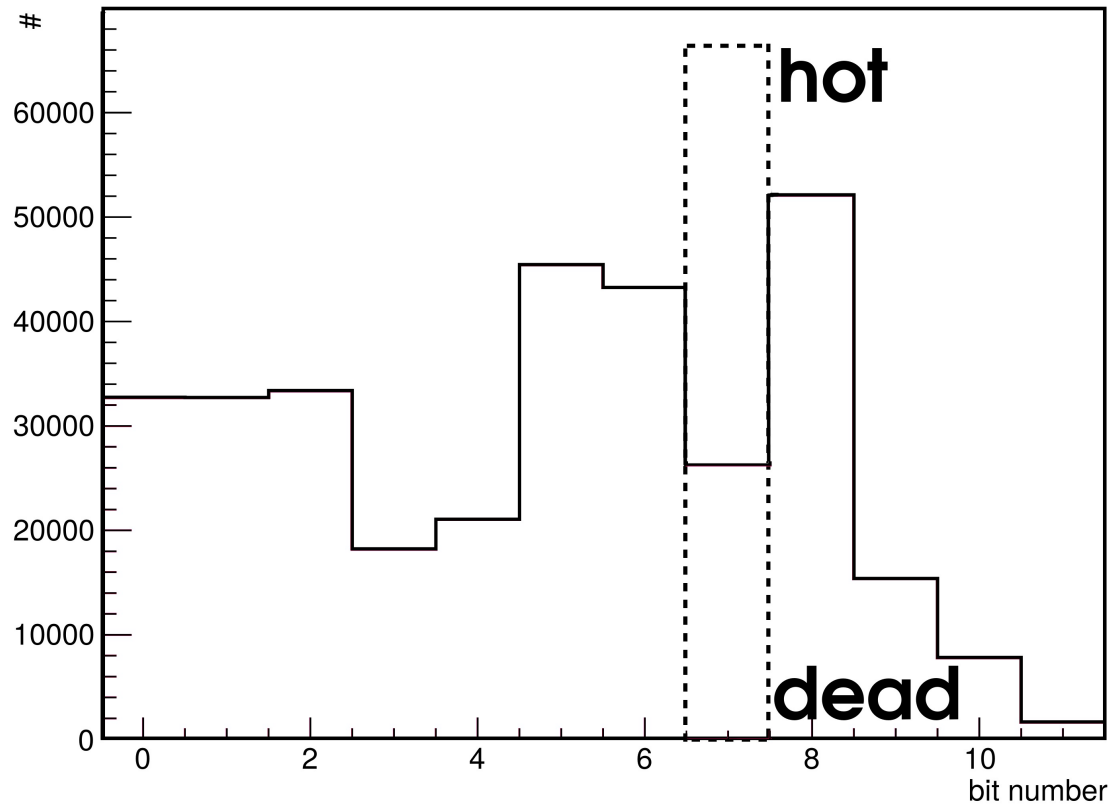
Test system - DAC linearity



Output pulse is linear within **15 mV** over the full dynamic range.
→ Further improvement can be obtained by tuning the input LUT

Bit test algorithm (method 1):

- Select UUB pulses in a fixed window of 40 samples
- Create a bit number distribution histogram for each pulse
- Analyse the distribution in order to identify bit errors

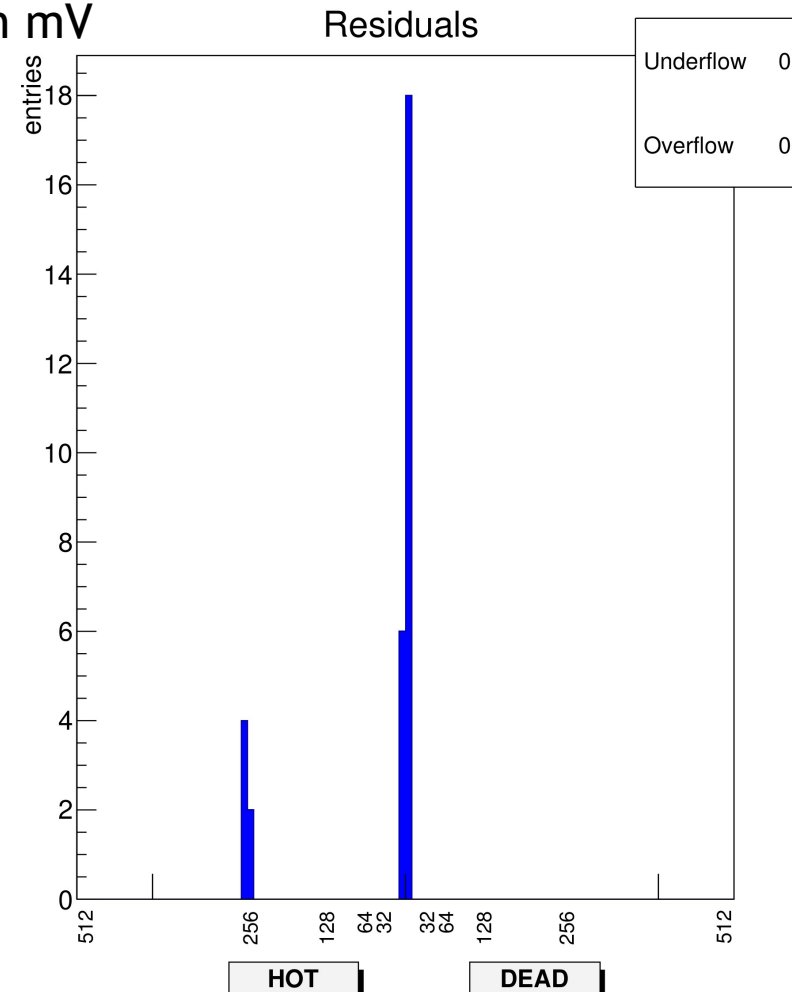
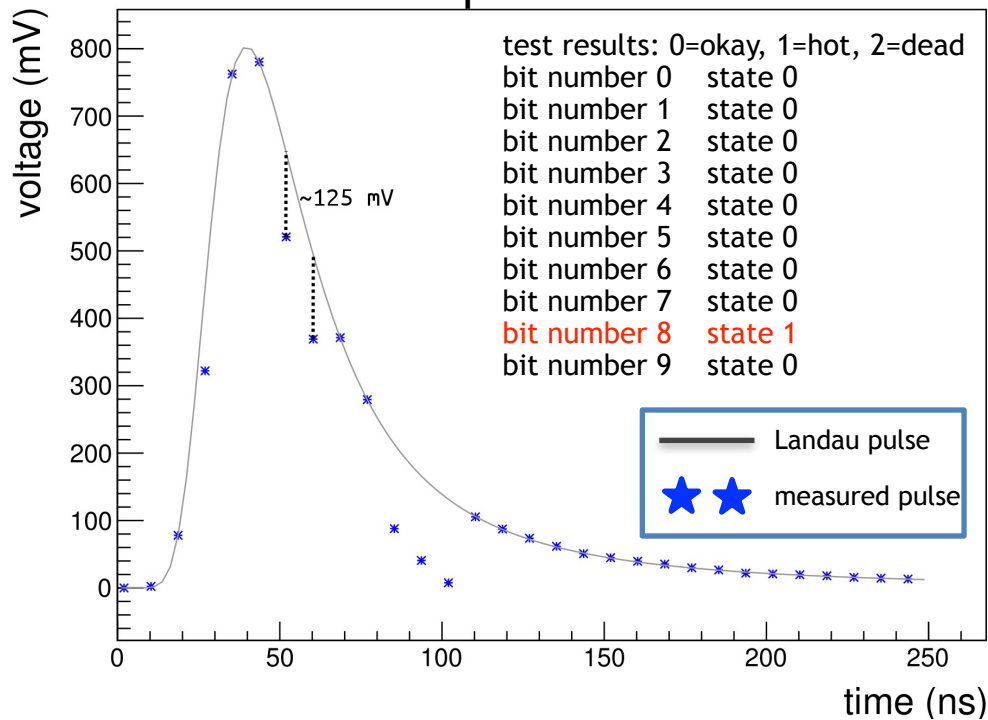


Bit test method 2

Bit test algorithm (method 2):

- Align the corrupted pulse with the input Landau pulse
- Measure the residuals between the two pulses in mV
- Interpret the residuals in bit number

An example of a bit test



The algorithm is able to intermittent bit errors