UUB Firmware & Timing

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for the SDEU team

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Trigger Status

- The following main features are now implemented in the most recent firmware on GitHub:

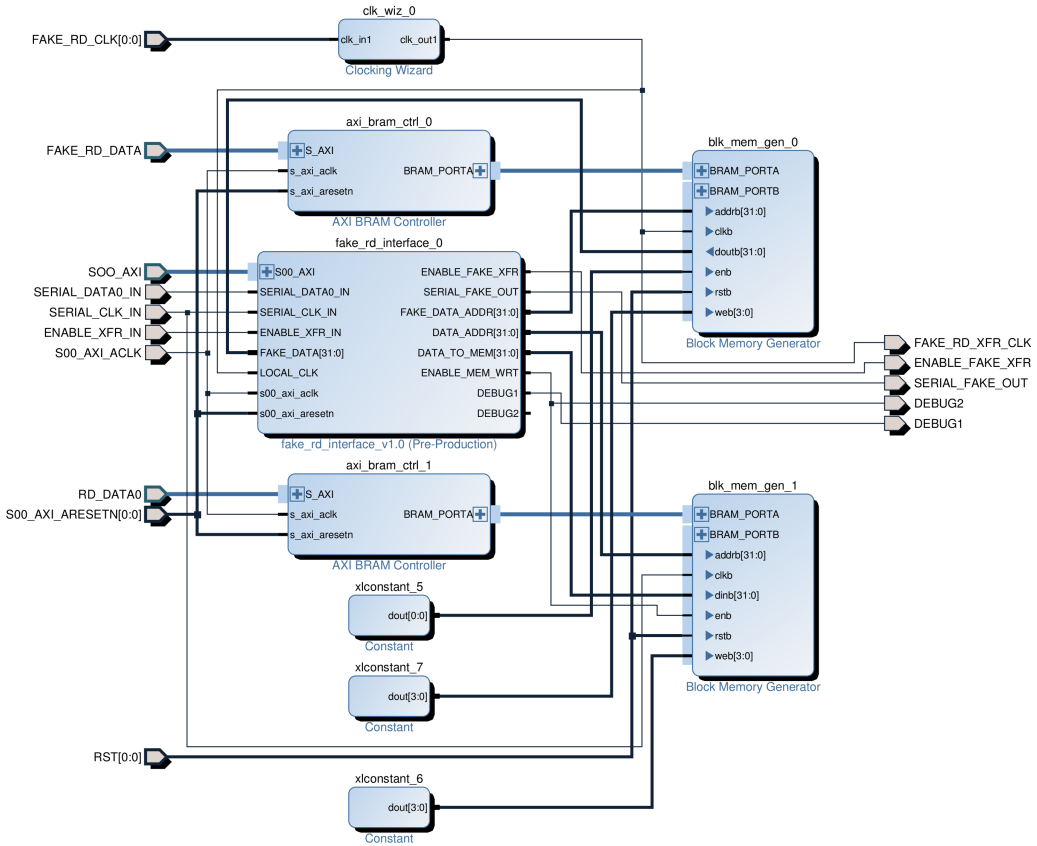
Feature	In Firmware	In DAQ
40 MHz single bin trigger	Yes	Yes
40 MHz ToT trigger	Yes	Yes
40 MHz ToTd trigger	Yes	Not yet
40 MHz MoPS trigger	No	No
120 MHz single bin trigger	Yes	Yes*
120 MHz ToT, ToTd, MoPs	No	No
AMIGA interface	Yes	No
Independent interrupts	Yes	Not yet
Independent DMAs	Yes	No
Scalars	No	No

- Yes* = Implemented but not enabled at present
- Not Yet = More testing on Didi is required before putting in field

Related Items & Issues

- Fake event feature has been upgraded to include
  - Randomly timed traces
  - Replay of recorded events
- 40 MHz ToTd testing on Didi not yet successfully completed
- A few percent of external triggers seem to be missing in Prague
  - Seems to be reproduced in MTU lab, diagnosis started
- Test of interface to Radio Upgrade (fake_rd_interface module) is implemented (not in released version)

UUB Radio Upgrade Interface Tests



First step - test module to send fake data out digital connector cable

Can form basis of the eventual real RD interface module

Signals are looped back at end of (conservatively long) 1m flat ribbon cable to look like signals from RD

Module includes:

Memory to store fake data

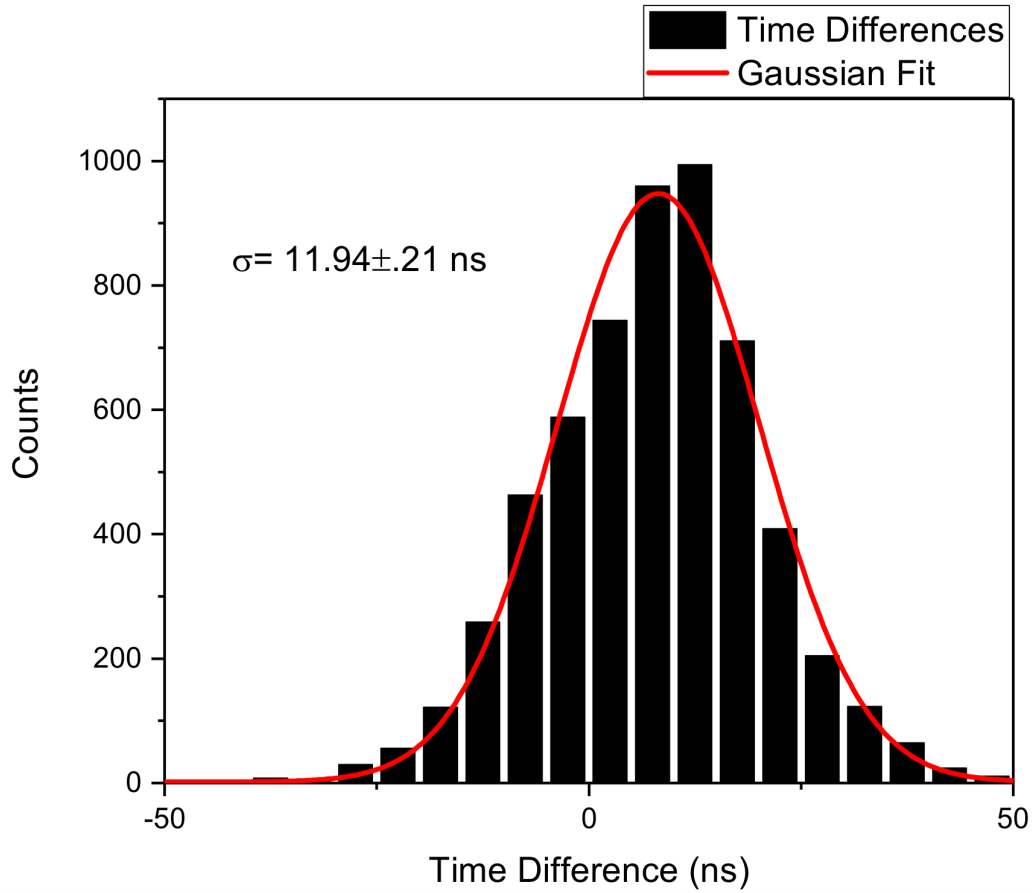
Parallel to serial & serial to parallel conversion

Memory to store data looped at end of cable

PLL to allow data transfer clock speed to be changed

200,000,000 random 12 bit signals transferred out and back cable with no errors at 100 MHz

CWRU Timing Studies (continued)



$$\textit{Single station RMS} \approx \frac{11.94}{\sqrt{2}} = 8.44 \text{ ns}$$

Independent tests with showers achieve $\sigma_{single} \approx \frac{14.8}{\sqrt{2}} \text{ ns} \approx 10.5 \text{ ns}$

Problems with Repositories?

Increasing SDEU team $\Longleftrightarrow$ Designs are shared

- Firmware
  - https://github.com/auger-prime-sde/uub-firmware/wp1
  - https://github.com/auger-prime-sde/uub-firmware/wp2
  - https://github.com/auger-prime-sde/uub-firmware/wp5 (Packaged wp2 releases)
    - Relevant source code & test programs seem to be in the repository
- UUB Linux integration
  - https://github.com/auger-prime-sde/uub-integration
    - Only binary files in the repository — where are the relevant source files?
    - For example, where are the device tree files?
    - Not clear what configuration is incorporated
  - https://github.com/auger-prime-sde/uub-linux
    - No updates since 2016 - Some problems cloning?
  - https://github.com/auger-prime-sde/u-boot-uub
    - No updates since 2016 - Some problems cloning?

Problems with Repositories?

- DAQ
  - svn://server1.auger.mtu.edu/uub_sw
    - All relevant source files are in the repository
- Slow Control
  - https://at-web-physik.uni-wuppertal.de/svn/sde_upgrade/
    - All relevant source files are in the repository — need to clarify access
  - Also there is a slow control repository at https://github.com/auger-prime-sde/uub-firmware/wp4
    - Does not seem to be updated. Is this now obsolete? Which is the true repository?