SDE Upgrade
WP5 ECRs

V2 Status

December 2017, 10 UUB produced

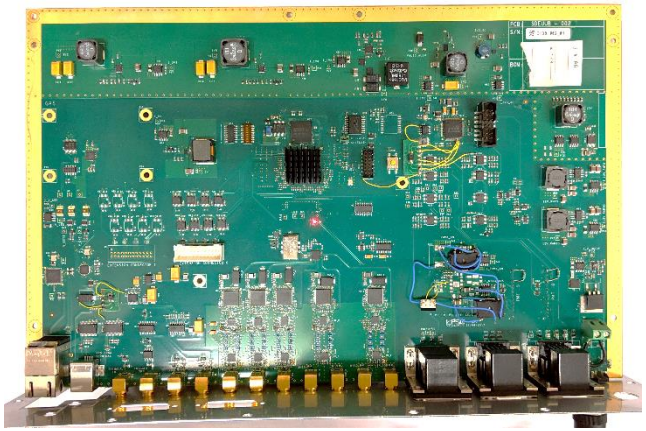
- 42 NCRs:

  19 critical, 4 was still pending

Begin October 16, EA:

- 6 UUBs available, retro-fitted and tested at Malargüe (WP5):
- Total 57 NCRS:

  22 critical

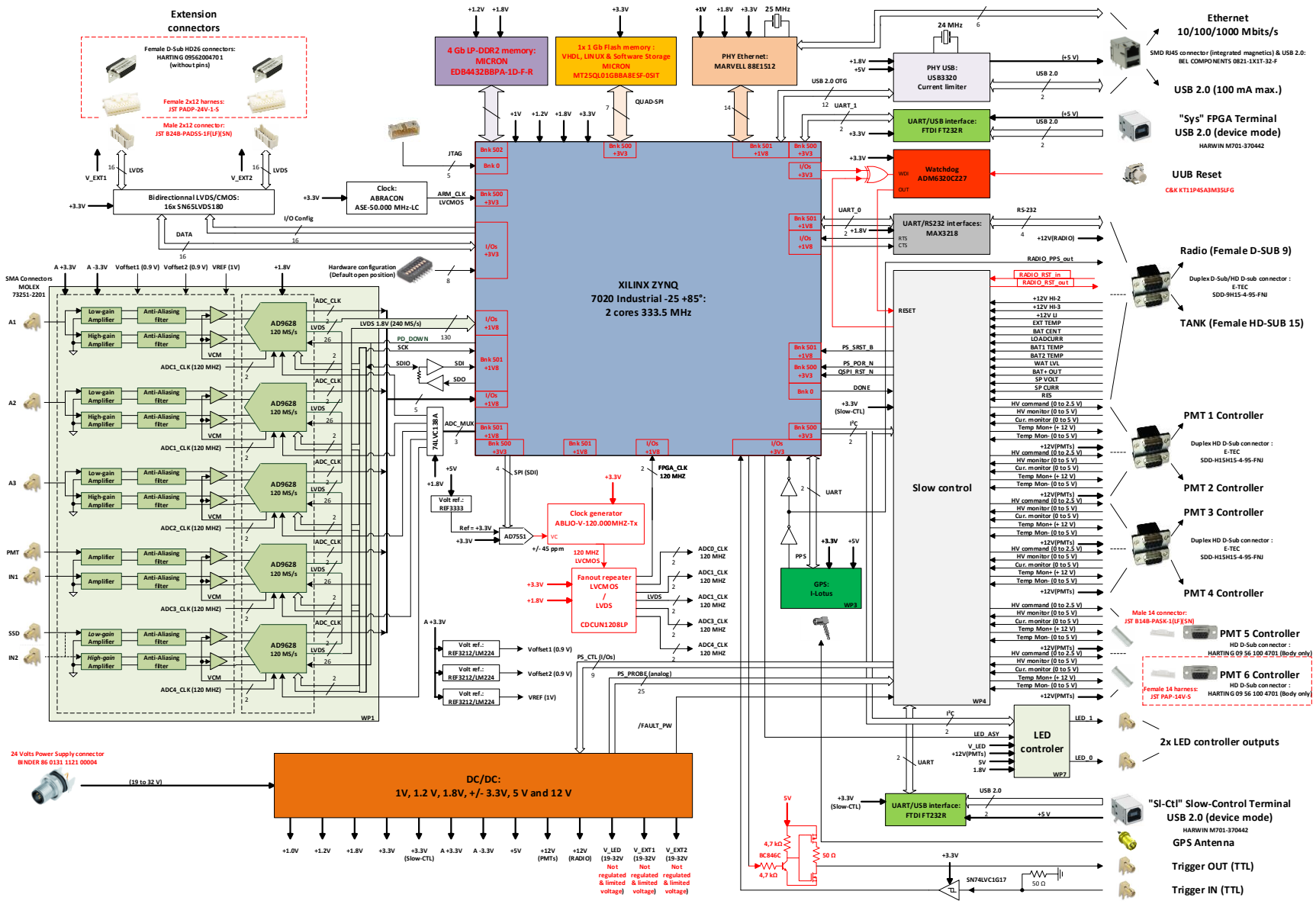


Next prototypes must FULLY tested before mass-Prod

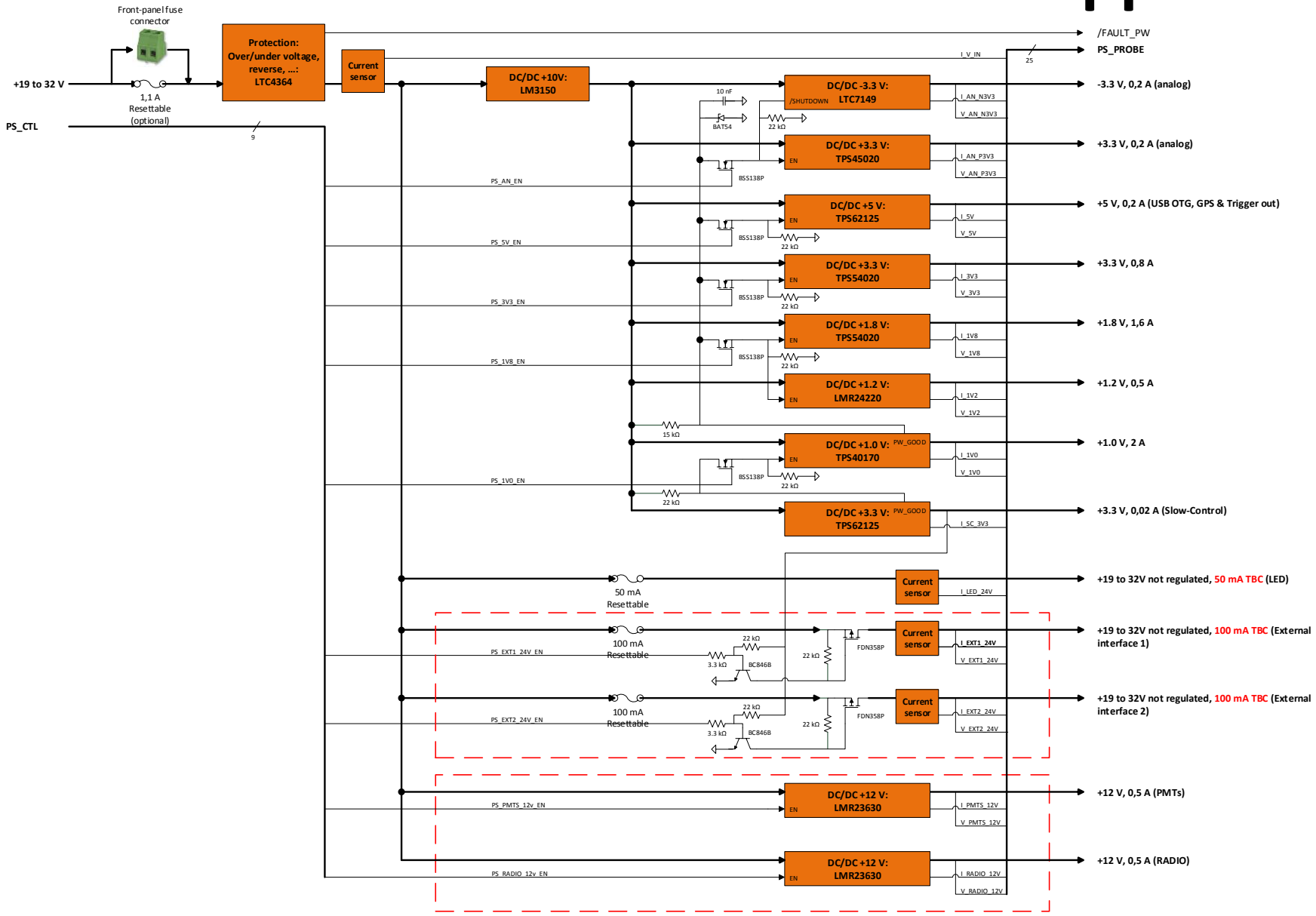
ECRs (Dec 2018) for the next UUB version 3

- Present UUB block Schematics
- ECRs description

UUB block Schematic – main (v2.0)

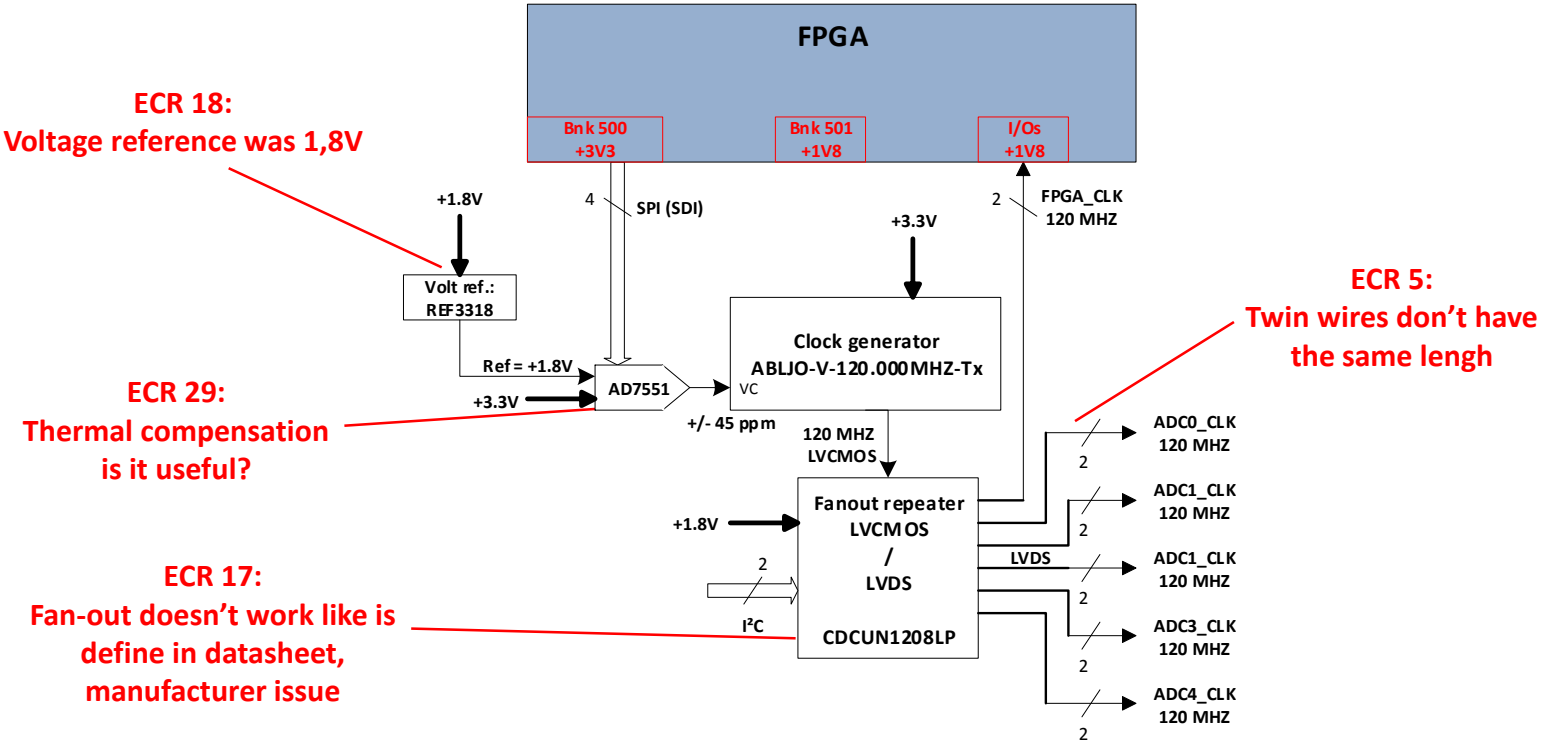


UUB block Schematic – Power supplies



ECR 5, 17, 19 & 29: 120 MHz clock 1/2

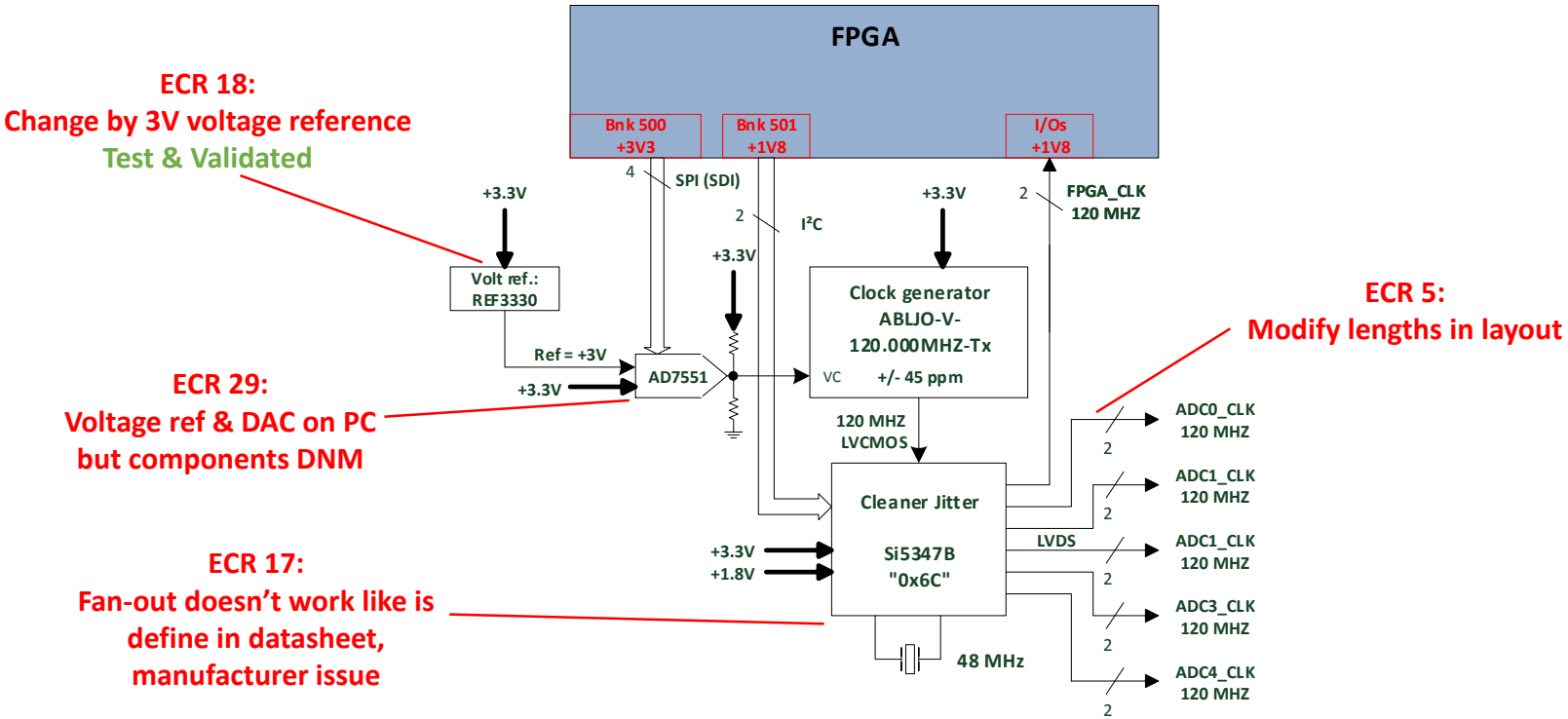
Present V2.0 Schematic:



The Fan-out component must be changed. It is not conform to the manufacturer specification

ECR 5, 17, 19 & 29: 120 MHz clock 2/2

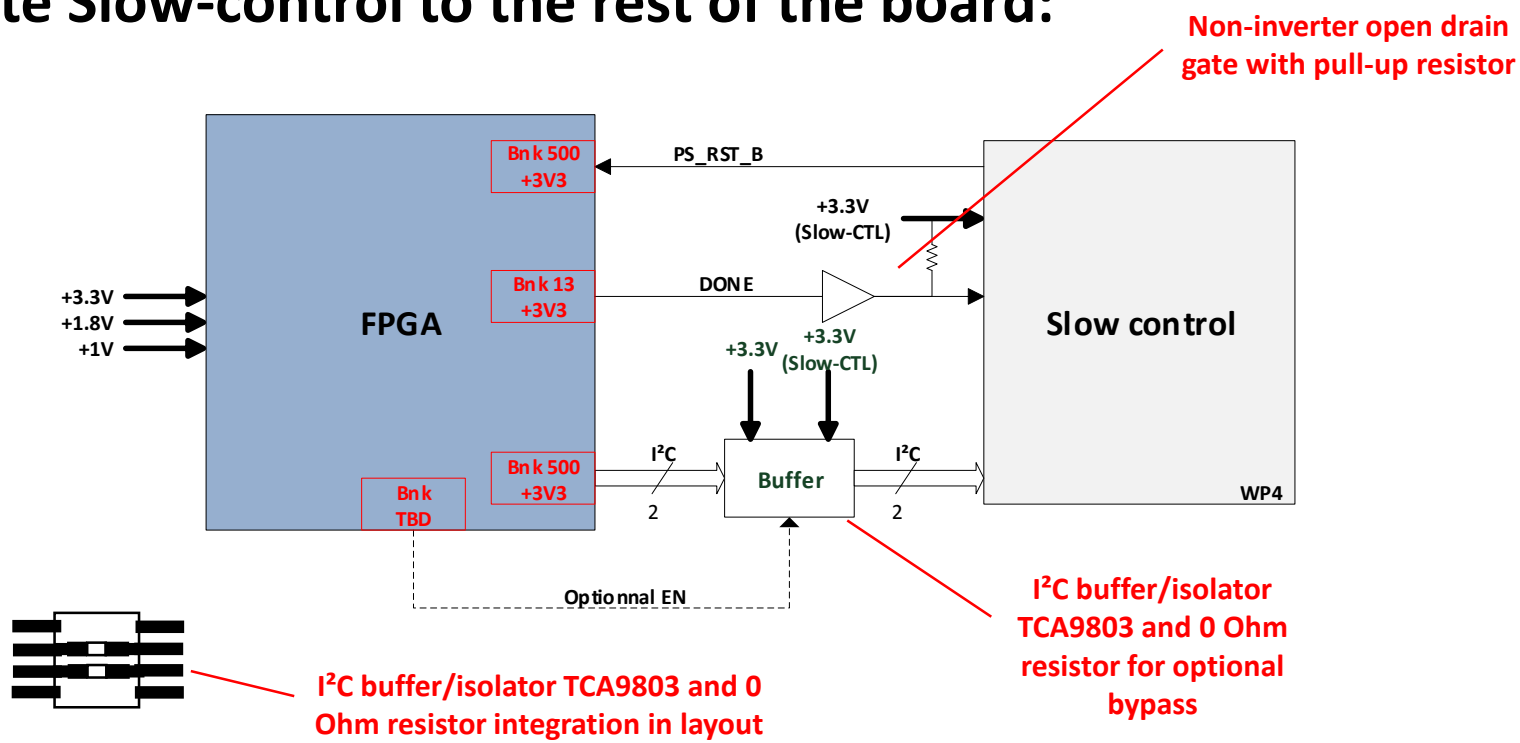
Next V3.0 Schematic:



- The Fan-out is changed by a solution already test and validated: **Jitter Cleaner**
- Thermal frequency compensation useless: Time tagging function already integrated -/+ 45ppm tolerance

ECR 4, 38 & 46 : FPGA protection

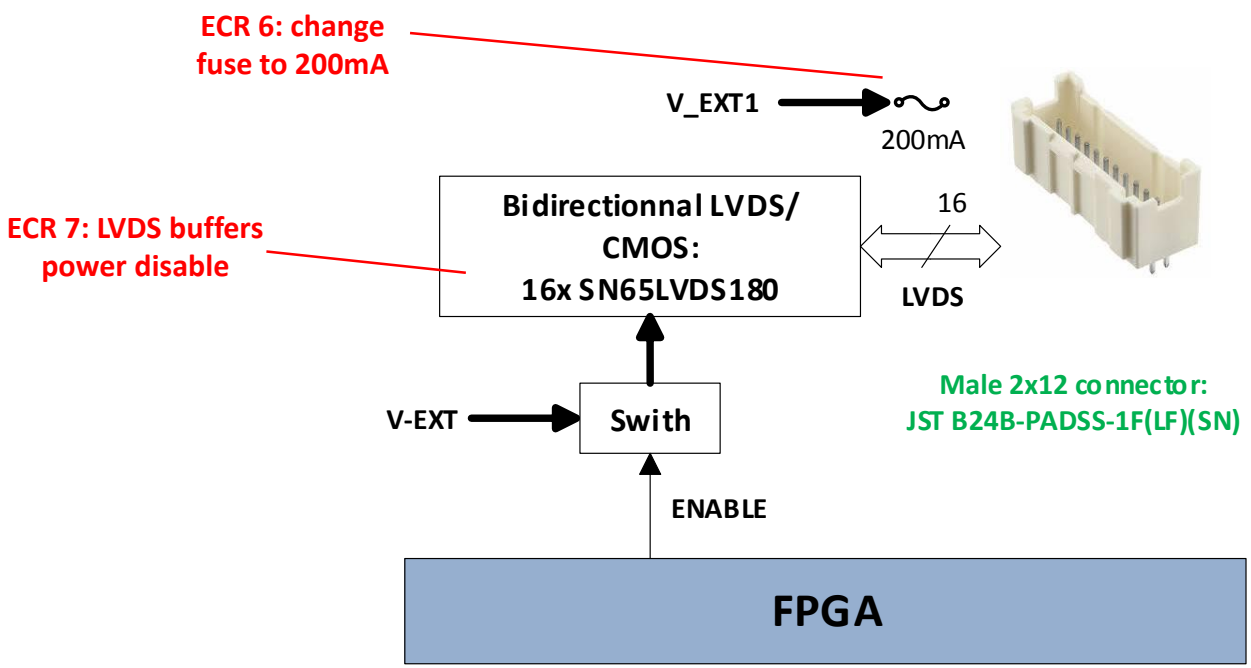
Isolate Slow-control to the rest of the board:



The slow-control starts the first and send voltage to FPGA when it isn't powered:

Dangerous for FPGA

ECR 6 & 7 : Digital connectors



When Digital connectors are unused, the buffer power could be disable:

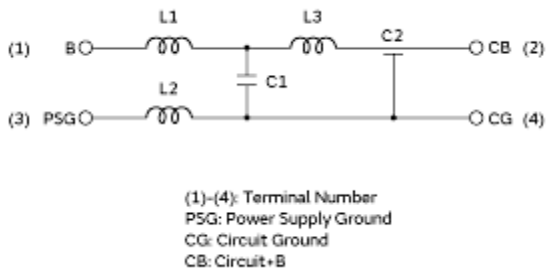
less power consumption

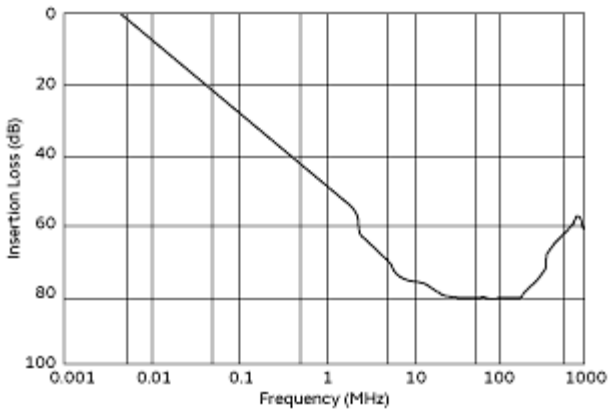
ECR 11, 47 & 48: UUB EMC noise

Noise is generates by UUB and transmit by the cable

A EMI filter will be added after main UUB power connector:

BNX002-01

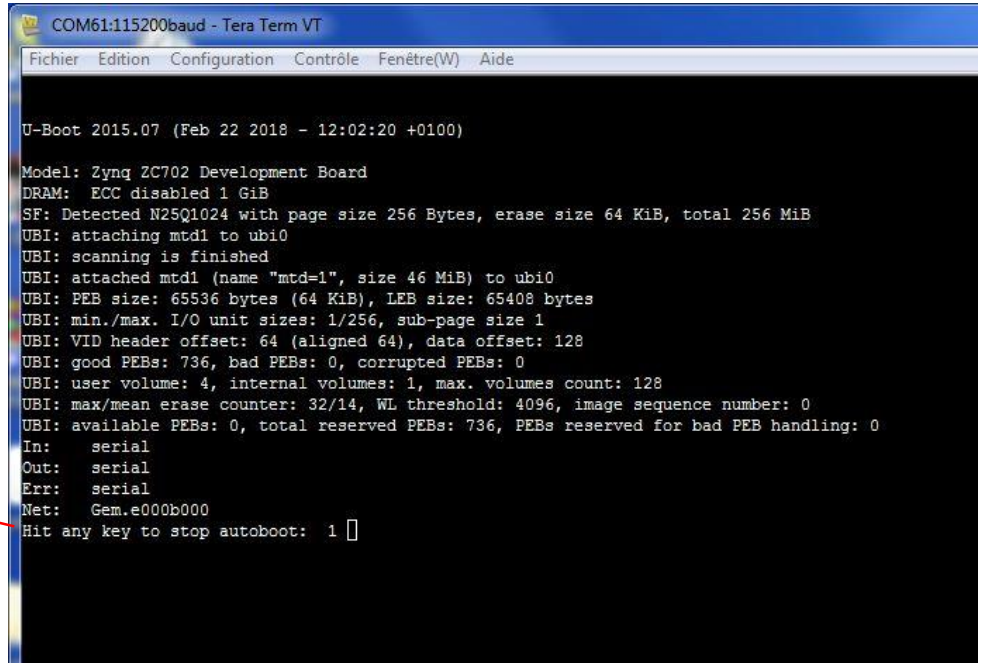




- **The 24 Volts provided by UUB on digital connectors should also be filtered. These connectors will power external devices**
- **External cables should be shielded. They transmit the noise everywhere**

ECR 20 : FPGA frozen when no USB PC connected 1/2

- **Several hardware solutions (v1 & v2 schematic, added buffer, …) was tested, but no one solve this issue for all boards.**



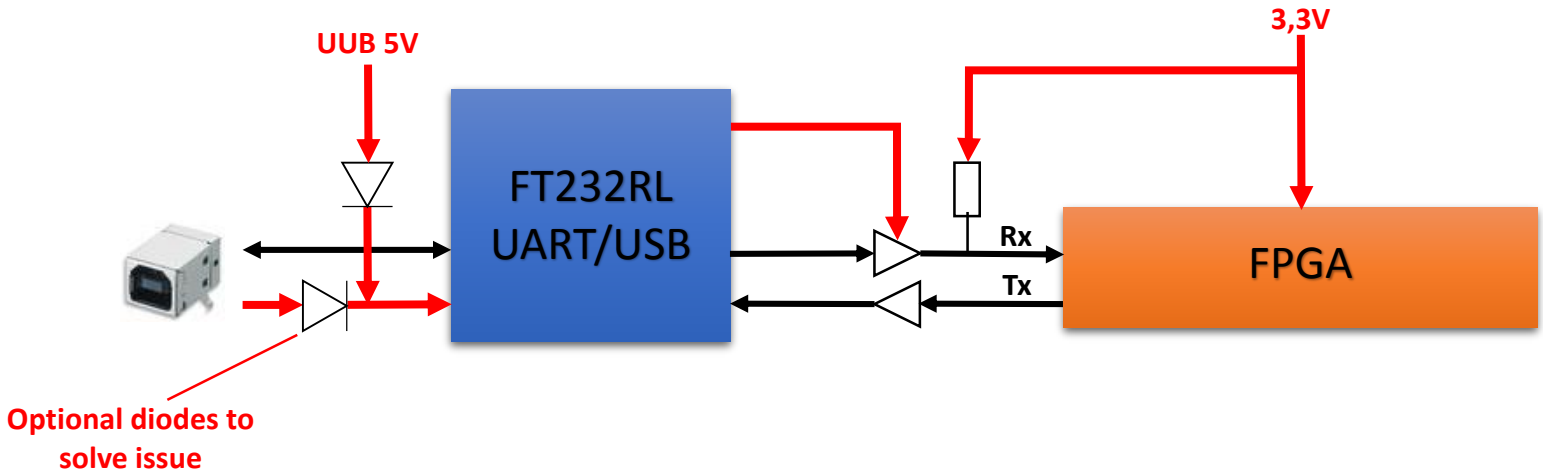
U-BOOT stop sequence

Tested with V2 hardware schematic and a specific software where the U-BOOT can't be interrupted: the issue is solved

Software update and MAC address could be made with Peta-Linux

ECR 20 : FPGA frozen when no USB PC connected 2/2

- **The FPGA must have protection against external voltage from USB interface**

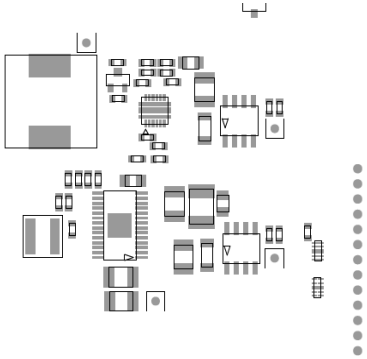


Buffer open-drain must be added for FPGA protection. VCCIO pin powered by UUB 3,3V, it's not enough.

ECR 26: TRACO DC/DC modification

The present -/+3,3V DC/DC:

They are too noisy. But the Enable function works.



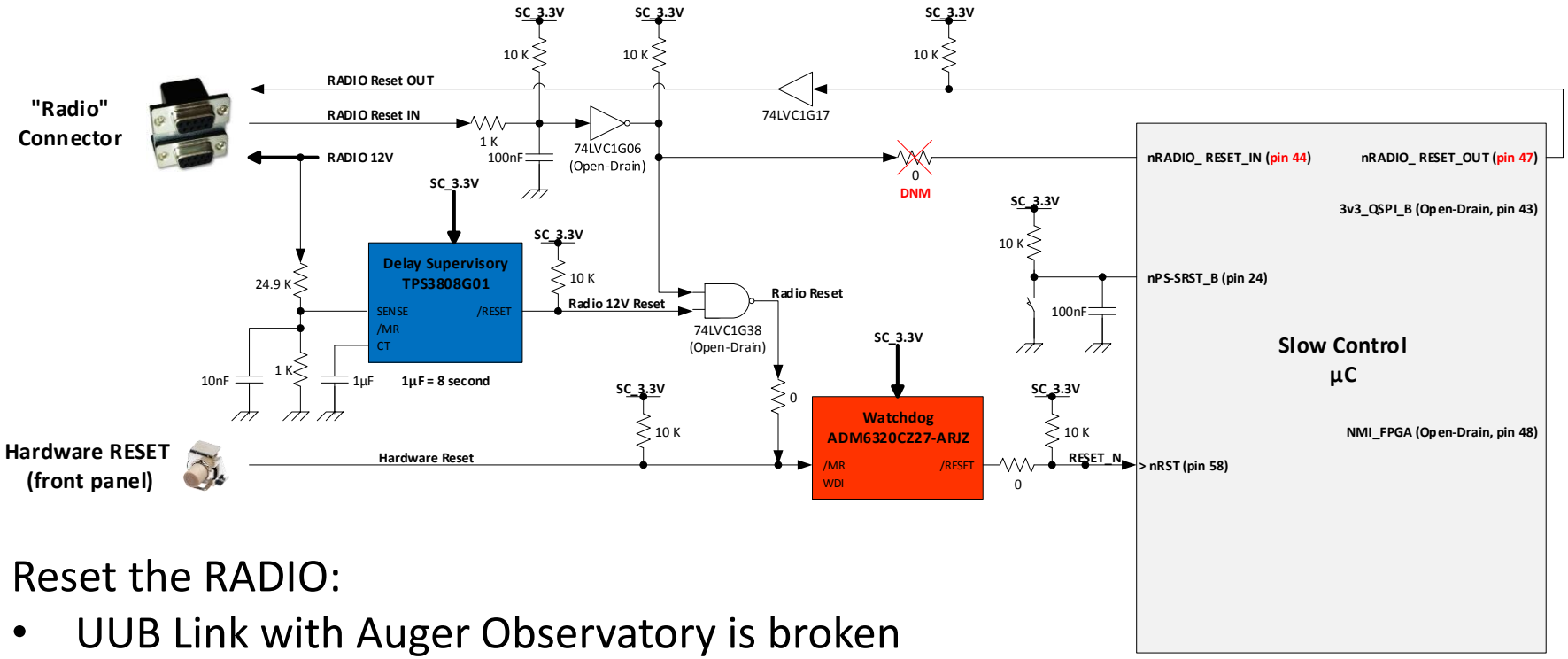
The TRACO POWER DC/DC:

Less noisy but up to now a relay is used for Enable/Disable function. It could generate problem, like spike in channel 9.

If it is possible, the Relay should be changed by a new electronic: In work

ECR 34: Radio Reset Out

Radio Reset Out:



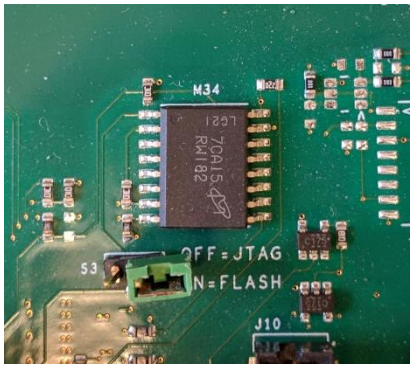
Reset the RADIO:

- UUB Link with Auger Observatory is broken
- UUB can be Reseted
- Possible UUB restart loop: Not tested at Malargüe

Keep footprint on PCB but components not soldered

ECR 35: Programmed component

Slow-control µC & Flash Memory:



Slow-control µC:

- Programmed by manufacturer
- Optional package reference

Flash Memory:

- Programmed and repackaged by a subcontractor

Min 21 weeks lead time

Final software for Slow-control must be provide early

NO SOFTWARE UPDATE DURING MASS PRODUCTION AT SUBCONTRACTOR

ECR 37: Digital cable

Slow-control µC & Flash Memory:

Slow-control µC:

- Programmed by manufacturer
- Optional package reference

Flash Memory:

- Programmed and repackaged by a subcontractor

Min 21 weeks lead time

Final software for Slow-control must be provide early

NO SOFTWARE UPDATE DURING MASS PRODUCTION AT SUBCONTRACTOR

ECR 40: Spikes on channel 9

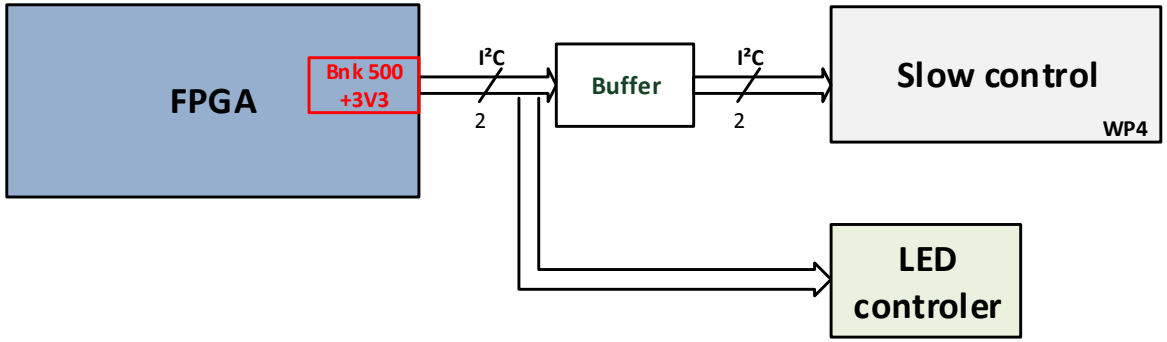
Present -/+ 3,3V DC/DC:

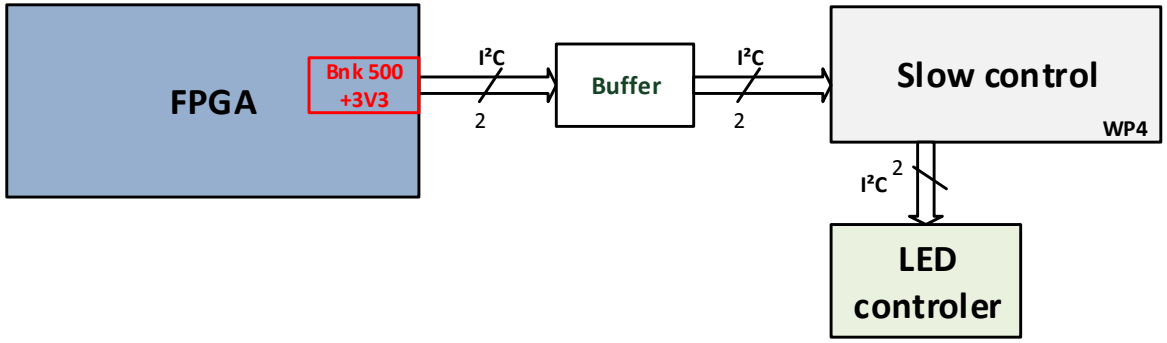
Spikes come from DC/DC Position. They are on the back, with their internal coil close UUB PCB.
Relay doesn't generate spikes

ECR 44, 45 & 49: UUB restarts & I²C

Sometime the UUB restarts in DAQ mode:

I²C communication with LED DAC problem generates Watchdog restarts the UUB





2 available channel in Slow-control could be used for LED-controller

Minor ECR

ECR 1, FPGA can't start, bad H/W config:

R214 in layout, must be D.N.M. but present BOM:

R214 must be removed in BOM: Tested & Validated

ECR 2, Set in Flash Reset without transistor:

New flash memory has a Reset pin, so its switched 3,3V power is useless:

Remove Q6 & add R223, R227: Tested & Validated

ECR 8, GPS antenna cable is too long:

Could disturb integration:

Remove 1 or 2 cm

ECR 9, PMT cable is too long:

Could disturb integration:

Remove 0,5cm

Minor ECR

ECR 10, GPS antenna or its cable:

Sometime the 5V is in short-cut:

Add fuse for GPS 5V

ECR 12 & 13, J1 connector is not good position:

The footprint is not compliant with specifications:

Change J1 footprint

ECR 14, C50, C127, C129 & C155 capacitor footprint:

PCB footprint doesn't compliant with the component:

Change CAP-021 footprint

ECR 15, C389 capacitor footprint:

PCB footprint doesn't compliant with the component:

Change CAP-056 footprint

Minor ECR

ECR 16, M52 Fan-out clock component has 2 pull-up for OE pin:

ECR 17 dependent:

remove R294

ECR 18, R339 resistor has bad value:

Could generate a "Reset loop" :

R339 must be changed to 24K in BOM: Tested & Validated

ECR 21, Slow-control 3,3V isn't connected to USB interface power:

USB interface internal buffers aren't powered :

Connect M38 pin 4 to 3,3V

ECR 22, Fan-out 3,3V I²C connected to 1,8V FPGA bank:

ECR 17 dependent:

Change connection to Bank 500 I²C (FPGA, S-L & LED DAC I²C)

Minor ECR

ECR 24, No 10V power measurement:

10V power monitoring:

Make connection to Slow-control

ECR 25, PMT extension cable too short:

Can't be connected from UUB to Front-panel:

New longer cable has been made: Tested & Validated (EA)

ECR 27, UUB integrated in box doesn't start:

Front-panel pushes Reset switch button:

Move J1 connector and SW1 Reset switch. Made a larger hole on front-panel (EA)

ECR 28, PMT & Tank signals are attenuated:

ESD components attenuate signal:

Remove these signals on ESD components: Tested & Validated (EA)

Minor ECR

ECR 32, Additional test point to measure DAC signal:

Make modification in schematic and layout

ECR 42, R1_2, R4_1 & R4_2 Resistor package:

Bought in 0402, but the footprint is 0603:

Make modification in BOM

ECR 43, Q1_1, Q1_3, Q1_4 & Q1_5 transistor package:

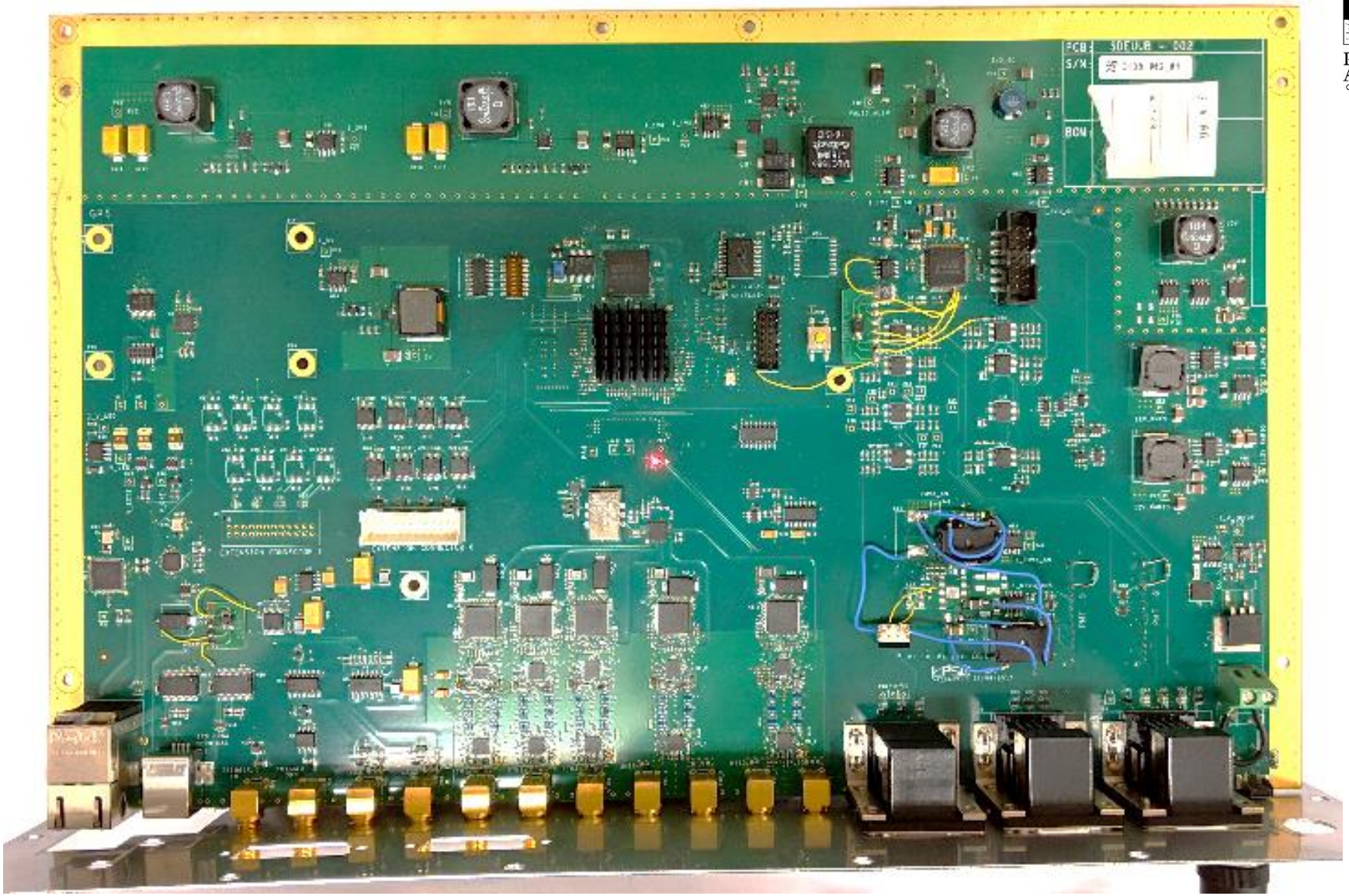
Footprint in PCB defined in SOT-23, but the component in SOT323/SC-70:

Change footprint in layout.

Conclusion

- All WPs design (Schematic & BOM) must be validated by them. Layout will start when all WP designs will be validated.

- WPs must check obsolescence status for their design.


PCB: SDEU.B - 002
S/N:
BOM:
GPS