DIRAC 2 Status and very preliminary results

LAPP

Renaud Gaglione

Laboratoire d'Annecy-le-Vieux de Physique des Particules
9 Chemin de Bellevue
74 941 Annecy-le-Vieux
FRANCE

february 24, 2009

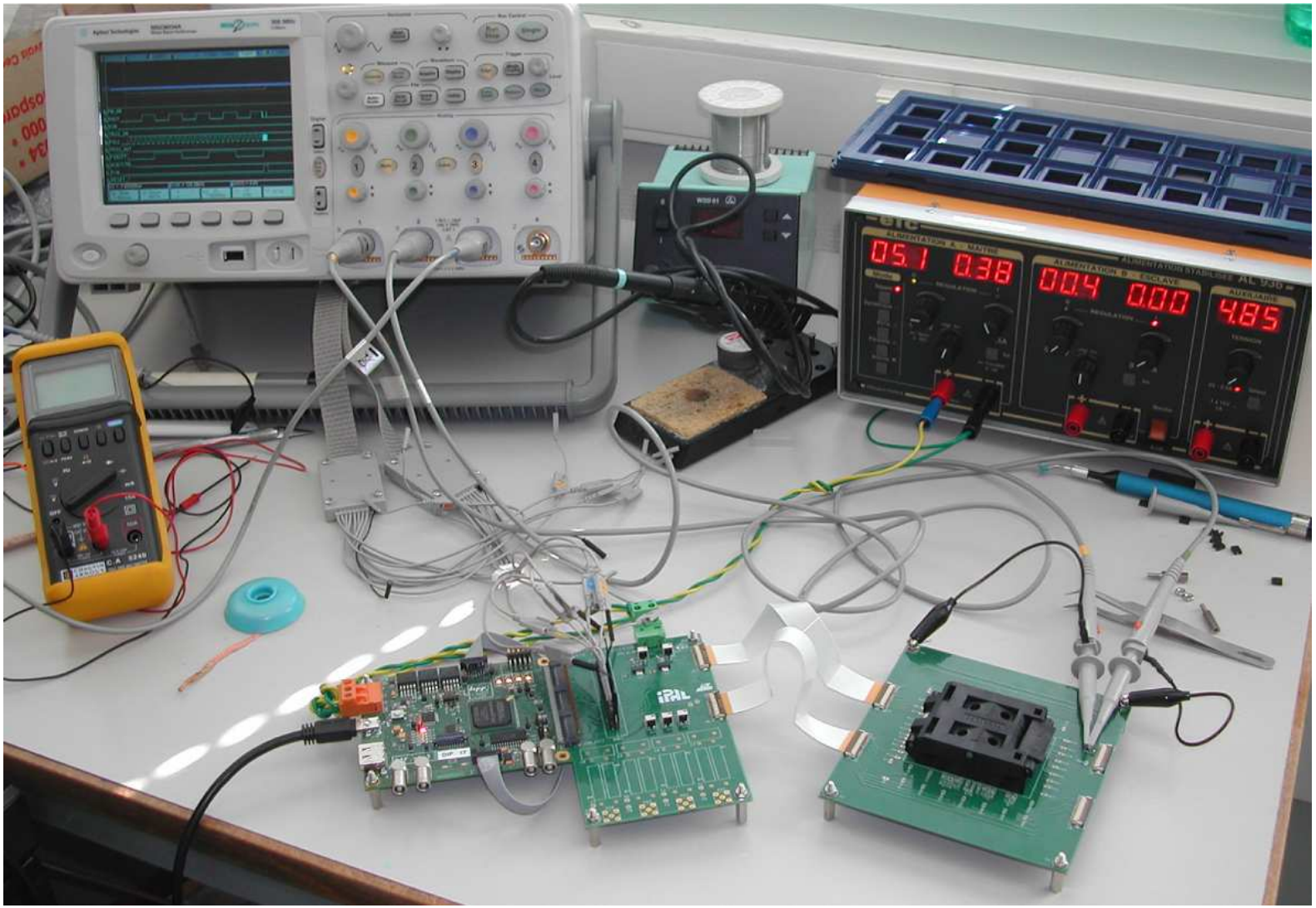
Outline

Outline

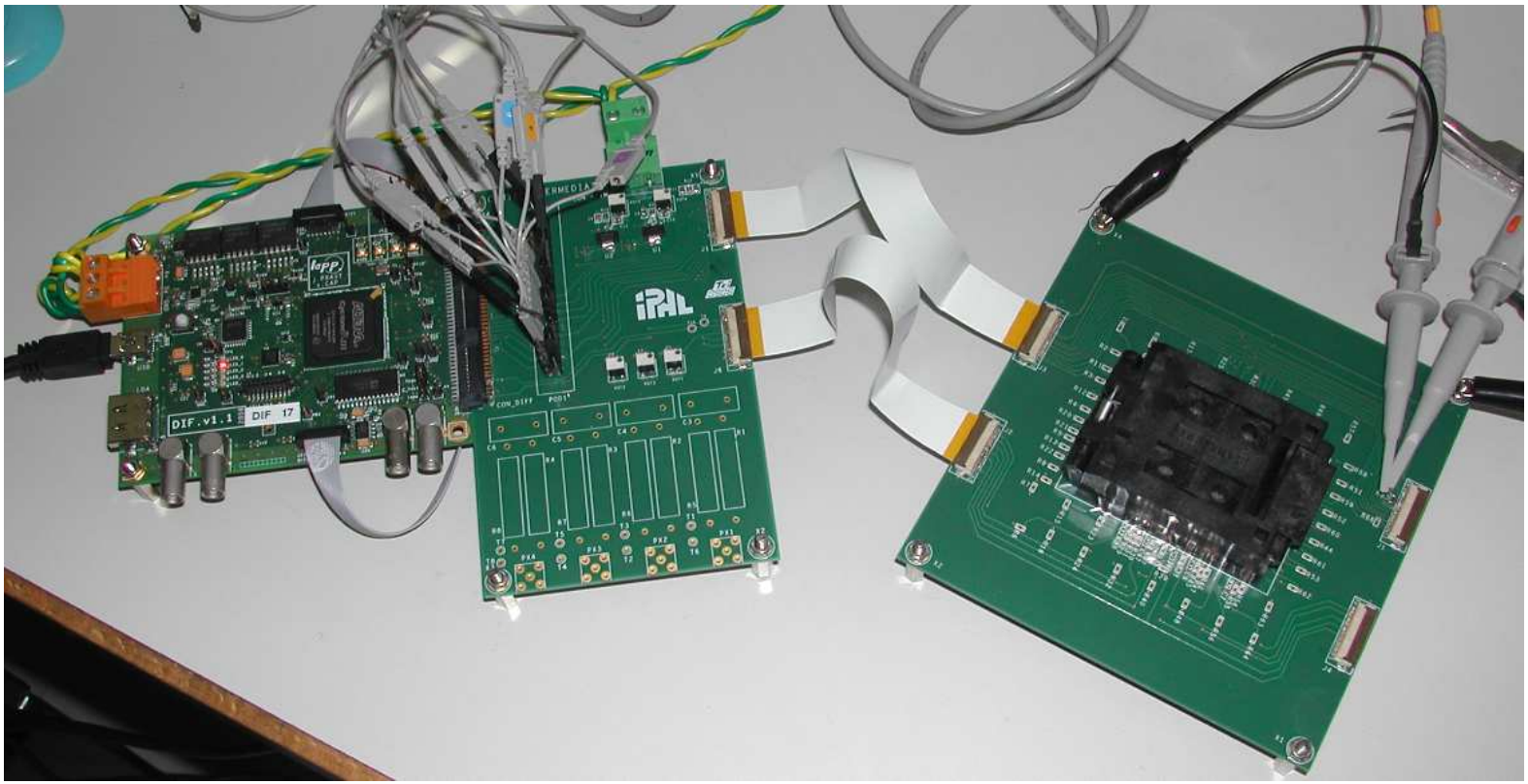
What do we have?

- 5 chips packaged in CQPF120 + 20 dies;
- 1 intermediate board (IPNL);
- 1 testboard (IPNL);
- 1 DIF with VHDL for DIRAC from G. Vouters;
- 1 Labview software from C. Drancourt.

Test bench



Test bench



Outline

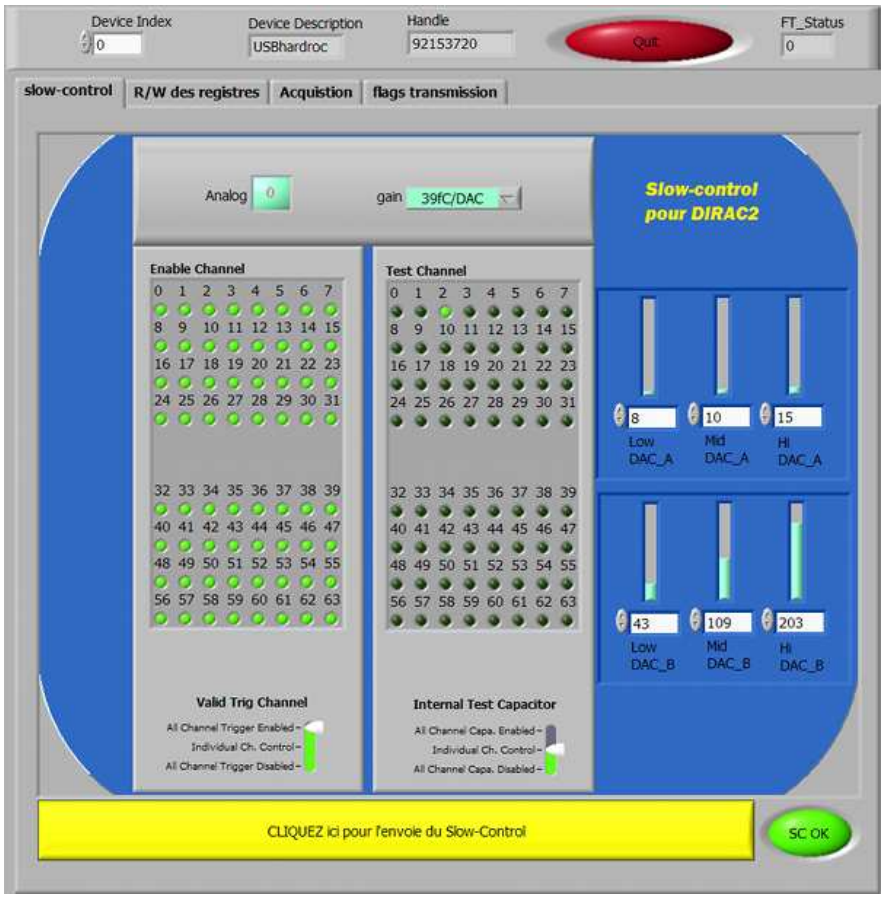
Board tests

- Test testboard (supplies, short circuits. . .) ✓
- Test intermediate board (supplies, short circuits. . .) ✓
- Test both (interconnection): inverted bus ! ✓
- Test with DIF (right level on each ASIC pin) ✓
- Test with ASIC and software: bad daisy chaining ✓

IB is OK, testboard has 2 non-critical mistakes.

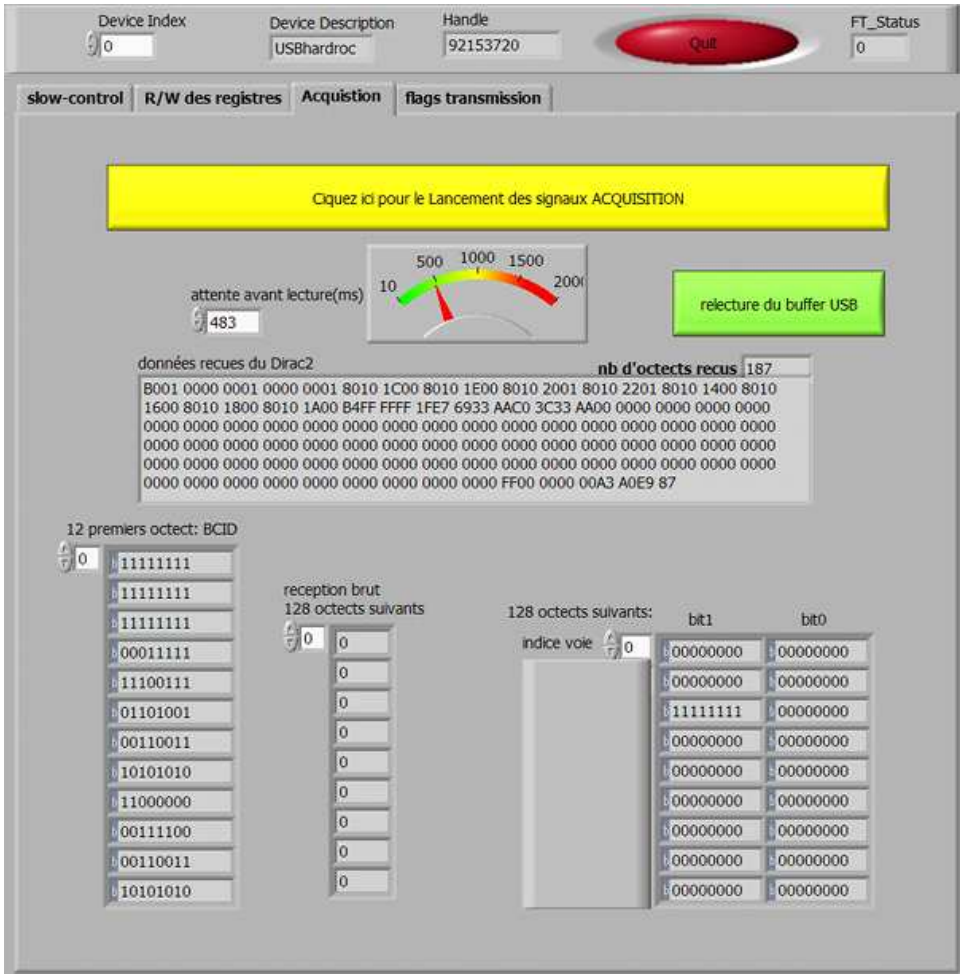
ASIC tests

Labview from C. Drancourt



ASIC tests

Labview from C. Drancourt



Outline

Functionnality

- LVDS clock receiver: ✓
- Configuration: ✓
- Digital I/O: ✓
- Channel tested: channel hited: ✓
- If DAC code decrease, output increase: ✓
- Digital noise immunity seems to be better (*vs* DIRAC 1): ✓

Characterization

Still some bugs:

- BCID seems wrong;
- Input charge with C_{test} seems wrong (S-curve @ 22 DAC instead of 42);
- Some limitations in DIF code (end of readout, period of stimulation);

Outline

Status

- Very promising preliminary results !
- Still waiting for C. Combaret XDAQ software !
- Need to write software to convert from Labview to ROOT;
- Need small changes/updates in Guillaume's VHDL;
- Full characterisation of ASIC;

Plan

- Delay for additional chips: 20 days;
- 200 circuits: 7 650€ (38.25€ each);
- 400 circuits: 11 250€ (28.12€ each);
- Plastic packaging (200 or 400): 2 500€;
- Ceramic packaging: 79€ each (not advantageous $\geqslant$31 packages).

What about ASU design ? Which size ?