News from raft construction and CCD optimization

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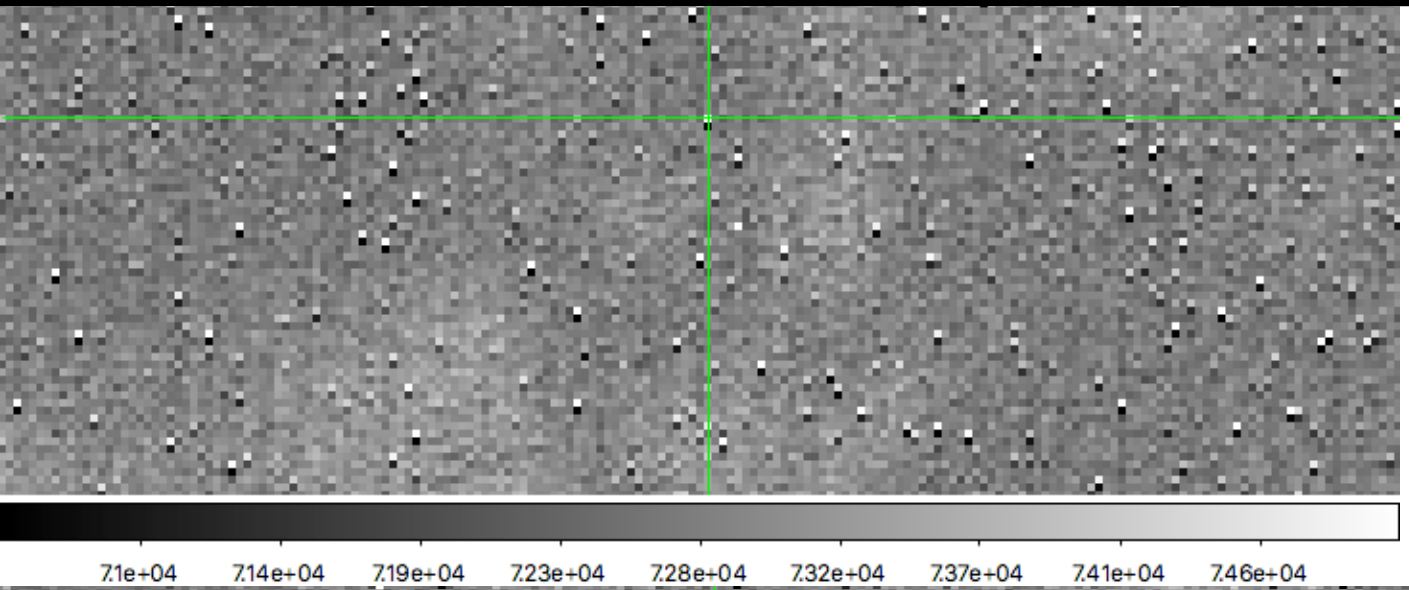
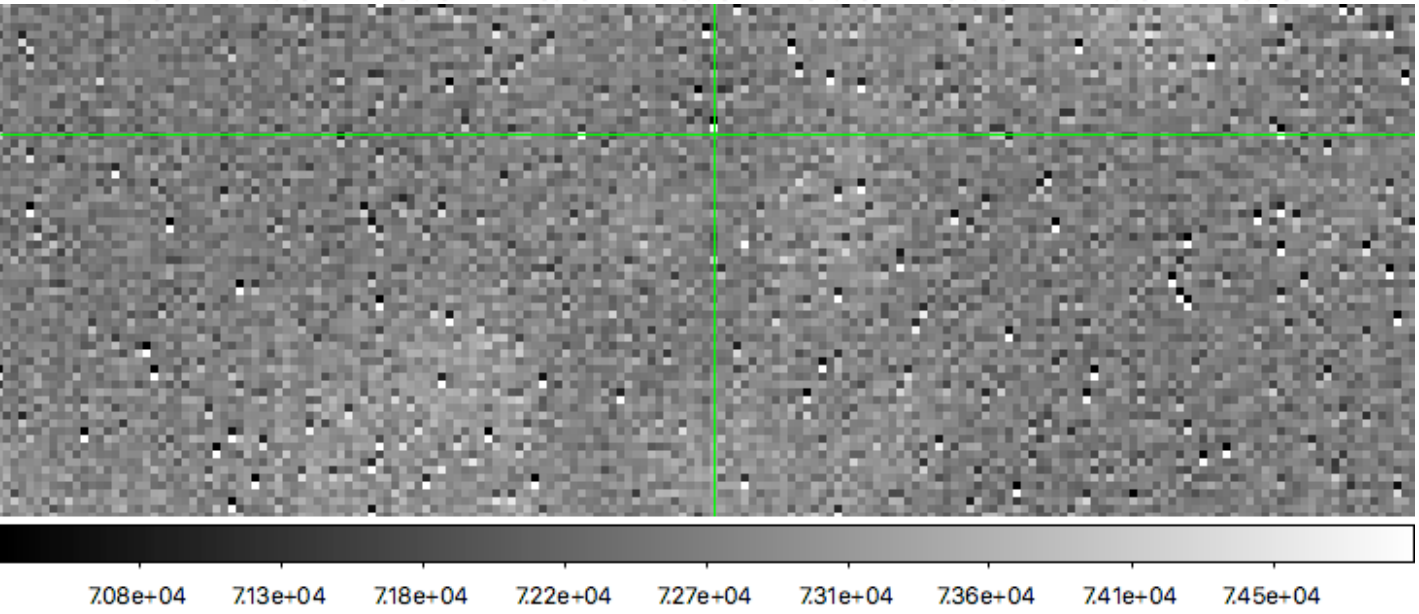
Dipoles in ITL sensors

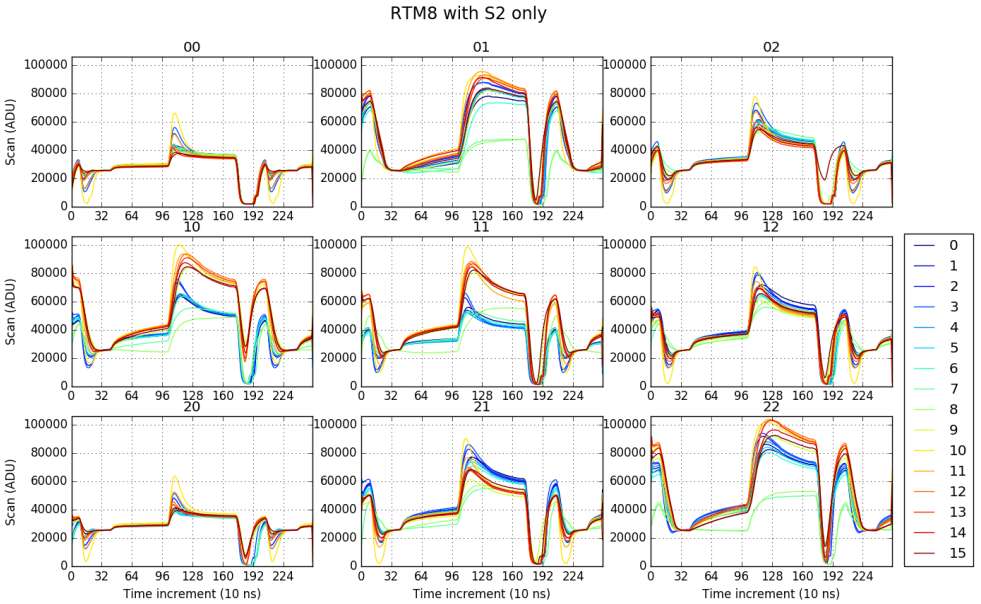


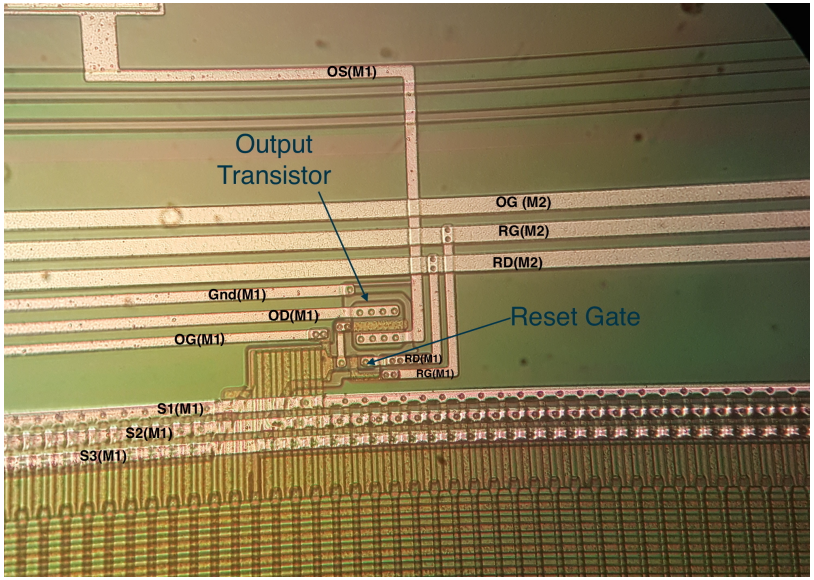


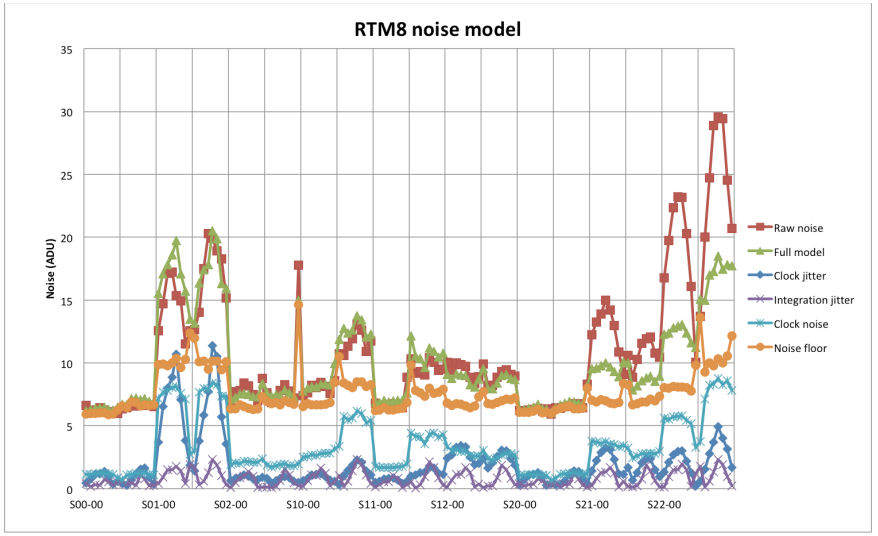
- Solved by integrating with two parallel phases high (out of three) instead of one

Clock injection in ITL sensors

- Issue: in some sensors, up to 5% of the serial clocks is injected right into the sensor output
- Creates a noise contribution up to 20 e-

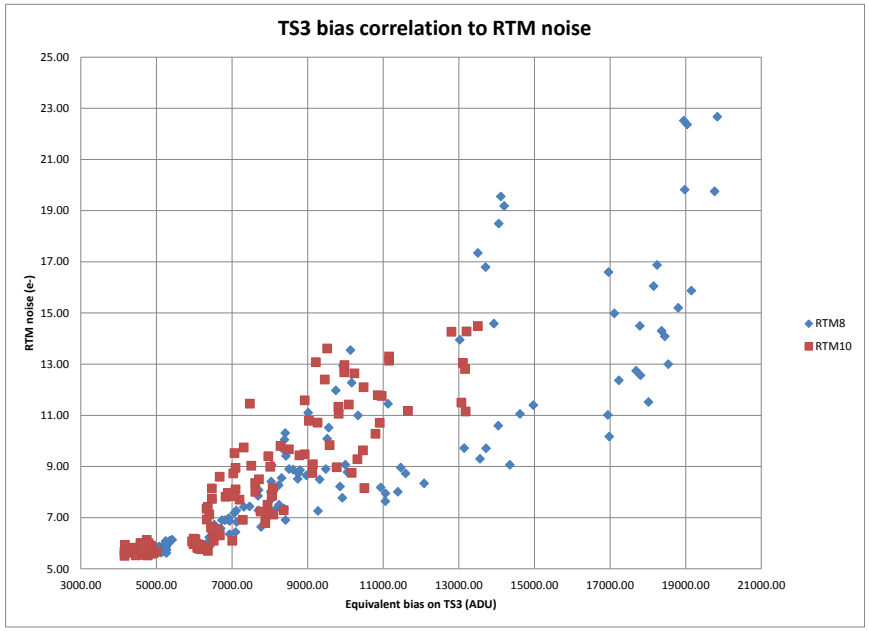


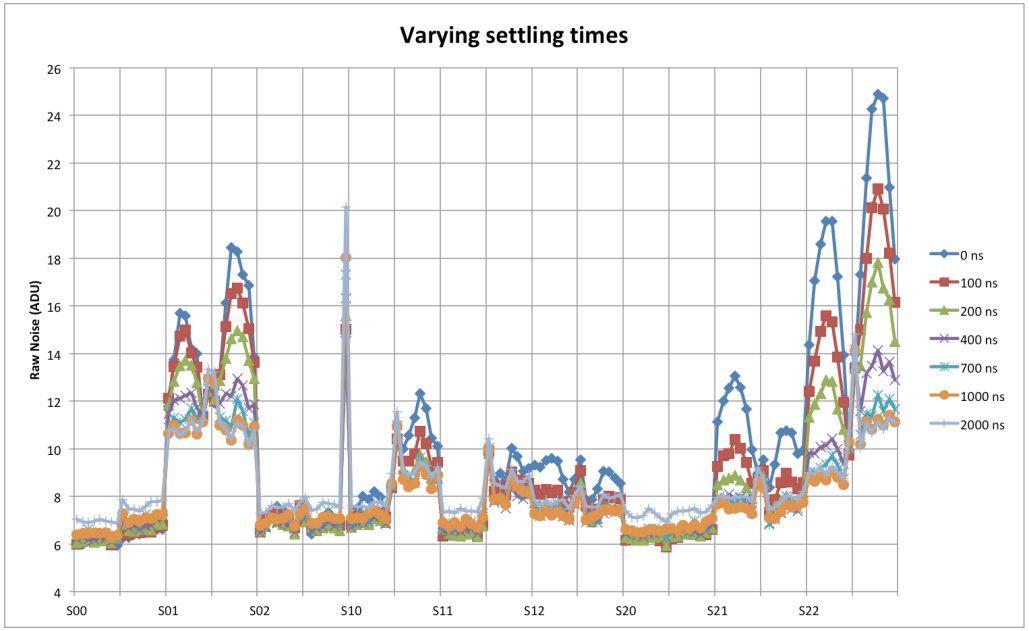




Clock injection in ITL sensors

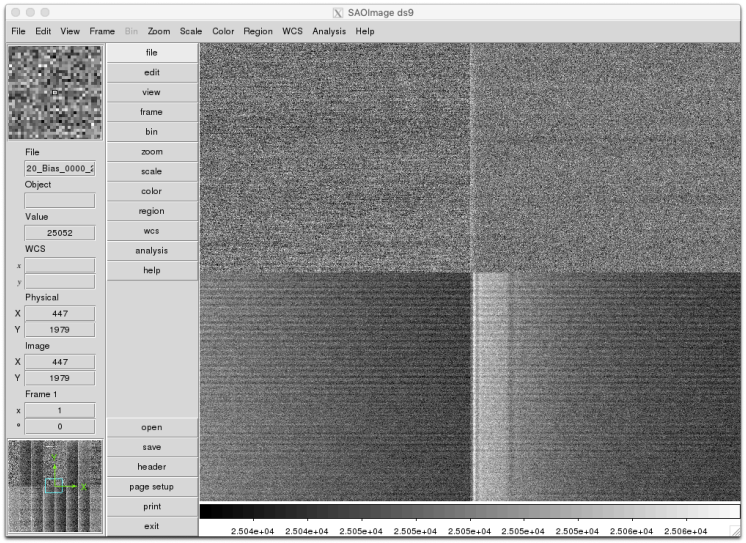
- Attributed to bad grounding on the substrate below the output transistor
- Solution: grade sensors based on measurement on single-CCD test-stand at BNL
- Also a solution: read slower…

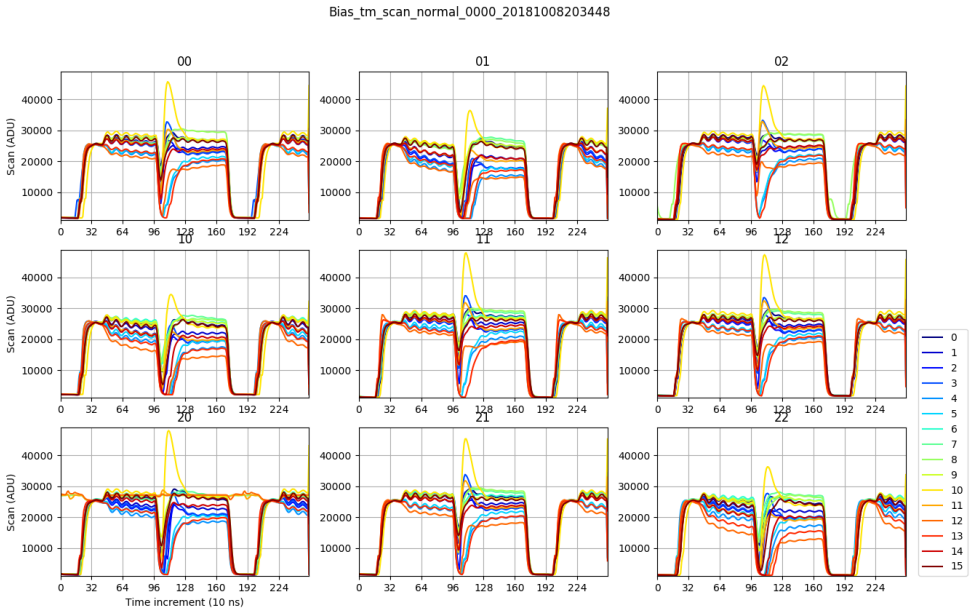


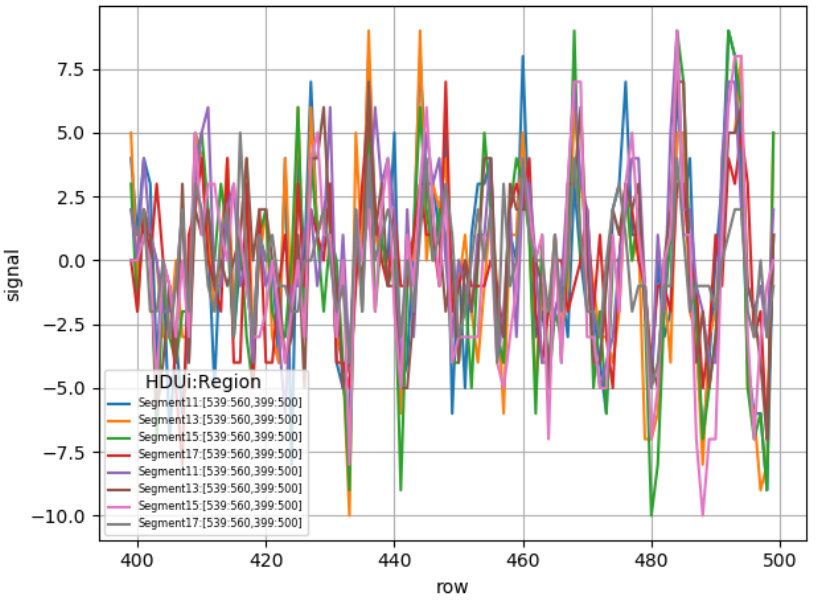


Noise issue in ITL rafts

- Appeared after shipping from BNL to SLAC
- All ITL rafts, only ITL rafts
- Correlates with ringing pattern in output

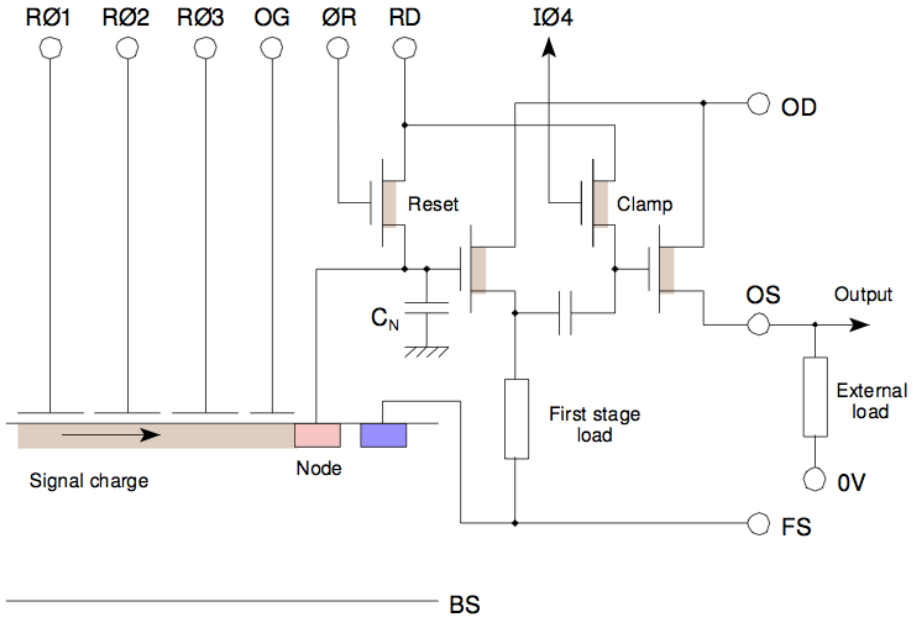


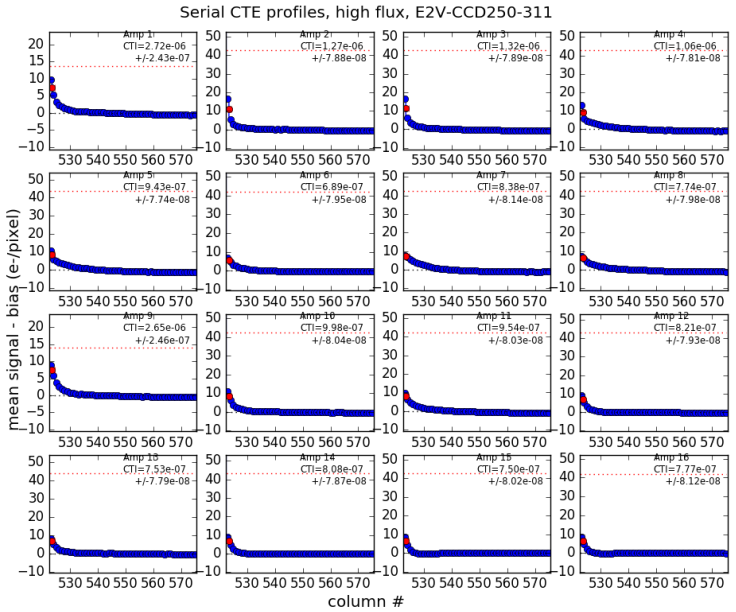


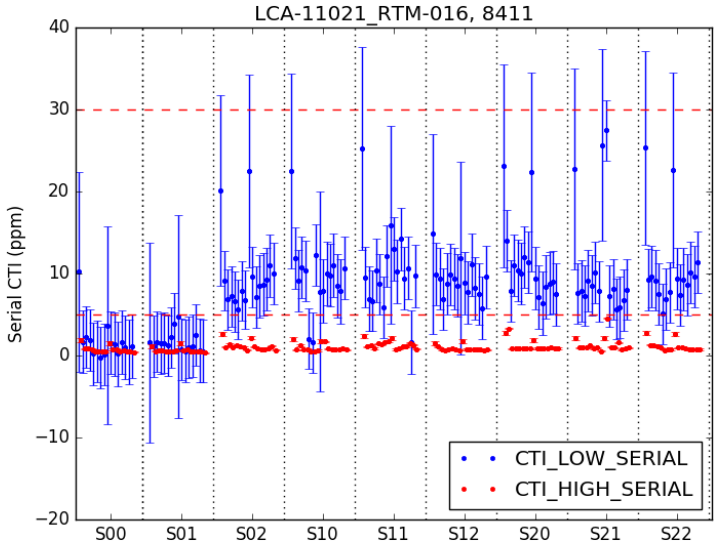


CTE and reset issue in E2V rafts

- Long tail after end of “flat” frame
- Seen in some channels at SLAC first
- Affected massively RTM-016 at BNL

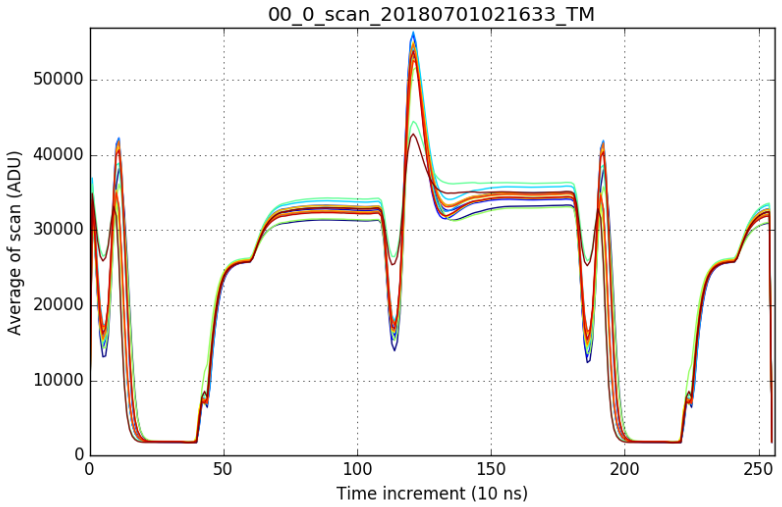


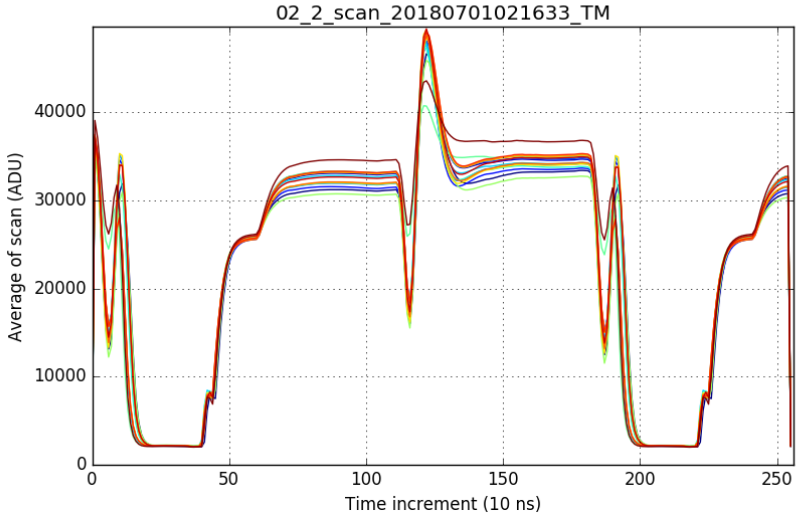


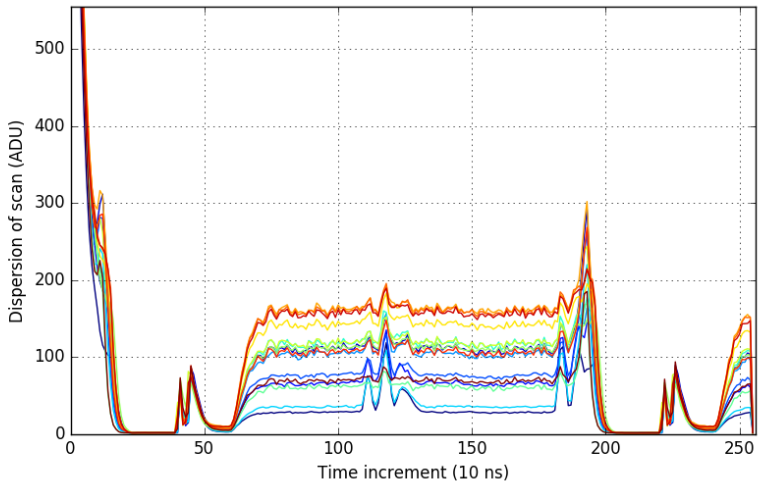


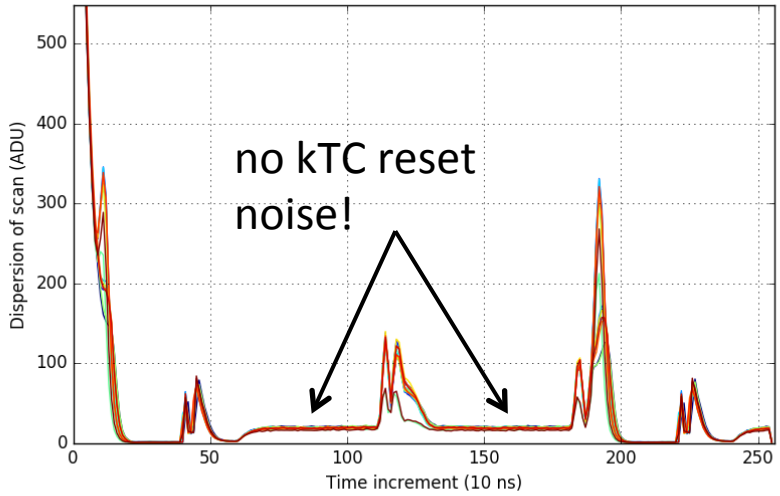
CTE and reset issue in E2V rafts

- Statistics on scan mode + ASPIC in transparent mode

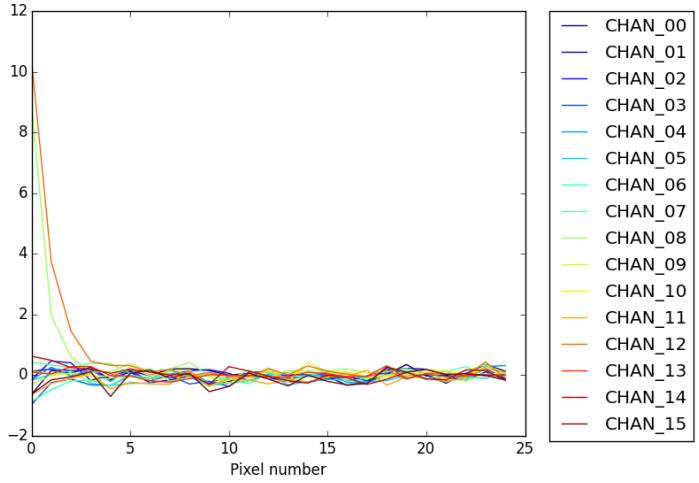






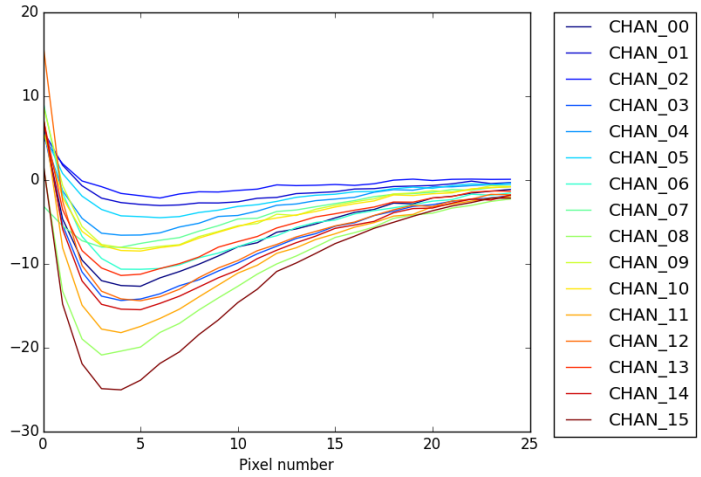


CTE and reset issue in E2V rafts

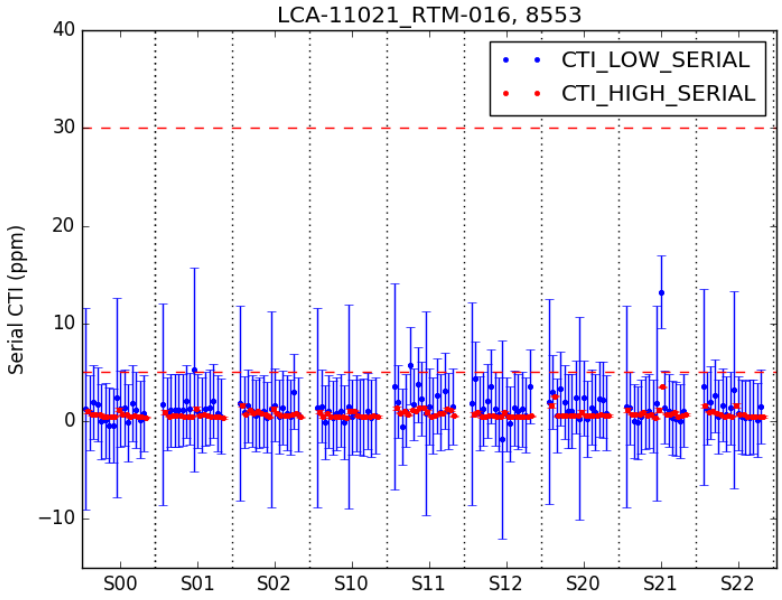


← RG-high at 11.7 V

RG-high at 11.0 V →

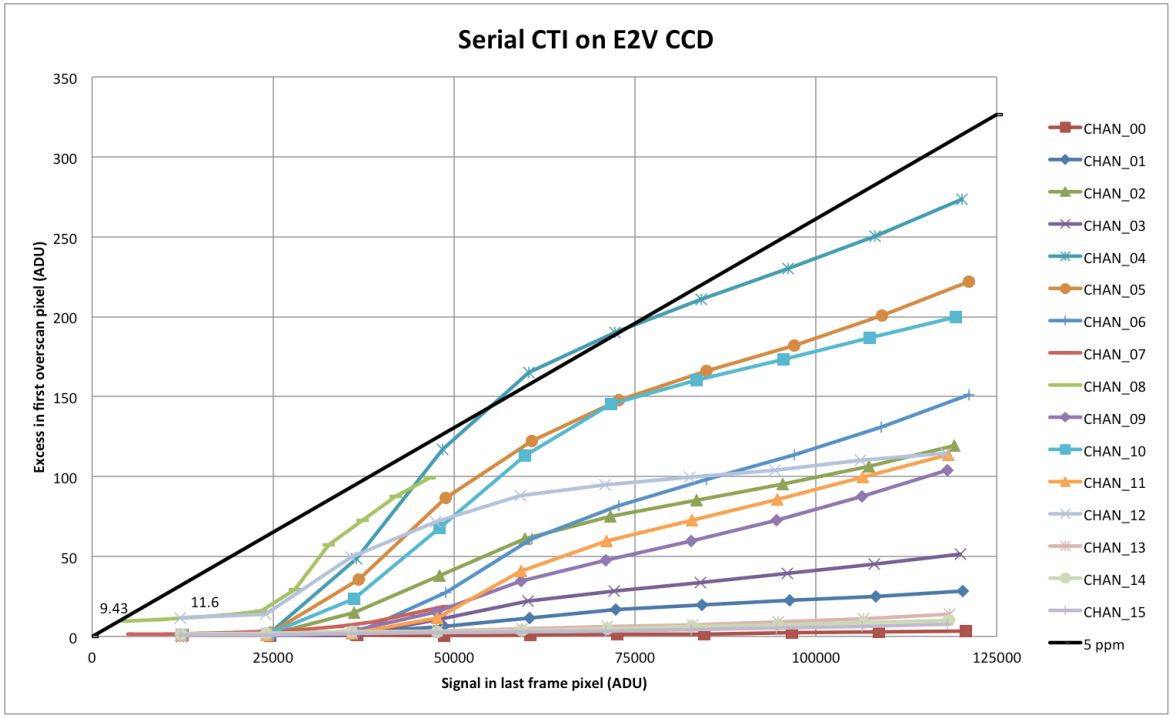


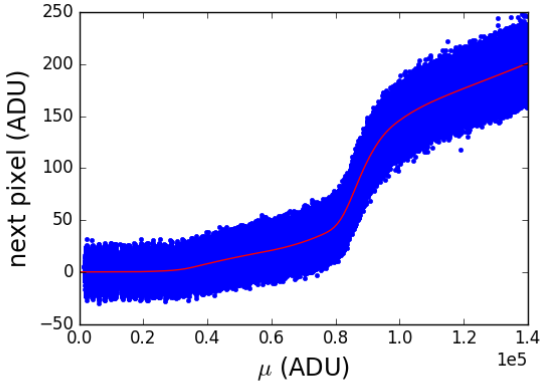
- Zener diode for safety between clock rails, <12 V amplitude nominally, threshold decreases with temperature: 10.7 V at -30C (REB temperature)
- Tested at LPNHE: CCD reset only happens if RG-high is close enough to RD (18 V)
- Set RG-low to +1 V instead of 0 V, can increase RG-high to +11.7 V instead of +10.7 V -> fixed reset and CTE

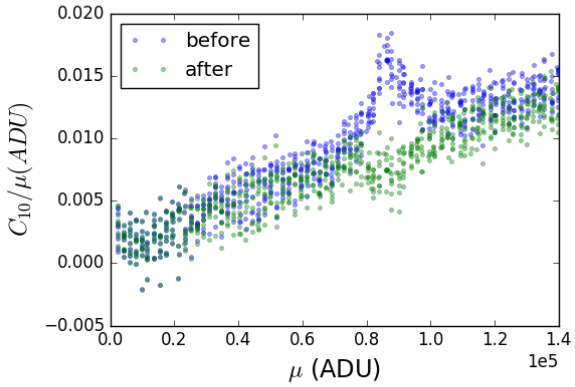


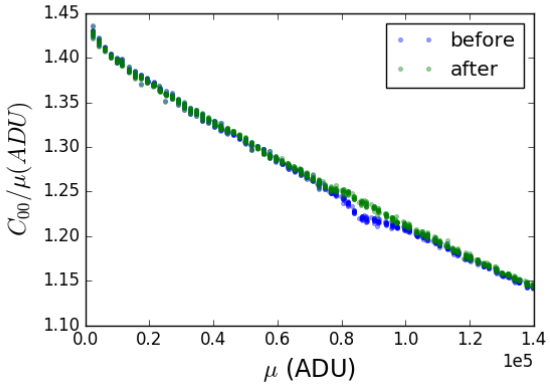
E2V sensors: traps and CTE jumps

- Traps: electrons in serial register are captured as soon as they are available, and released in the first empty pixel
- Serial Charge Transfer Efficiency depends on flux in some channels
- Fine look at Photon Transfer Curves in E2V sensors

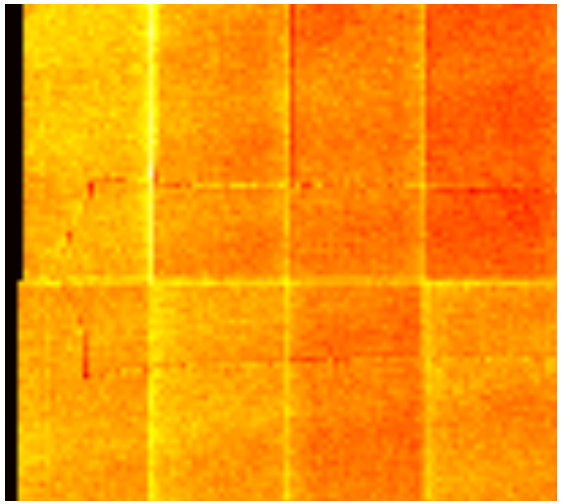


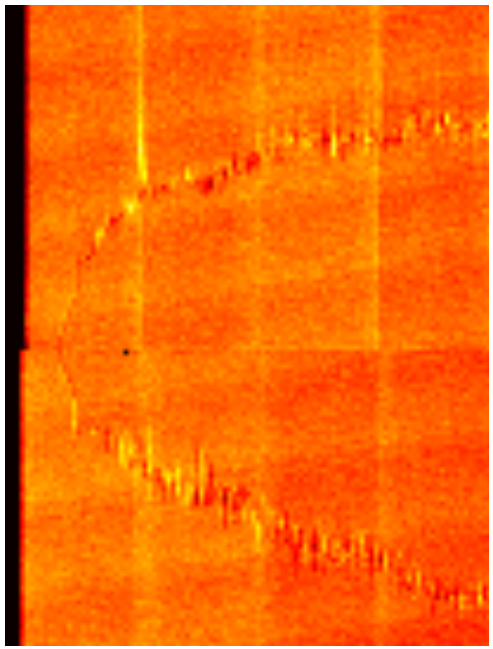


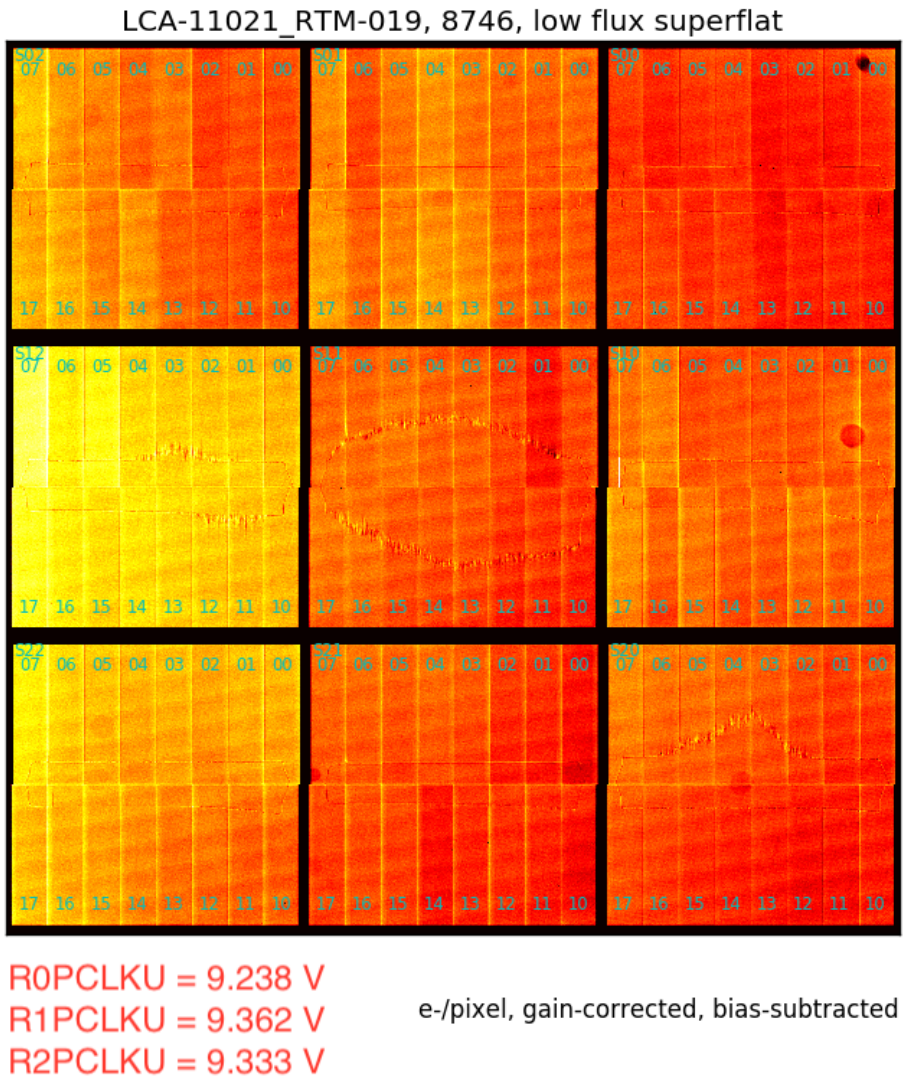




E2V sensors: tearing

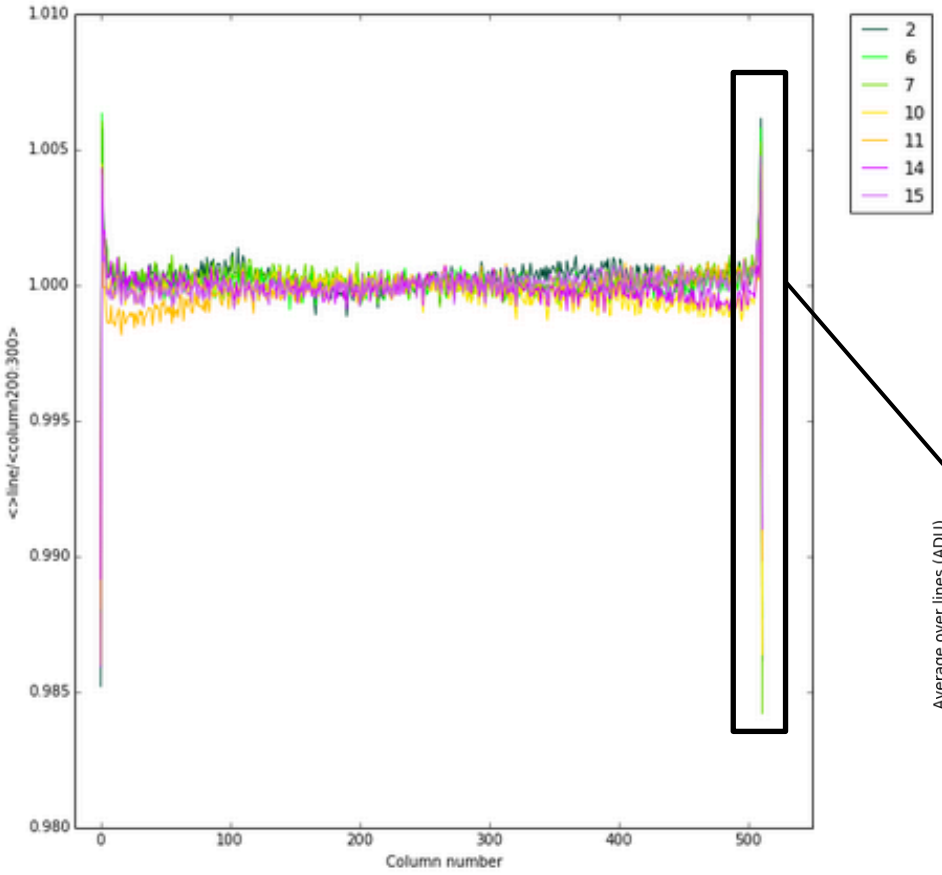


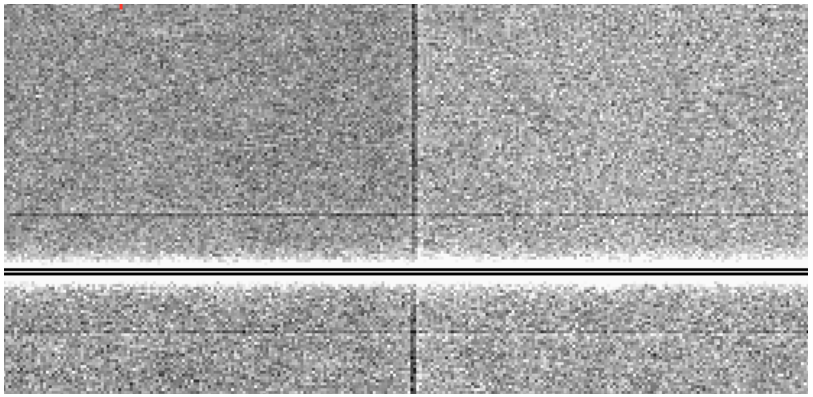


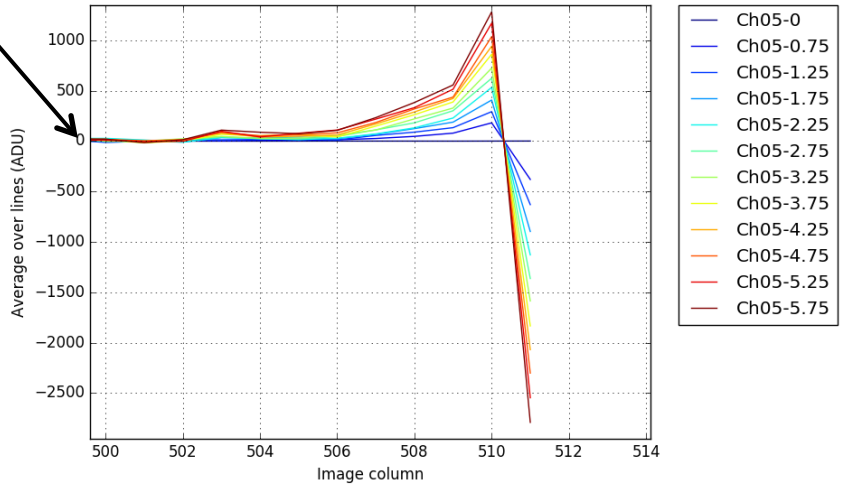


E2V sensors: segment edge pattern

- Lots of ad-hoc solutions to solve tearing: fast clear, decrease P-high, overlaps between clock phases
- Tearing pattern disappears, but “rabbit ears” pattern at segment edge remains

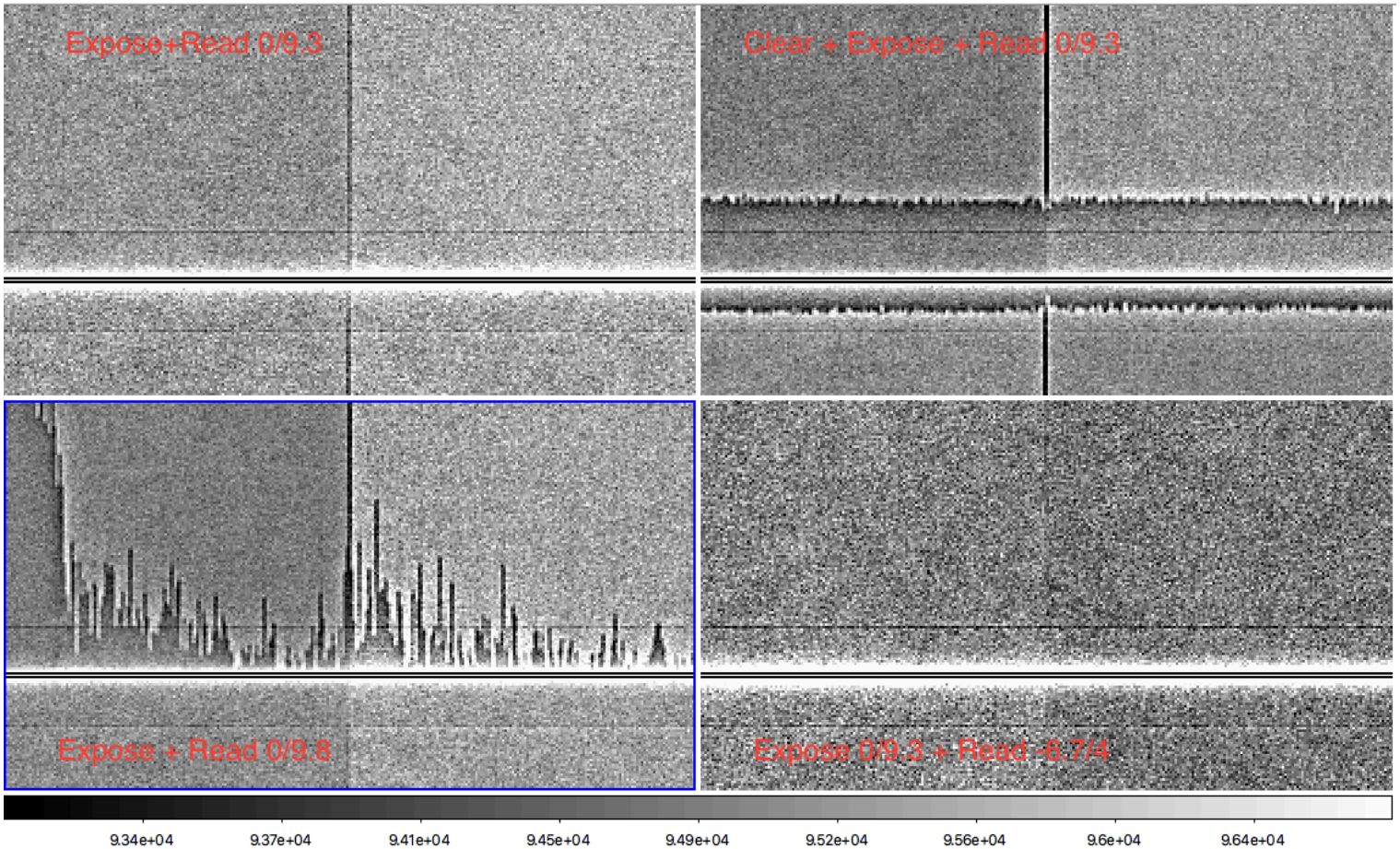






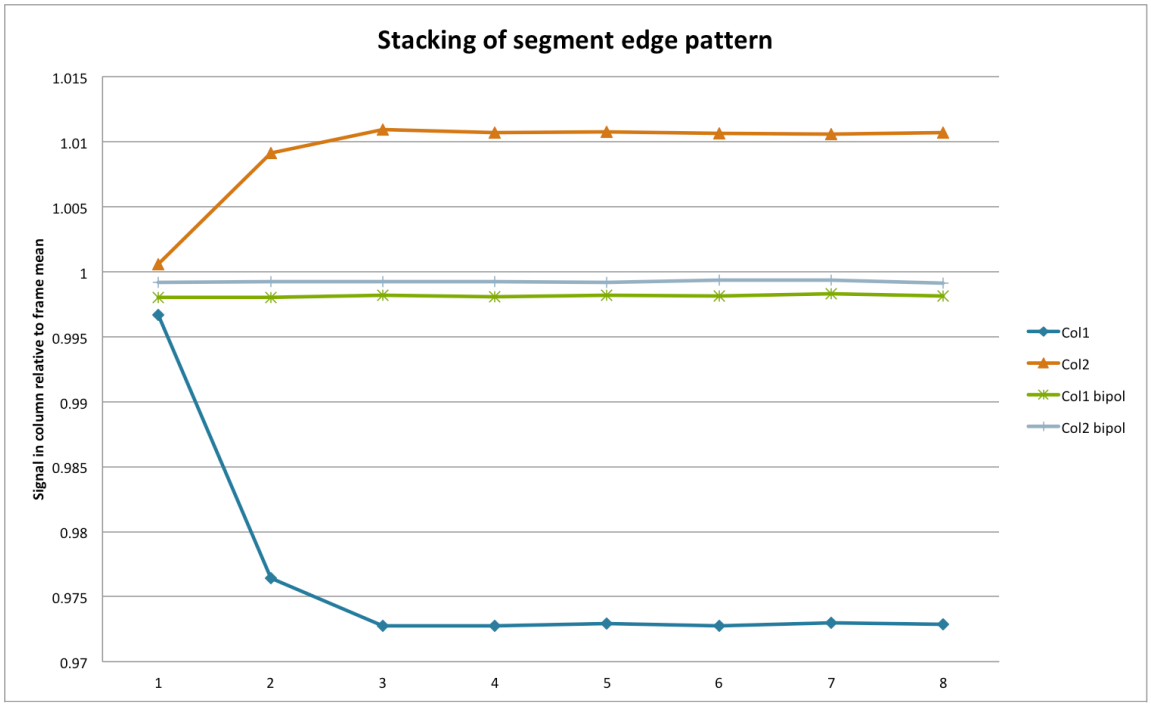
E2V sensors: segment edge pattern

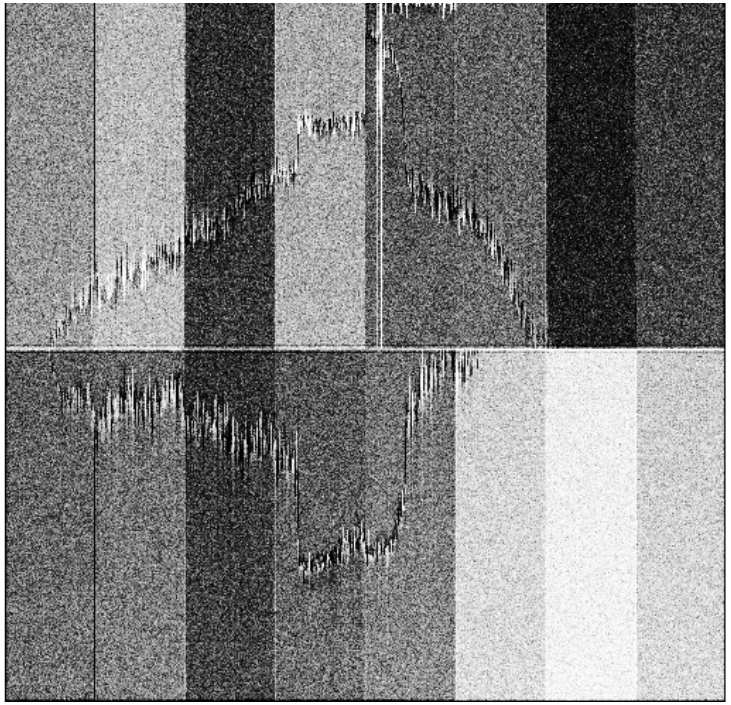
- Continuity between tearing patterns and segment edge pattern
- Shifting to bipolar readout with P-low ≤ -6.5 V removes the segment edge pattern



E2V sensors: tearing

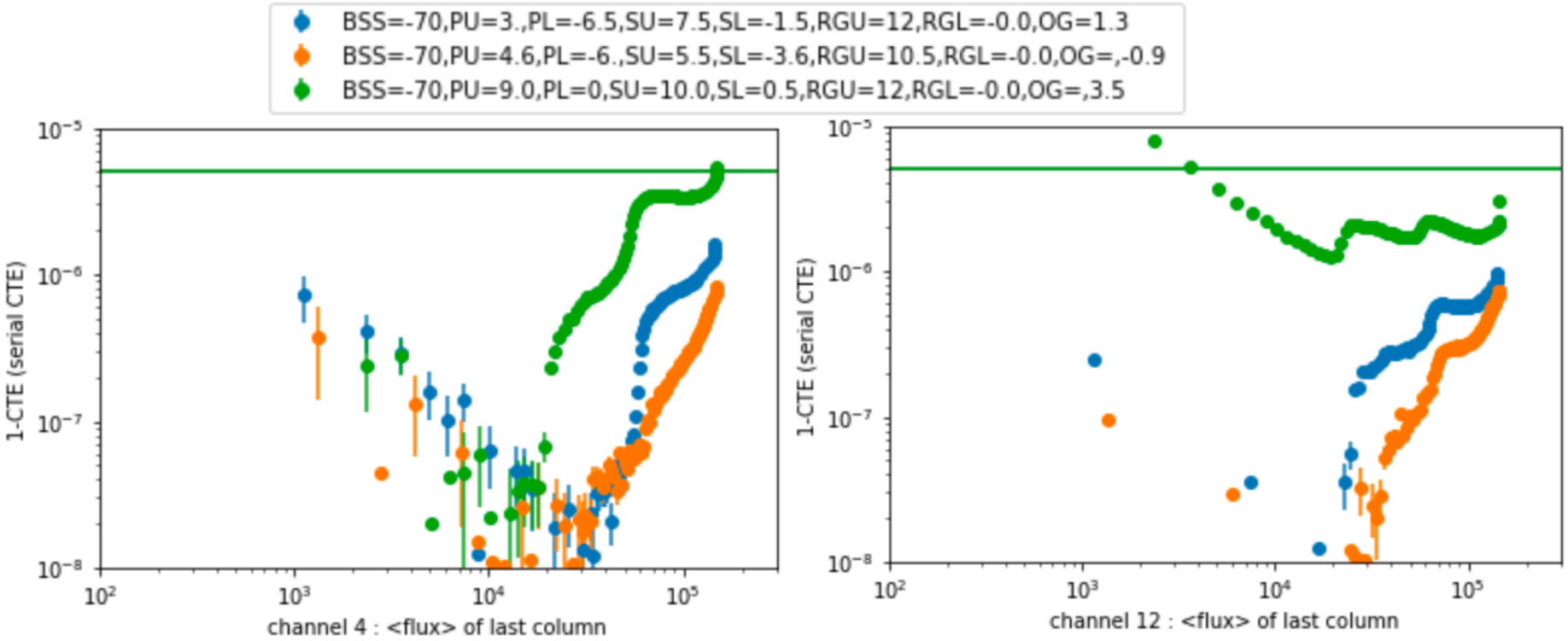
- In most sensors, using parallel clocks with P-low = -7 V is sufficient to remove the patterns
- In some cases a purge right before each frame is required to get rid of holes
- Purge = put all parallel clocks to < -7 V for ~ 2 ms = put the sensor in inversion (front-side surface becomes conductive for holes)





E2V sensors: the case for bipolar clocking

- Running with bipolar clocks had the unexpected effect to remove traps and jumps in serial CTE
- Cost of running in bipolar clocking: lower voltage difference between front and back of sensor = weaker drift field -> need to lower BSS



E2V sensors: optimizing bipolar voltages

- For P-low = - 7 V, all other voltages on the sensor need to be adjusted: set of rules given by E2V
- Additional constraint: parallel clock used for reset of second stage in E2V CCD output
- Check with Photon Transfer Curves for multiple configurations: linearity, full well, blooming