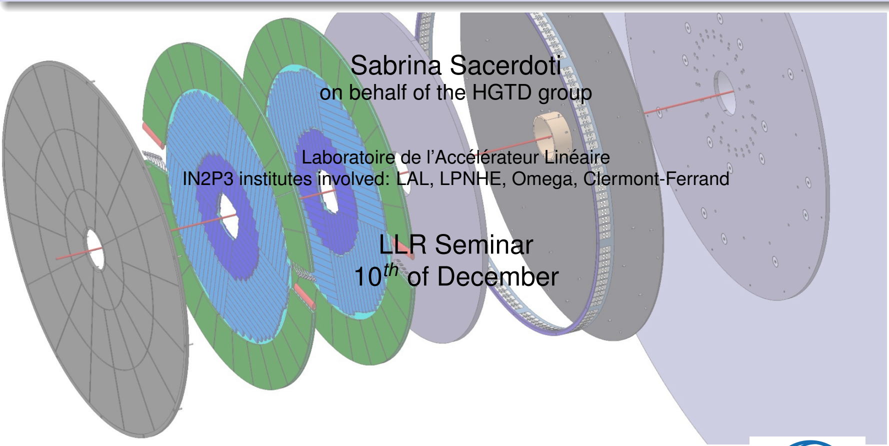
The ATLAS High-Granularity Timing Detector



Sabrina Sacerdoti
on behalf of the HGTD group

Laboratoire de l'Accélérateur Linéaire
IN2P3 institutes involved: LAL, LPNHE, Omega, Clermont-Ferrand

LLR Seminar
10^{th} of December

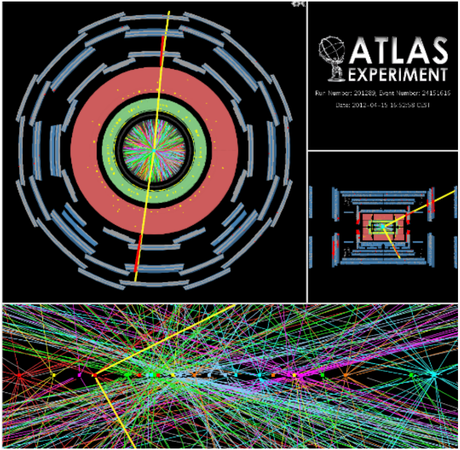
LABORATOIRE DE L'ACCÉLÉRATEUR LINÉAIRE

ATLAS EXPERIMENT

Contents

The High-Luminosity LHC

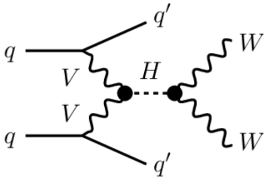
- The HL-LHC :
  - will start operation in 2026
  - instant luminosity $5 - 7\times$ nominal
  - integrated luminosity $10\times$ LHC
- Pileup is one of the most difficult challenges of the HL-LHC
- ATLAS Upgrade involving
  - new electronics in LAr and Tile
  - improved TDAQ
  - improved muon trigger/tagging
  - ITk: tracking up to $|\eta| = 4.0$
  - HGTD



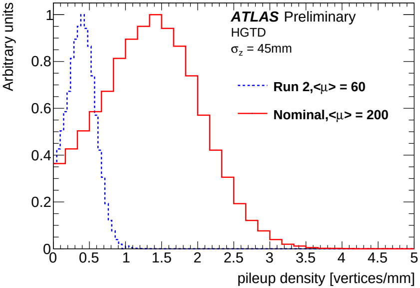
Key aspect for ATLAS analysis: maintain the track-vertex association performance in spite of the harsh environment

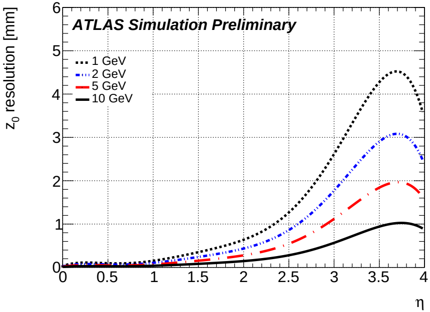
Motivation: beam conditions and z_0

- Increased luminosity at the HL-LHC:
  - expected $\langle\mu\rangle = 200$
  - average interaction density $\sim$ 1.8 vtx/mm



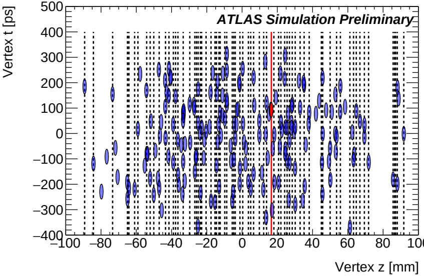
- The z_0 resolution worsens with $|\eta|$:
  - several vertexes could be merged
  - degradation of performance in forward jet reconstruction (i.e. critical for VBF signals)

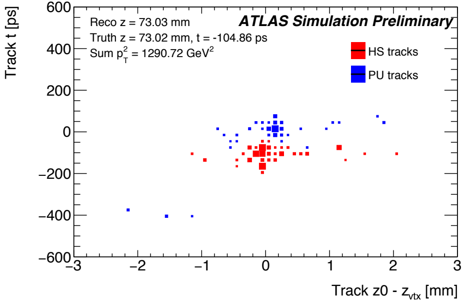




Motivation: precise timing measurements

- An additional dimension (4D) in existing detectors can provide a new handle on increased interactions per mm
- Expected nominal HL-LHC beam conditions: $\sigma_z = 45$ mm and $\sigma_t = 175$ ps
- Assigning a time to a track with a small enough time resolution would boost the discrimination power of ATLAS ($\sim$ 6 times for $\sigma_t = 30$ ps)





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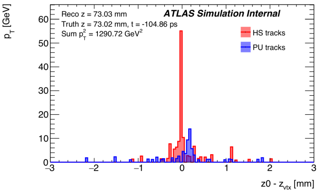
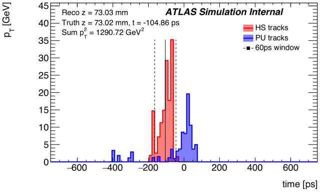
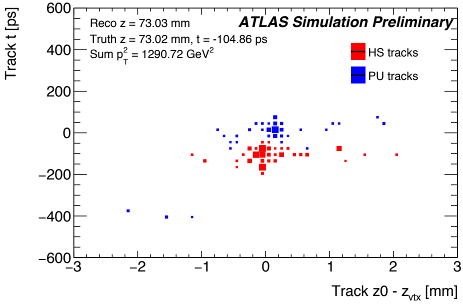
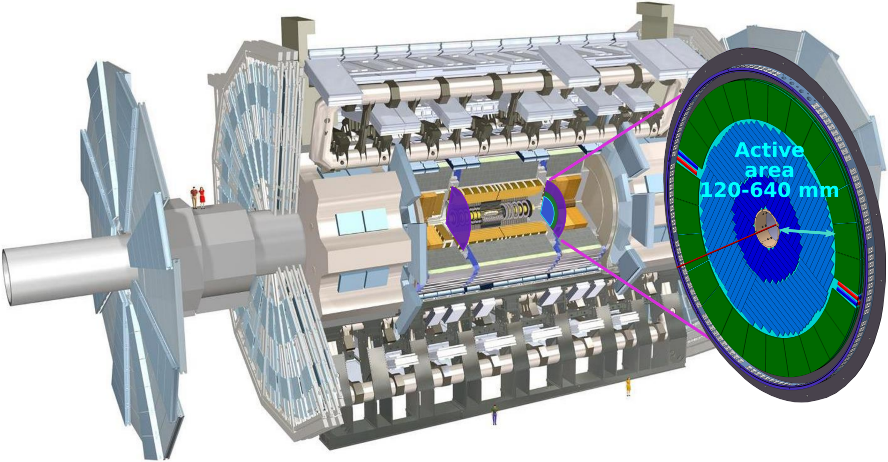






The High-Granularity Timing Detector

The HGTD will provide time measurements for objects in the forward regions of the ATLAS detector



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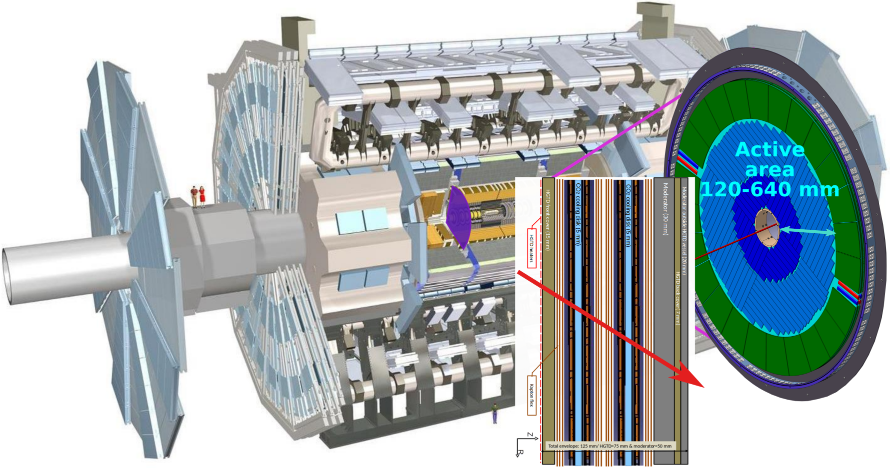


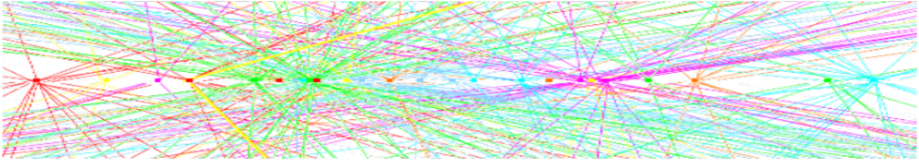
The HGTD: timing in ATLAS

General parameters:

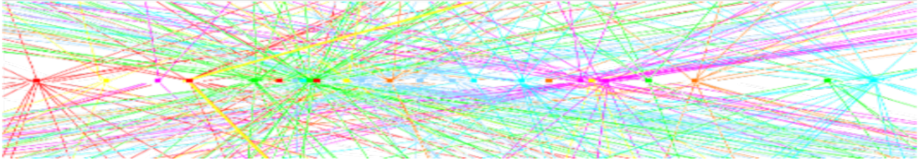
- $2.4 < |\eta| < 4.0$
- Active area 6.3 m^2 (total)
- Design based on $1.3 \times 1.3\,\mathrm{mm}^2$ silicon pixels ($2 \times 4\,\mathrm{cm}^2$ sensors)
  $\rightarrow$ optimised for $<$ 10% occupancy and small capacitance
- Radiation hardness up to 5.1 10^{15} n_{eq}/cm^2 and 4.7 MGy
- Number of hits per track:
  - 2 in $2.4 < |\eta| < 3.1$
  - 3 in $3.1 < |\eta| < 4.0$
- Inner ring to be replaced at half life-time of HL-LHC

Goal:

- Resolve close-by vertices
  - small timing resolution ($\sim$few 10s of picoseconds).
- Provide minimum bias trigger
- Instantaneous and unbiased luminosity measurement

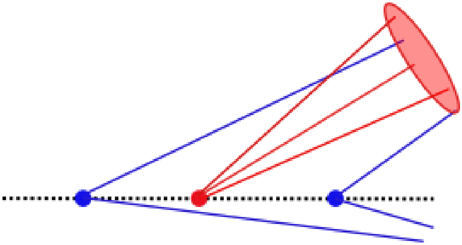


Performance Studies



Object Selection with Timing Information

- $\langle \mu \rangle \sim 60$
- $\Delta Z > \sigma_{z_0}$



- Example:
  pileup tracks in a forward jet

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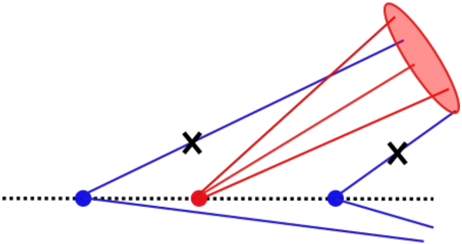

- Example:
  pileup tracks in a forward jet
- Well separated vertices:

$$\frac{|z_0 - z_{vtx}|}{\sigma_{z_0}} < 2$$

Object Selection with Timing Information

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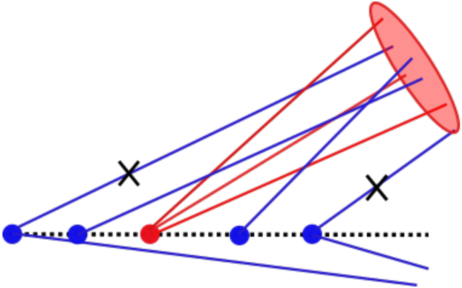

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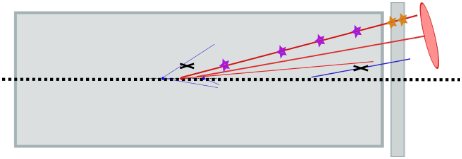

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Object Selection with Timing Information

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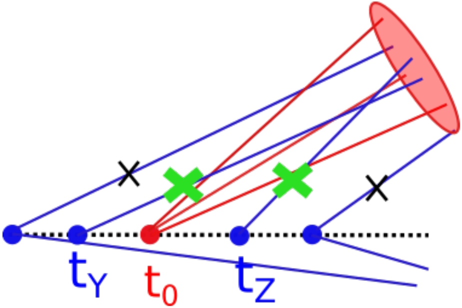
- $\Delta t > \sigma_t$



- Example:
  pileup tracks in a forward jet
- Well separated vertices:

$$\frac{|z_0 - z_{vtx}|}{\sigma_{z_0}} < 2$$

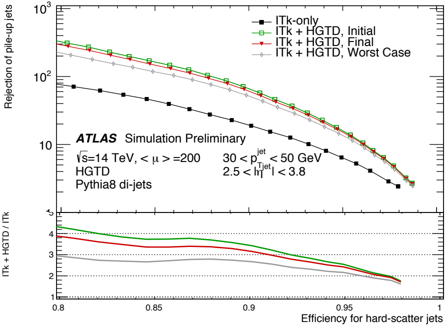
- Timing information:

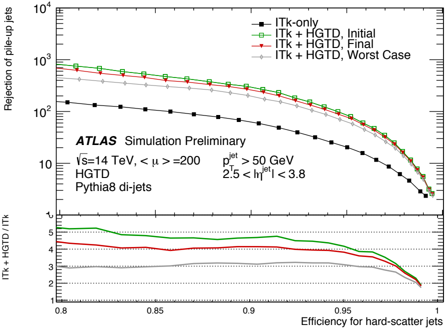
$$\frac{|t - t_0|}{\sigma_t} < 2$$

Pileup jet rejection

- Tagging pileup jets based on
- Fraction of p_T of a jet coming from PV tracks:

$$R_{p_T} = \frac{\Sigma p_T^{\mathrm{trk}}(\mathrm{PV}_0)}{p_T^{\mathrm{jet}}}$$

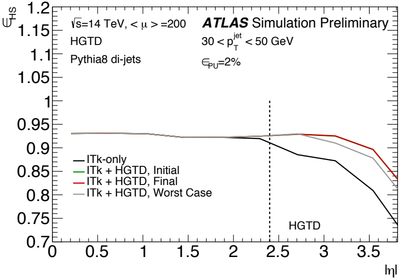


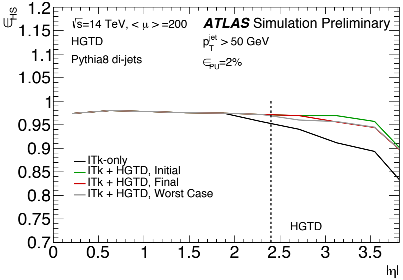


- Improving id of PV0 tracks improves the discrimination power of R_{p_T}
- Up to a factor of 4 higher pu-jet rejection with the use of timing information
- More robust pileup rejection

Hard-scatter jet efficiency

- Tagging of jets coming from the HS vertex
- Also using R_{p_T}
- Fixed pileup-jet efficiency of 2% (rejection factor of 50)

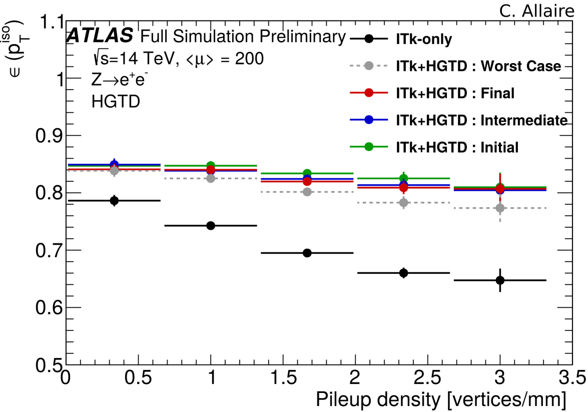




- The HGTD recovers the 10-30% drop in efficiency observed in the forward region.
- Allows to maintain similar pileup-jet suppression performance as in the central barrel.

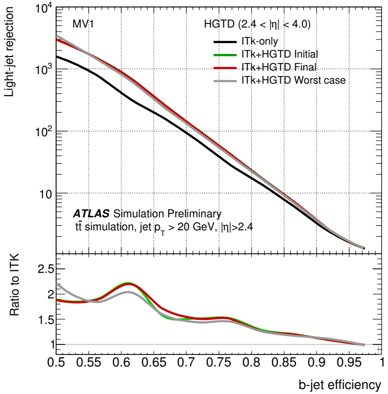
Lepton Isolation

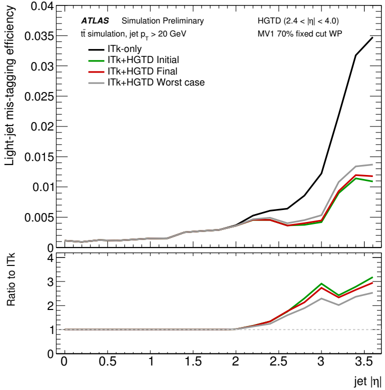
- The HGTD can be used to assign a time to leptons in the forward region.
- Isolation efficiency: probability that no track with $p_T > 1$ GeV is reconstructed within $\Delta R < 0.2$ of the lepton track.



- Efficiency above 80% even at higher pileup density

Heavy-flavour tagging

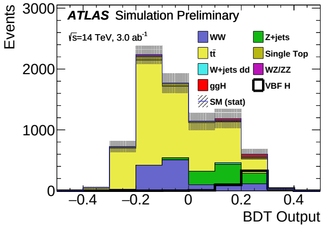


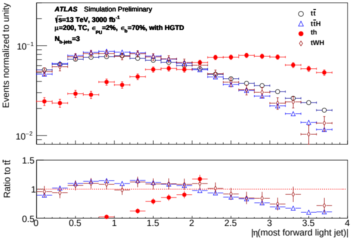


- Addition of the HGTD removes the majority of pileup tracks from the track selection.
- For a b-tagging efficiency of 70%(85%), the light-jet rejection for MV1 is increased by approximate factors 1.5 (1.2)
- The improvement could be higher in processes with more forward b-jets.

Impact in Analyses

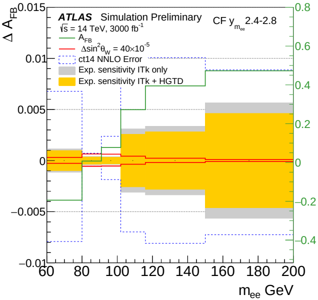
VBF $H \to WW^*$ $\sim$ 8% improvement

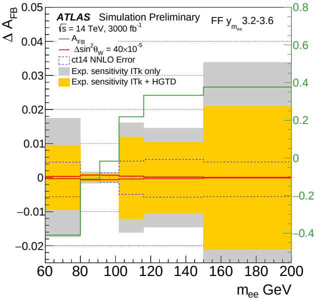




tH sensitivity:

Improved b-tagging $+$ PU rejection $\to$ 11% improvement



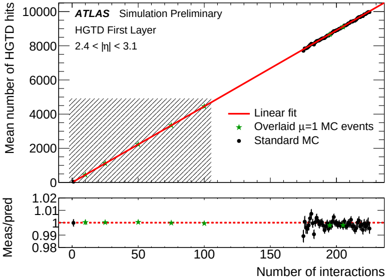


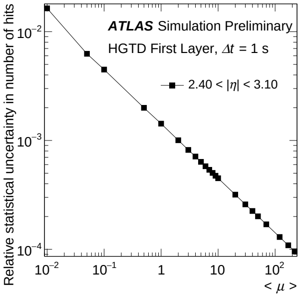
Weak mixing angle sensitivity:

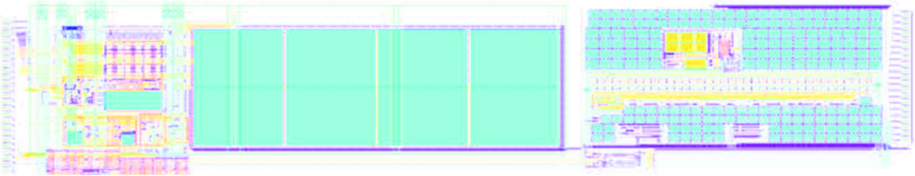
Improved lepton isolation $\to$ 13% improvement in exp. uncertainty

Luminosity measurement

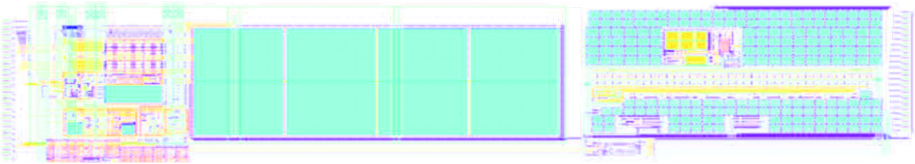
- The luminosity uncertainty could limit the accuracy of some high precision measurements at the HL-LHC
- Need measurement as precise as in Runs I & II (currently 2.4%)
- Key characteristics of HGTD:
  - Fast signals → N_{hits} per bunch-crossing
  - High granularity → low occupancy → $\langle N_{hits} \rangle \propto \langle pp_{int} \rangle$
- Unbiased and high statistics per-BC measurement, available online and offline.



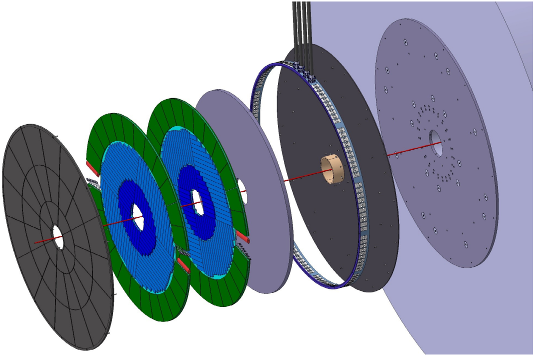




Detector Design



Mechanical Design

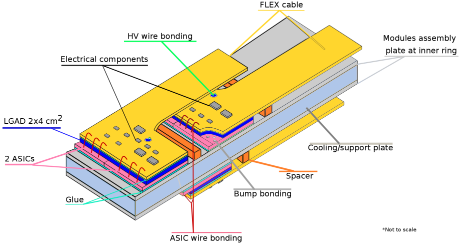


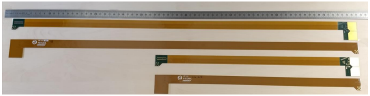
Design challenges:

- Strict spatial constrains:
  - Thickness in Z within 75 mm
  - Allow space for ITk services at $R \sim 1$ m
  - Cooling services
- Thermal isolation: covers must be above condensation temperature (~ 17 ℃)
- Weight ~ 350 kg per endcap

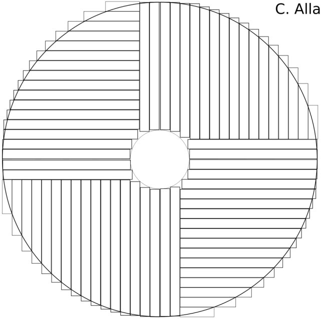
HGTD module

- sensor bump-bonded to 2 ASICs
- wire-bonded to a flex cable (input/output and power)
- placed on support stave





C. Allaire



Highly optimised read-out row geometry

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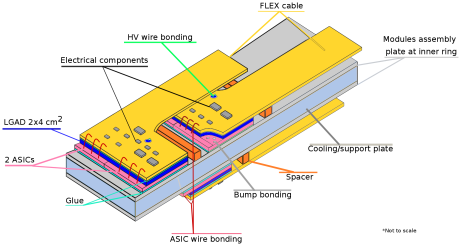

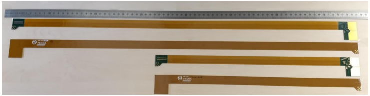

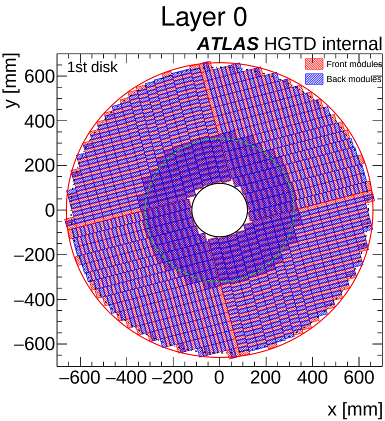

- High overlap up to $R \sim 320$ mm
- Optimized coverage in the edges
- Rotation $\pm 15°$ improves uniformity

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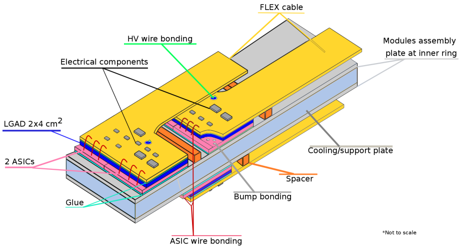

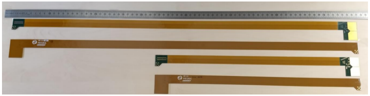

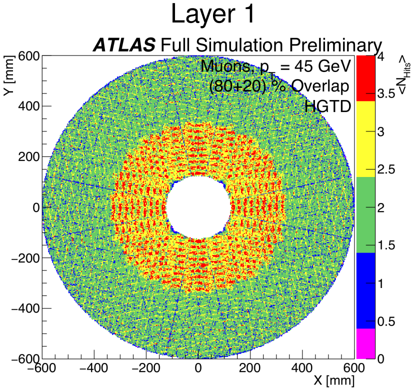

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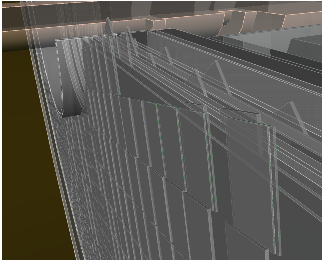
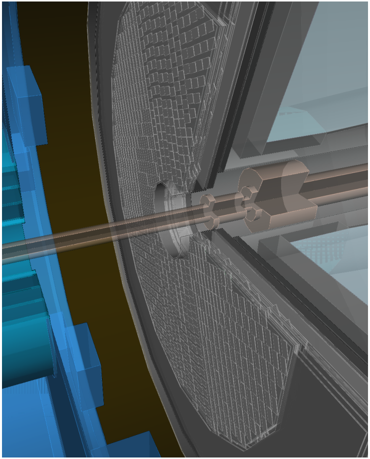
- Optimized coverage in the edges
- Rotation $\pm 15°$ improves uniformity

New Geant simulation for TDR

- Geant4 implementation of HGTD geometry for TDR
- Detailed implementation:
  - module: ASIC, active and inactive layers of LGAD, glue
  - different mechanical support structures
  - electronic boards
  - moderator





Time Resolution

Contributions to the timing resolution:

$$\sigma_T^2 = \sigma_S^2 + \sigma_{TW}^2 + \sigma_{jitter}^2 + \sigma_{clock}^2$$

- σ_S
  - Landau fluctuations in the energy deposits of the particles
  - non-uniformity of the energy deposit along the particle path; depends on the sensor thickness

Time Resolution

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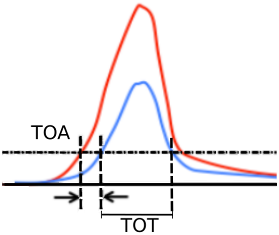
- σ_S
- $\sigma_{TW}^2 = [\frac{V_{th}}{S/t_{rise}}]_{RMS} \propto [\frac{N}{dV/dt}]_{RMS}$



- Variations due to differences in the amplitude of the signal.
- Expected to be negligible after applying an offline correction based on measuring the TOT.

Time Resolution

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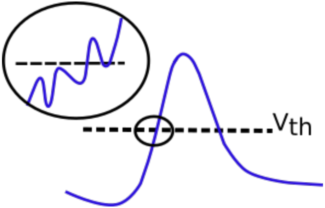
- σ_S
- $\sigma_{TW}^2 = [\frac{V_{th}}{S/t_{rise}}]_{RMS} \propto [\frac{N}{dV/dt}]_{RMS}$
- $\sigma_{jitter}^2 = \frac{N}{dV/dt} \sim \frac{t_{rise}}{S/N}$



Variations due to noise in the signal

Time Resolution

Contributions to the timing resolution:

$$\sigma_T^2 = \sigma_S^2 + \sigma_{TW}^2 + \sigma_{jitter}^2 + \sigma_{clock}^2$$

- σ_S
- $\sigma_{TW}^2 = [\frac{V_{th}}{S/t_{rise}}]_{RMS} \propto [\frac{N}{dV/dt}]_{RMS}$
- $\sigma_{jitter}^2 = \frac{N}{dV/dt} \sim \frac{t_{rise}}{S/N}$
- σ_{clock}^2 contribution from the clock distribution
  - High Frequency: bunch to neighbouring bunch 'jitter'
  - Low frequency: drift over longer periods ($\sim$ 1 ms), can be corrected offline with calibration
  - Expected to be below 10 ps in total

Time Resolution

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- σ_S
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- $\sigma_{jitter}^2 = \frac{N}{dV/dt} \sim \frac{t_{rise}}{S/N}$
- σ_{clock}^2 contribution from the clock distribution < 10 ps

Additional contributions from TDC expected to be negligible.

Time Resolution

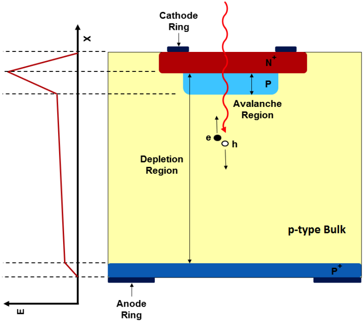
Contributions to the timing resolution:

$$\sigma_T^2 = \sigma_S^2 + \sigma_{TW}^2 + \sigma_{jitter}^2 + \sigma_{clock}^2$$

- σ_S
- $\sigma_{TW}^2 = [\frac{V_{th}}{S/t_{rise}}]_{RMS} \propto [\frac{N}{dV/dt}]_{RMS}$
- $\sigma_{jitter}^2 = \frac{N}{dV/dt} \sim \frac{t_{rise}}{S/N}$
- σ_{clock}^2 contribution from the clock distribution < 10 ps

Total time resolution per track $= \sigma(hit)/\sqrt{N_{hits}}$ goal < 30 ps

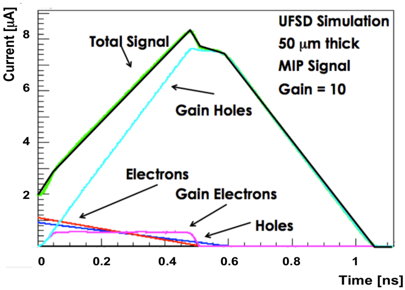
Low Gain Avalanche Diode (LGADs)



- n-on-p planar silicon detectors
- A thin highly-doped p-layer provides an internal gain (10-50)
- lower noise amplification improves S/N
- excellent timing resolution

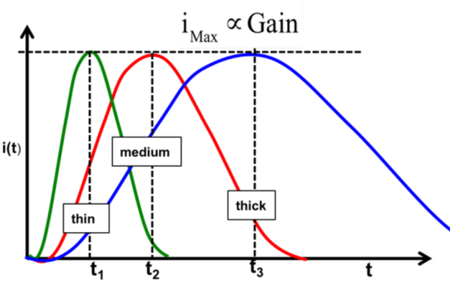
LGAD signal

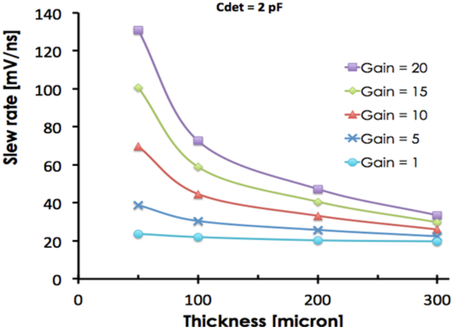
- Key aspect: rise time (t_{rise})
- $t_{rise} \sim 0.5$ ns
- Smaller rise time from:
  - thinner pads
  - larger gain



LGAD Gain

Gain (g) = charge of LGAD wrt diode



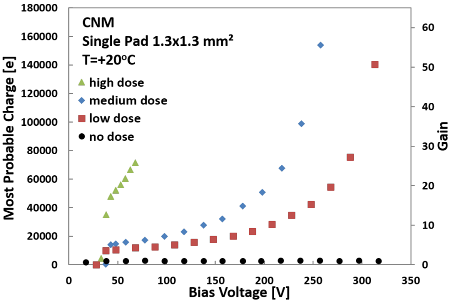


- Independent of the thickness
- 50μm is baseline and 35μm under study
- Depends on the characteristics of the additional p-layer

LGAD: gain vs bias voltage

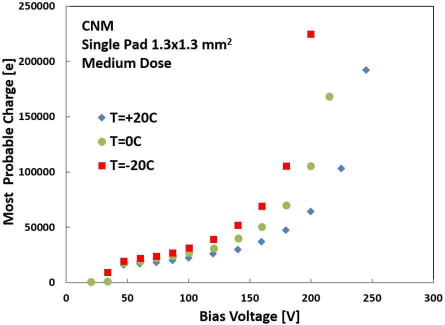
CNM (Barcelona) non-irradiated sensors

Various dopings



- The gain increases with doping
- Breakdown voltage is lower with higher dose
- Target gain $\sim 10 - 20$

Different temperatures



Operation at low temperature will allow:

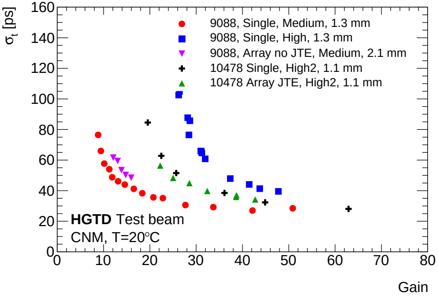
- higher gain
- at lower bias voltage
- reduced leakage current after irradiation

Target $\sim -35\,^{\circ}\mathrm{C}$

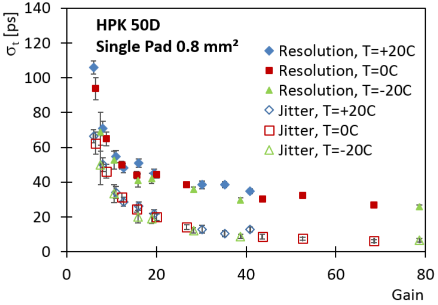
LGAD: time resolution vs gain

CNM (Barcelona) and HPK (Hamamatsu) non-irradiated sensors

Room temperature - CNM



Temperature dependence - HPK

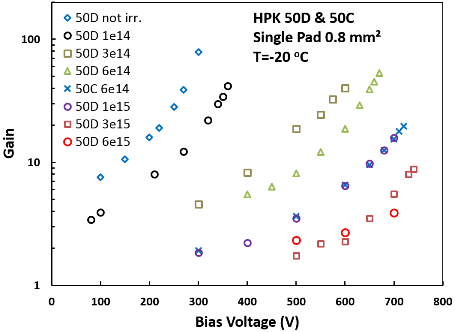


- Time resolution of 30 ps achieved for CNM and HPK sensors
- Jitter decreases with gain
- Limited by non-uniformity in energy deposits (σ_s)

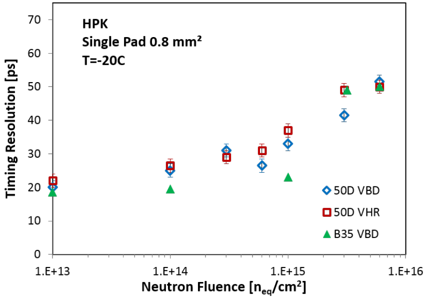
LGAD performance after irradiation

- Loss of doping in the gain layer $\rightarrow$ degradation of gain
- faster signal
- increase of leakage current (up to a few μA)

Gain HPK



Time resolution - HPK

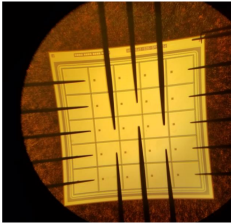


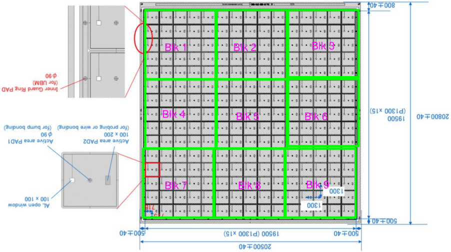
- Small gain (from bulk) after $10^{15} \mathrm{n}_{eq}/\mathrm{cm}^2$
- need to increasing the bias voltage

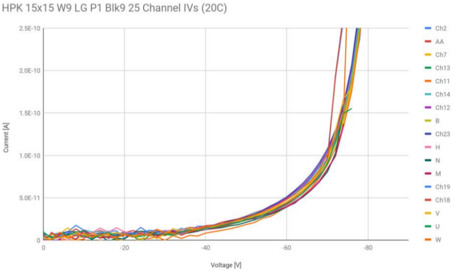
- $\sigma_t < 50$ ps up to $5 \times 10^{15} \mathrm{n}_{eq}/\mathrm{cm}^2$
- bias voltage at 10% below break down

LGAD testing for HGTD

- On-going tests of three vendors: HPK, FBK and CNM
- Testbeam results of single-pad and 2×2 sensors
- Radiation hardness: boron/gallium implanted, carbon diffused
- Lab studies on going for 5×5 arrays
- First IV curves obtained for 15×15 array





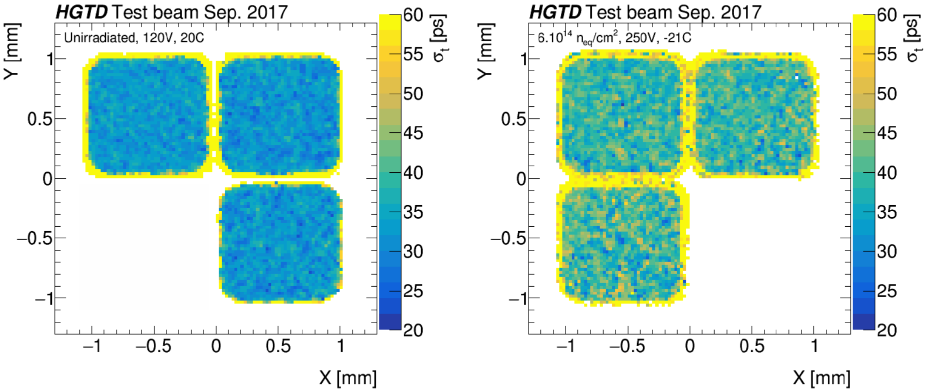


Test-beam results: time resolution

- September 2017 test beam with 120 GeV pions at CERN-SPS
- CNM 2×2 arrays, each pad $1.063 \times 1.063\,\mathrm{mm}^2$
- Test-beam 2016 paper available in arxiv 1804.00622

Non-irradiated

$6 \times 10^{14} \mathrm{n}_{eq}/\mathrm{cm}^2$



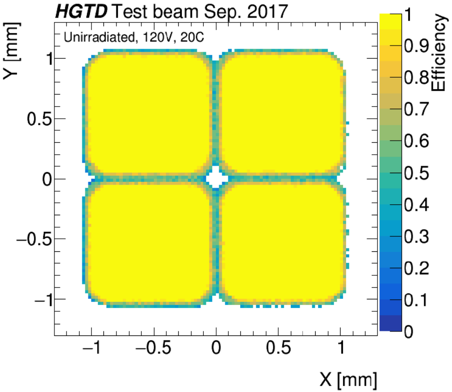
Average $\sigma_t \sim 30$ ps

Average $\sigma_t \sim 40$ ps

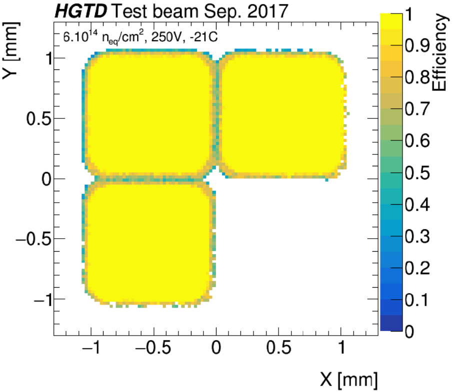
Test-beam results: efficiency

- September 2017 test beam with 120 GeV pions at CERN-SPS
- CNM 2 $\times$ 2 arrays, each pad 1.063 $\times$ 1.063 mm^2

Non-irradiated



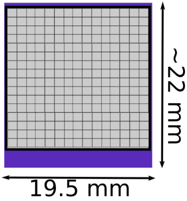
$6 \times 10^{14} \mathrm{n}_{eq}/\mathrm{cm}^2$



- Negligible inefficiency in the centre of the pads.
- Interpad area is not a dead region
- Also: cross-talk mostly negligible/$\sim$ 5% in irradiated sensors

ALTIROC ASIC

- The LGAD sensors will be read out by the ALTIROC
- specific ASIC designed for the HGTD
  - collaboration between Omega (design) and LAL (characterisation/test-beam)
- Bump-bonded to the sensor, it will read out 225 channels



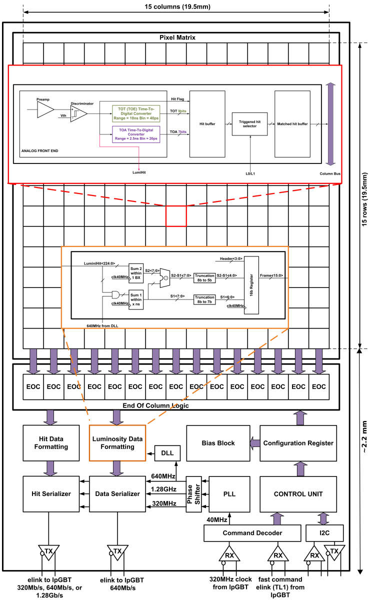
Requirements:

- Keep the excellent time resolution of the LGADs, $\sigma_{el} < 25$ ps
- Cope with a trigger latency of 10/35 μs for L0/L1 trigger
- TDC conversion within 25 ns
- Power consumption constrained by cooling power (sensors at -35℃)
- radiation hard

Development:

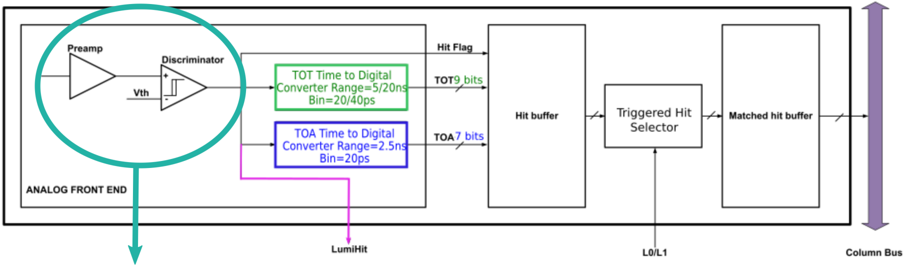
- ALTIROC0 single channel analog readout
- ALTIROC1 5×5 analog + digital channel readout
- ALTIROC2 15×15 expected submission end of 2019

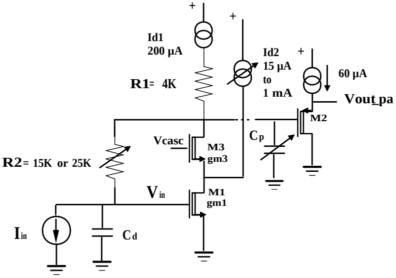
ASIC architecture



- single pixel readout (15 $\times$ 15)
- luminosity formatting block
- end-of-column logic
- off-pixel electronics:
  - Handling of input/output signals to peripheral electronics
  - clock distribution

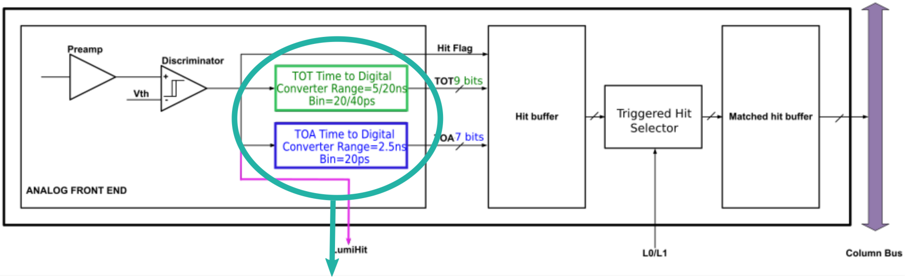
Single-pixel architecture





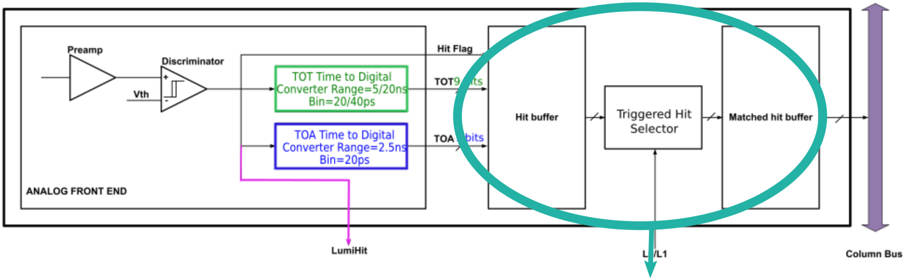
- Baseline: voltage sensitive preamplifier
- C_p to vary the signal speed
- Optimise t_{rise} to match the drift time of the sensor (0.5-1) ns to minimise jitter
- Fixed threshold discriminator
- Tested in ALTIROC0

Single-pixel architecture



- Time Of Arrival TDC (20 ps bin/2.5 ns range)
- Time Over Threshold TDC (40 ps bin/20 ns range)
- signal is also sent to the luminosity formatting unit
- ALTIROC1 tests started

Single-pixel architecture



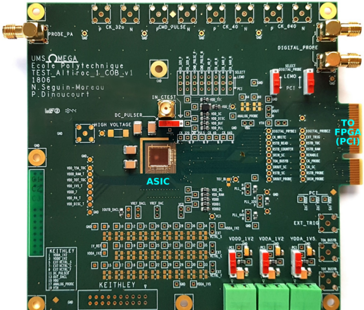
- store hit information until trigger
- select hit
- store until transfer
- First simple SRAM implemented in ALTIROC1

ALTIROC0 - ALTIROC1

Tests on-going on both ASIC iterations:

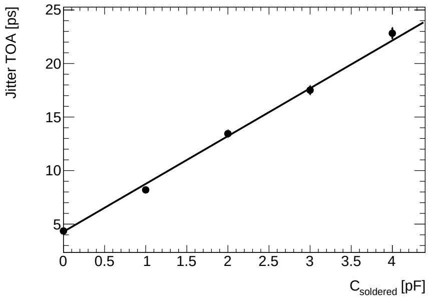
- 2 × 2 channels
- Analog readout electronics:
  - preamplifier
  - discriminator
- Voltage/VPA and transimpedance/TZ studied
- Bump-bonded to an LGAD sensor (testbeam)

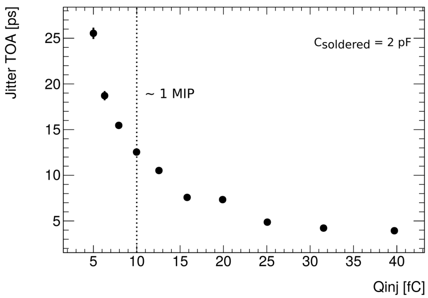
- 5 × 5 channels
- Same pramp+discri, added digital:
  - TOA and TOT TDCs
  - SRAM
- Phase shifter (independent)
- SC parameters transmited through PCI by an independent FPGA board
  → irradiation tests



Preamplifier Jitter

- Varies with the capacitance seen by the ASIC (board and sensor/soldered)
- Achieved jitter of $\sim$ 13 ps for $C_{soldered} = 2$ pF (total $C \sim 5$ pF)
- Sensor expected to provide at least 5 fC

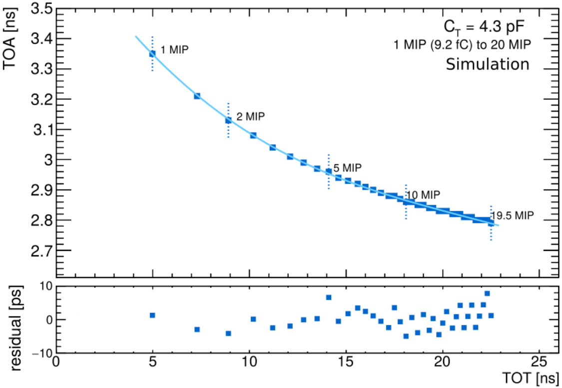




*generator jitter of 6 ps subtracted in both measurements

Time Walk correction

- Using measurement of the TOT (estimator of the pulse amplitude)
- Expected residual difference between simulation and measurement < 10 ps



Time Walk correction

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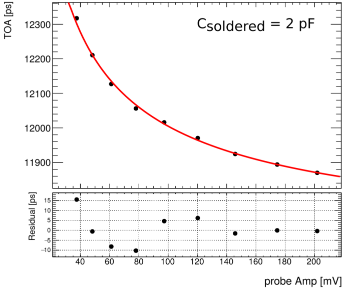
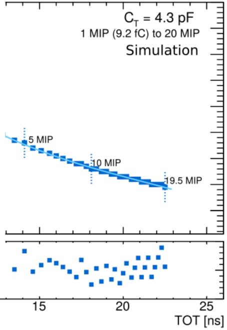
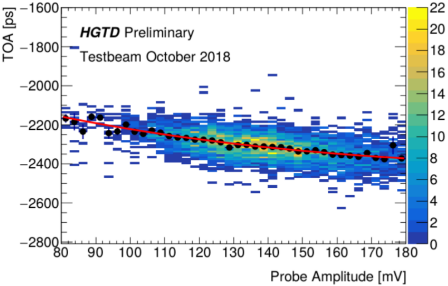


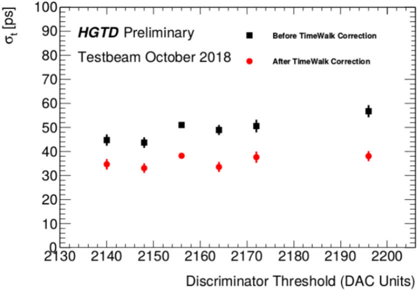


- ALTIROC0 showed good performance by itself but suffered from coupling that affected the TOT measurement when connected to the sensor.
- TW correction performes using the probe amplitude - studies on-going

Testbeam performance

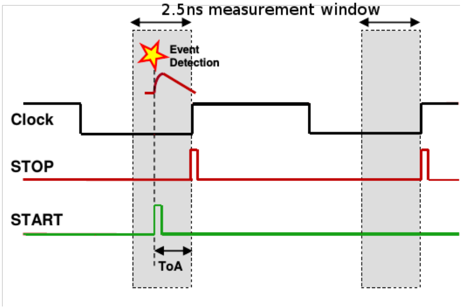
- ALTIROC0 bump-bonded to a non-irradiated LGAD
- TOT correction estimated using probe amplitude ($\propto$ preamplifier signal) $\rightarrow$ 30% improvement
- Time resolution corrected for time-walk $\sim$ 35 ps.

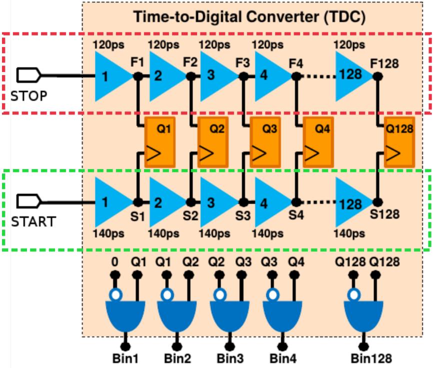




Time-to-Digital Converter

- Achieves a 20 ps resolution by combining two lines of fast (120 ps) and slow (140 ps) cells
- Vernier delay line configuration with a reverse START-STOP scheme
- Power saving: no consumption if no hit
- Implemented in ALTIROC1 - tests started!





Count the number of cells it takes for the stop signal to surpass the start signal.

Summary

- The HGTD is a Phase-II upgrade ATLAS project that will provide timing capability in the forward region.
- Compromise in the detector layout:
  - spatial/monetary constrains
  - goal to guarantee 3 hits per track for smaller radius (high η) and $\sim$ 30 ps resolution per track
- Performance studies:
  - have shown potential of having timing information in the forward region to improve pileup rejection
  - more complex studies could show further impact in analyses
- Aspects of the detector design to be demonstrated:
  - LGAD's radiation hardness needs to be tested up to 5.1 10^{15} n_{eq}/cm^2 (1.5 10^{15} n_{eq}/cm^2 tested so far)
  - validation of ASIC's demanding performance with a TDC, connected to a sensor (ALTIROC1)
  - optimisation of services given the small space available

Status

- Technical Proposal successfully reviewed by LHCC in June 2018
- Next major step: submission of the Technical Design Report by April 2019, where the technical feasibility of the detector should be demonstrated

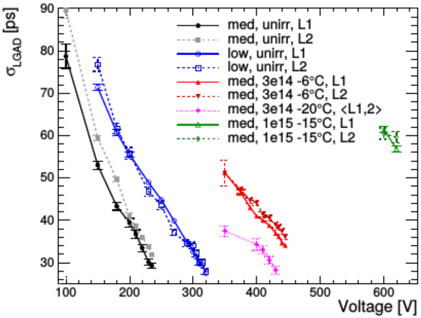
BACK UP

Overview of test beam results

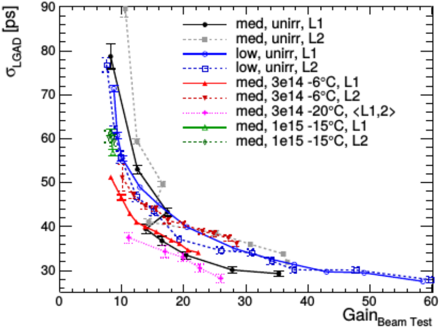
- Several test beam campaigns since 2016 (sensors from CNM and HPK).
- Achieved time resolution below 30 ps

CNM - 45 μm thick single pads[1]

σ_t vs V_{bias}



σ_t vs gain

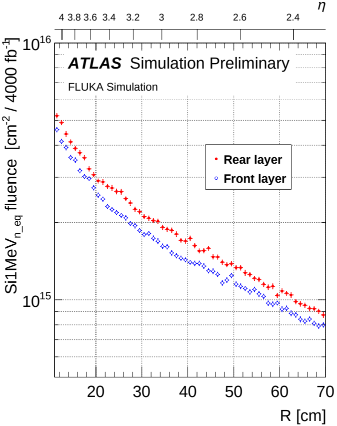


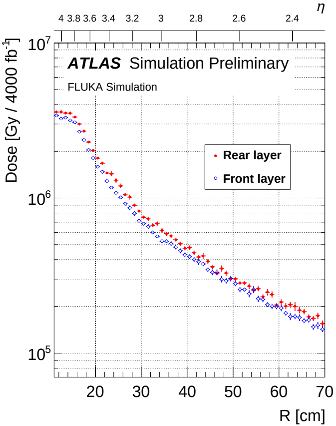
- Strong decrease of σ_t with V_{bias} ($\sigma_t < 30$ps at 235/320 V in non-irrad. sensors)
- Irradiated sensors tested at different temperatures.
- Decrease of σ_t with gain. Studies point to a safe gain of 10-20.

[1] results from J. Lange et al.; similar results in sensors from FBK

Radiation Levels

- Irradiation levels studied using FLUKA simulations
- Additional safety factors: 1.5 uncertainty in sim, 1.5 unc in electronics behaviour
  $\rightarrow$ 1.5 for fluene and 2.25 for dose
- Updated studies show an increase of $\sim$ 30% wrt TP:
  5.1×10^15 n_{eq}/cm^2 and 4.7 MGy

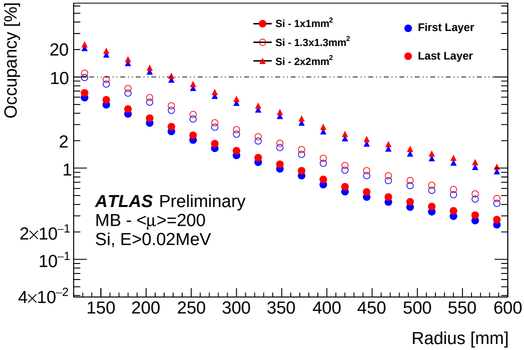




Pixel Size

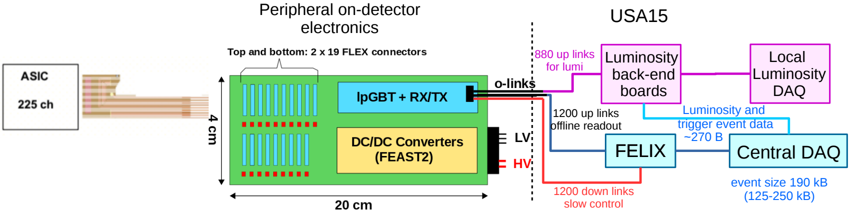
The definition of the size of the pixel is a result of several considerations, mainly:

- The need to keep occupancy low (below 10%)
- A small detector capacitance reduces noise, $C = \epsilon_r \epsilon_0 A/w$



Readout Path

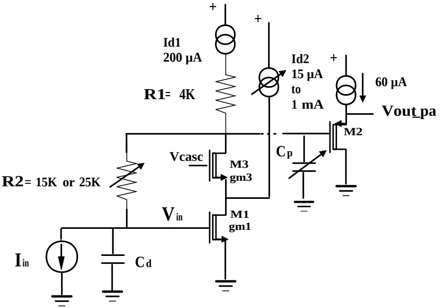
General design of the readout path from the ASIC to USA15:

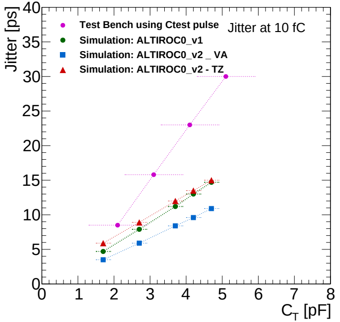


One of the main challenges: design of on-detector board. More realistic designs already available, studies on-going:

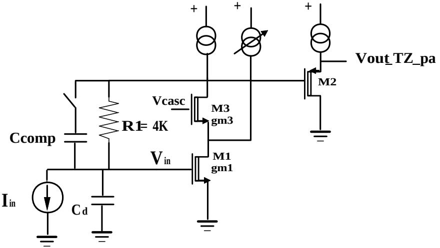
Voltage/Transimpedance preamplifier: schematics

Voltage Preamplifier



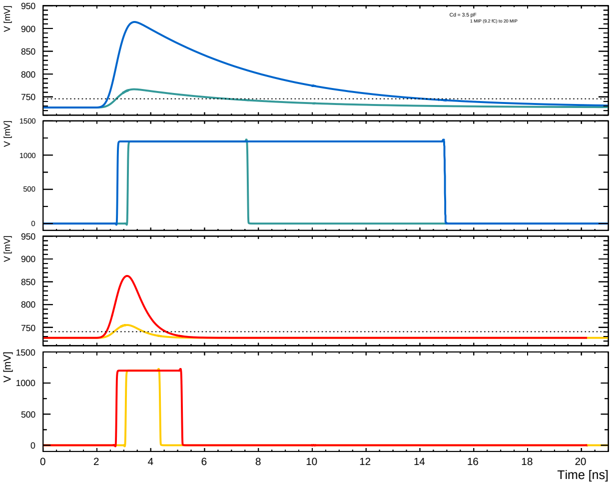


Transimpedance Preamplifier



- Difference btw measurement and simulated jitter attributed to different noise
- Lower jitter in v2
- Jitter in TZ larger than in VPA

Voltage/Transimpedance preamplifier: pulse simulation

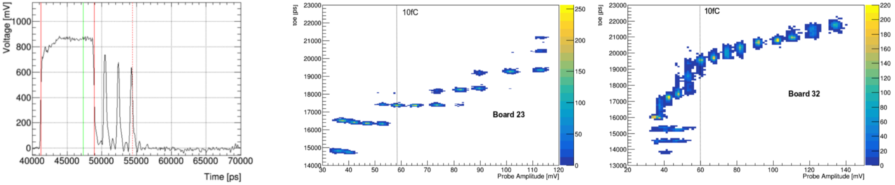


- TZ preamplifier gives a faster, lower amplitude pulse than VPA.

TOT measurement issues

In ALTIROC0, it was not possible to achieve a good measurement of the TOE when the ASIC is bump-bonded to an LGAD (and thus it is not possible to make a TW correction using the TOT):

- TOE scales discretely with probe amplitude
- Re-triggering effect obserbed
- Suspected causes: coupling between discriminator output and preamplifier input
- Improvement: new ALTIROC0 PCB, with larger HV pad for wire bonding. Expected further improvement in ALTIROC1.



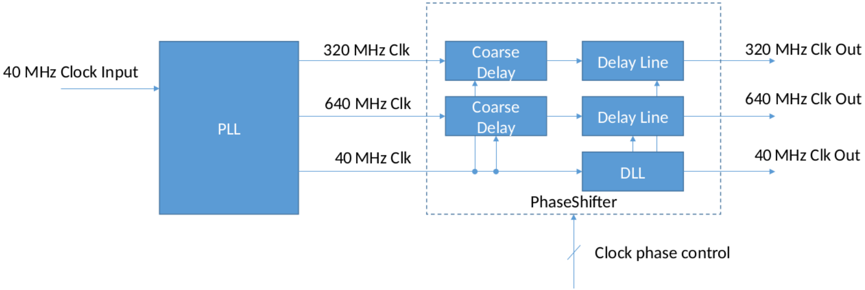
Off-pixel electronics - Phase shifter

The inner clocks of the ASIC have to be in phase, with an accuracy $\sim$ 100ps, in order to:

- ensure the correct time conversion of the TDC
- correctly adjust the time windows necessary to measure the luminosity

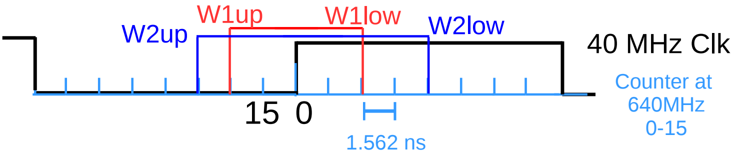
Characteristics:

- Receives clocks at 40, 320 and 640 MHz from the PLL
- Output phase adjusted to a step smaller than 100 ps
- Additional jitter below 5 ps
- Estimated power consumption around 10 mW
- Design is ongoing



Off-pixel electronics - Luminosity

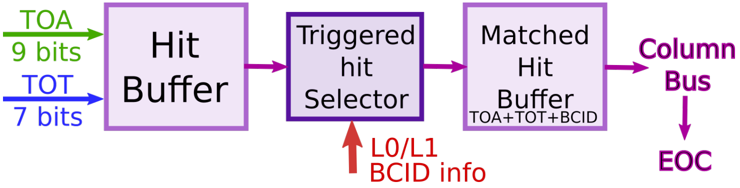
- $\mathcal{L}$ is linearly proportional to N_{hits}
- Non-linearities arise from:
  - double hits $\rightarrow$ low occupancy
  - background noise (*afterglow*)$\rightarrow$ compare N_{hits} in a smaller and wider time window around the BC



- Two time windows, W2>W1
- Rising and falling edges of both windows are tunable
- Transmit the sum of hits per ASIC for each BC
- Only for ASICs at $R > 320$ mm
- The sum over ASICs is computed in 64 regions and saved.

Single pixel memory

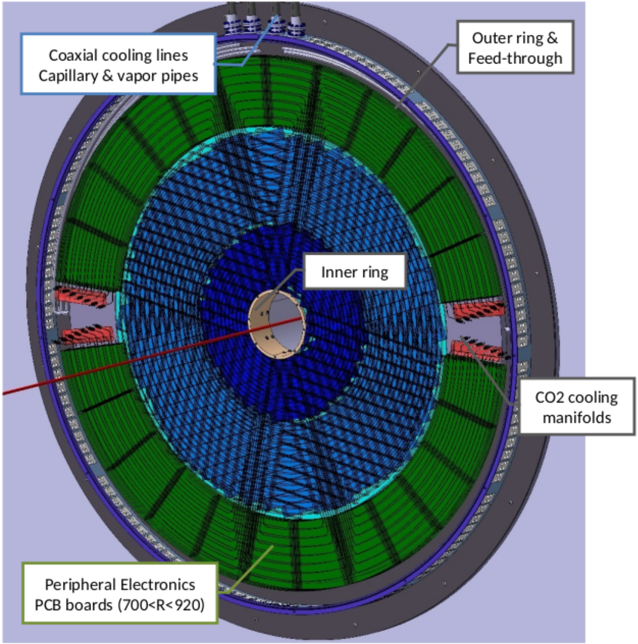
Temporarily store hit data and select hits associated to a trigger.



Baseline design is to use full buffering, storing TOA+TOT/hit flag:

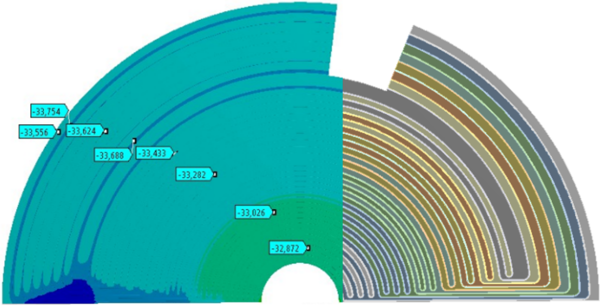
- Handle 10/35μs latency for L0/L1 trigger
- Small space
- Limited power consumption
- SEU
- Alternative design: partial buffering

Services



Coaxial cooling lines
Capillary & vapor pipes
Outer ring &
Feed-through
Inner ring
CO2 cooling
manifolds
Peripheral Electronics
PCB boards (700<R<920)

CO_2 cooling



J. Bonis-A. Fallou

Several challenges:

- LGAD sensors need to be kept at low temperature at all times (-30 ℃)
- CO_2 cooling will be used
- Finite element analysis: temperature distribution of (27 ± 1) ℃
- possible to have the vessel walls > 18 ℃ using heaters