Testing electronic calibration with CCD Reset Gate

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PCWG workshop, October 2018

CCD output stage

- Pixel content is transferred to the capacitive node. The voltage on the node is amplified through one (ITL) or 2 (E2V) transistors to reach the OS output of the channel.
- When the RG clock is high, the capacitive node is forced to the RD voltage instead.
- When RG is released, there is a downward jump in the output voltage, and it stabilizes at the 'post-reset level'
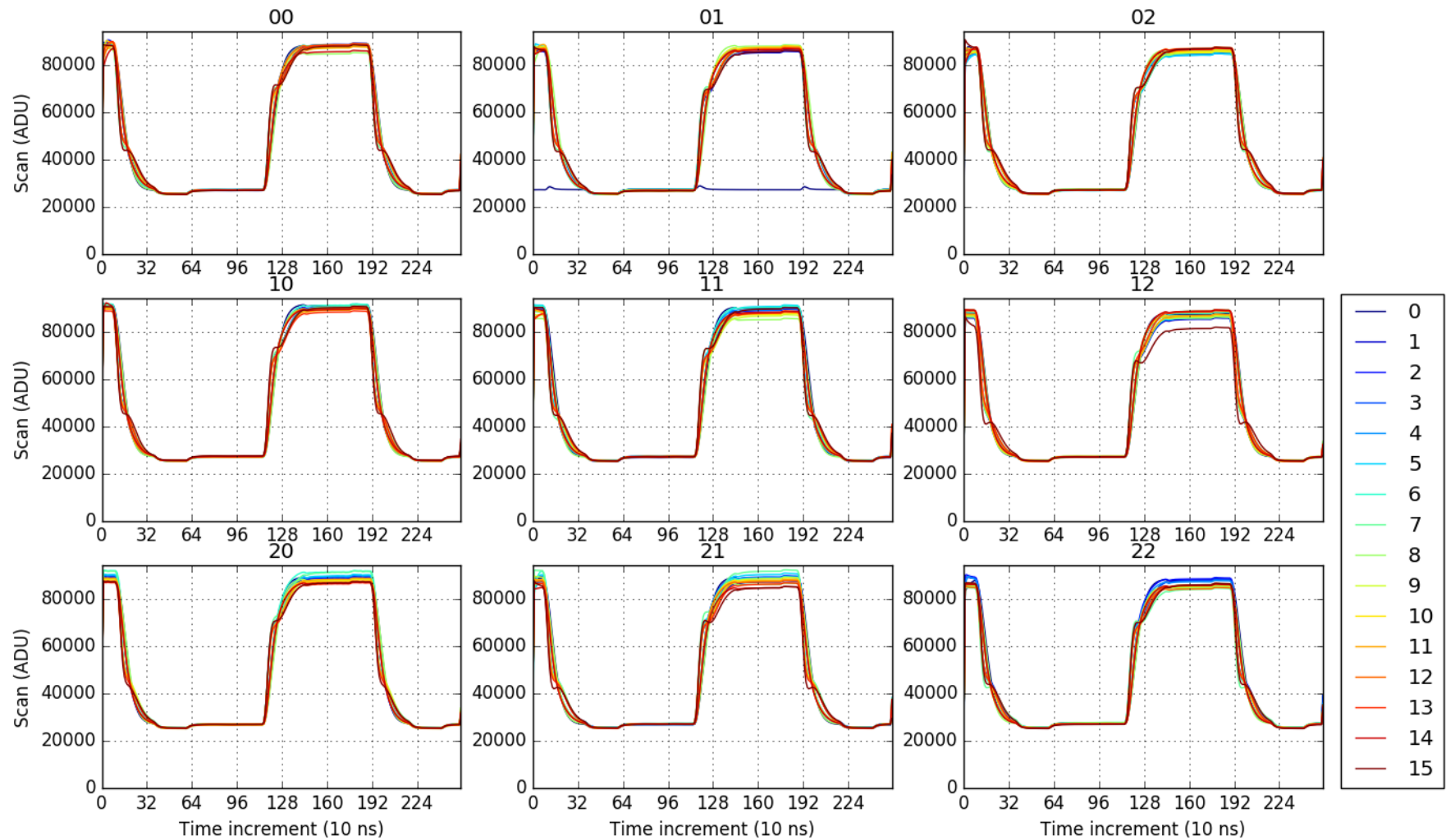
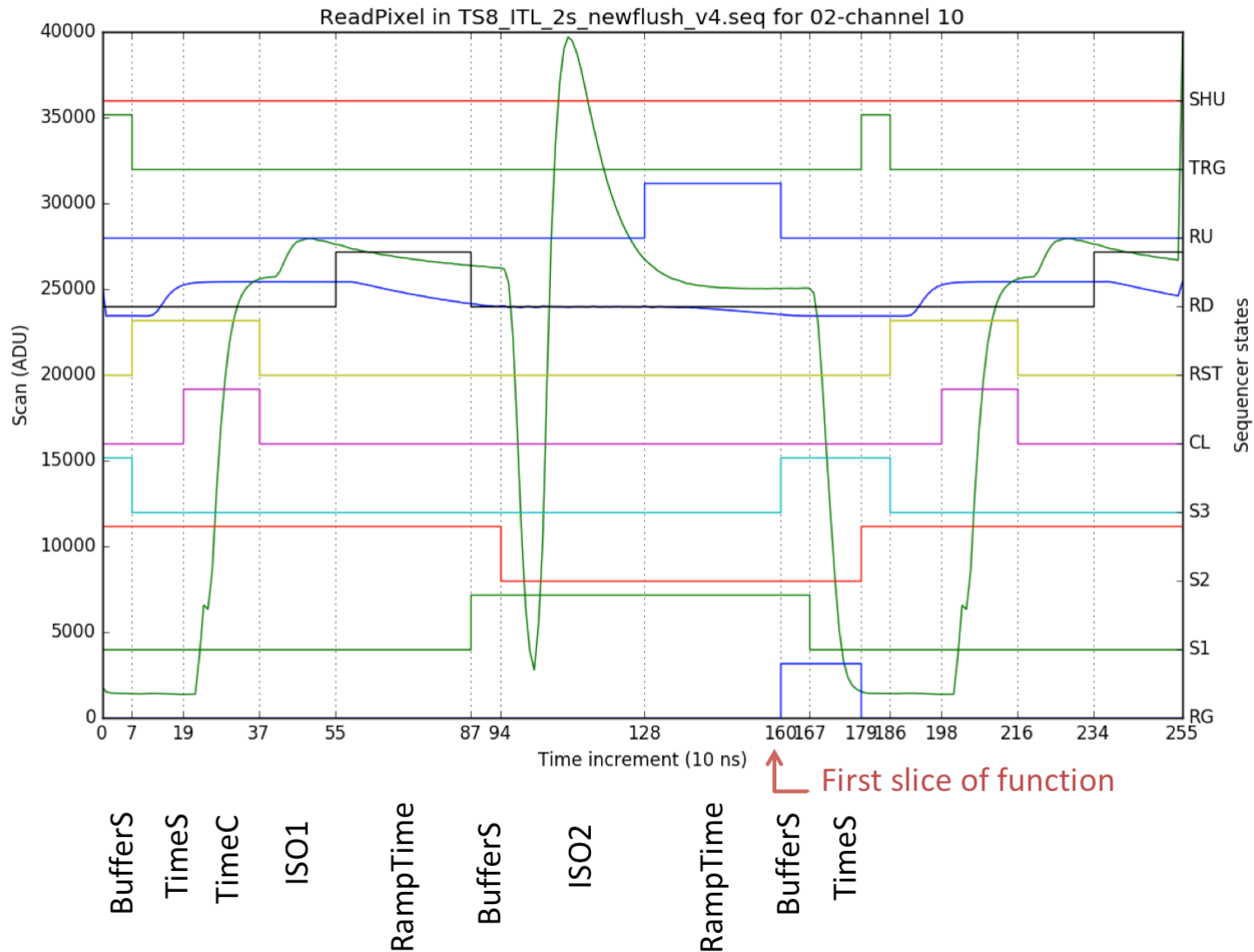# E2V readout sequence

3

E2V signal with RG

ReadPixel in seq-e2v-injectRD.seq for 01-channel 04
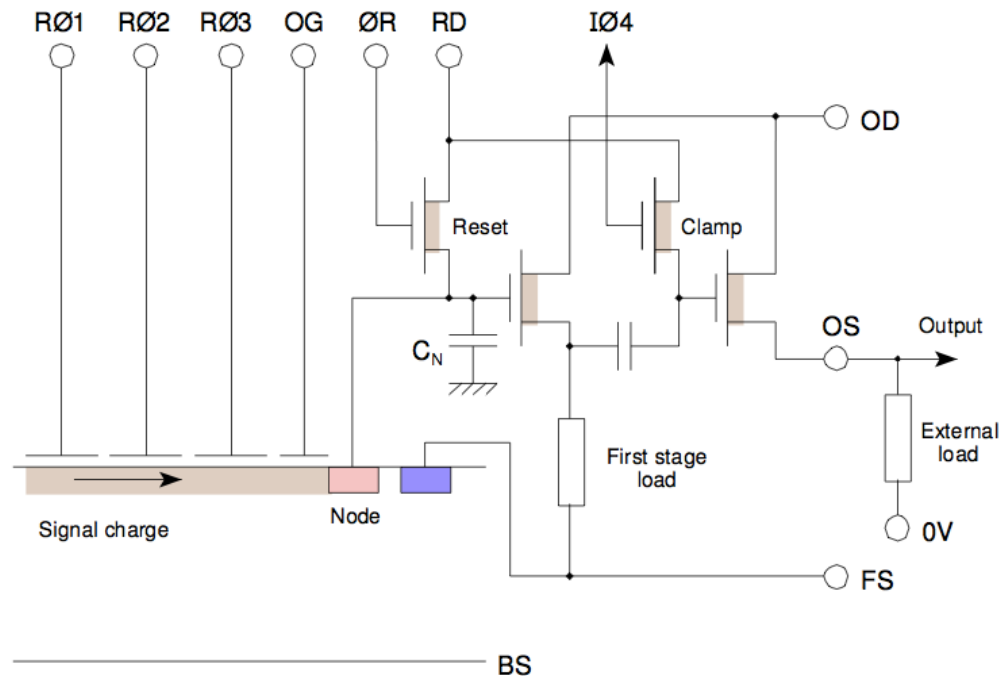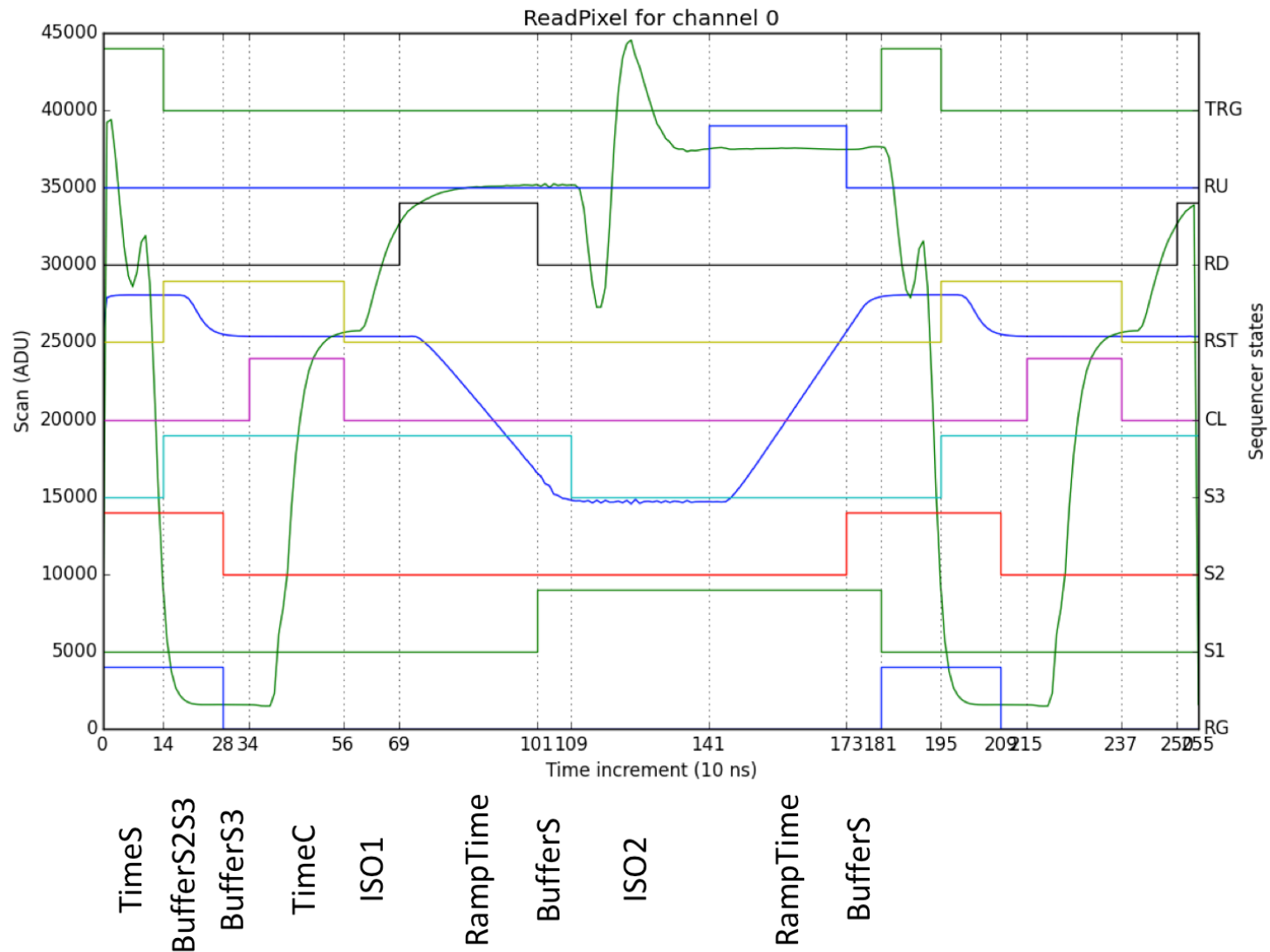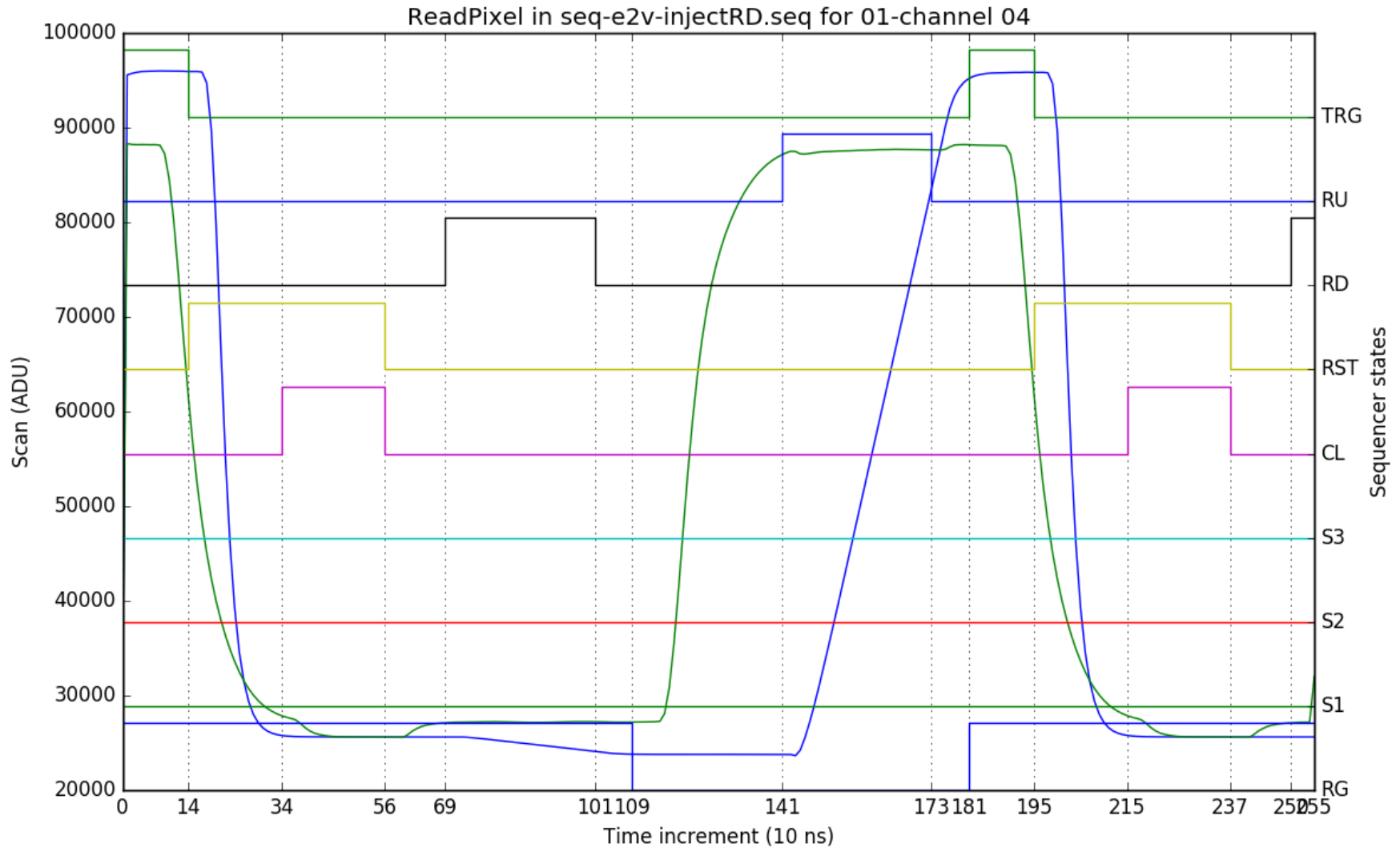
E2V signal with RG

RTM9 with RG injection

ReadPixel in TS8_ITL_2s_newflush_v4.seq for 02-channel 10

First slice of function
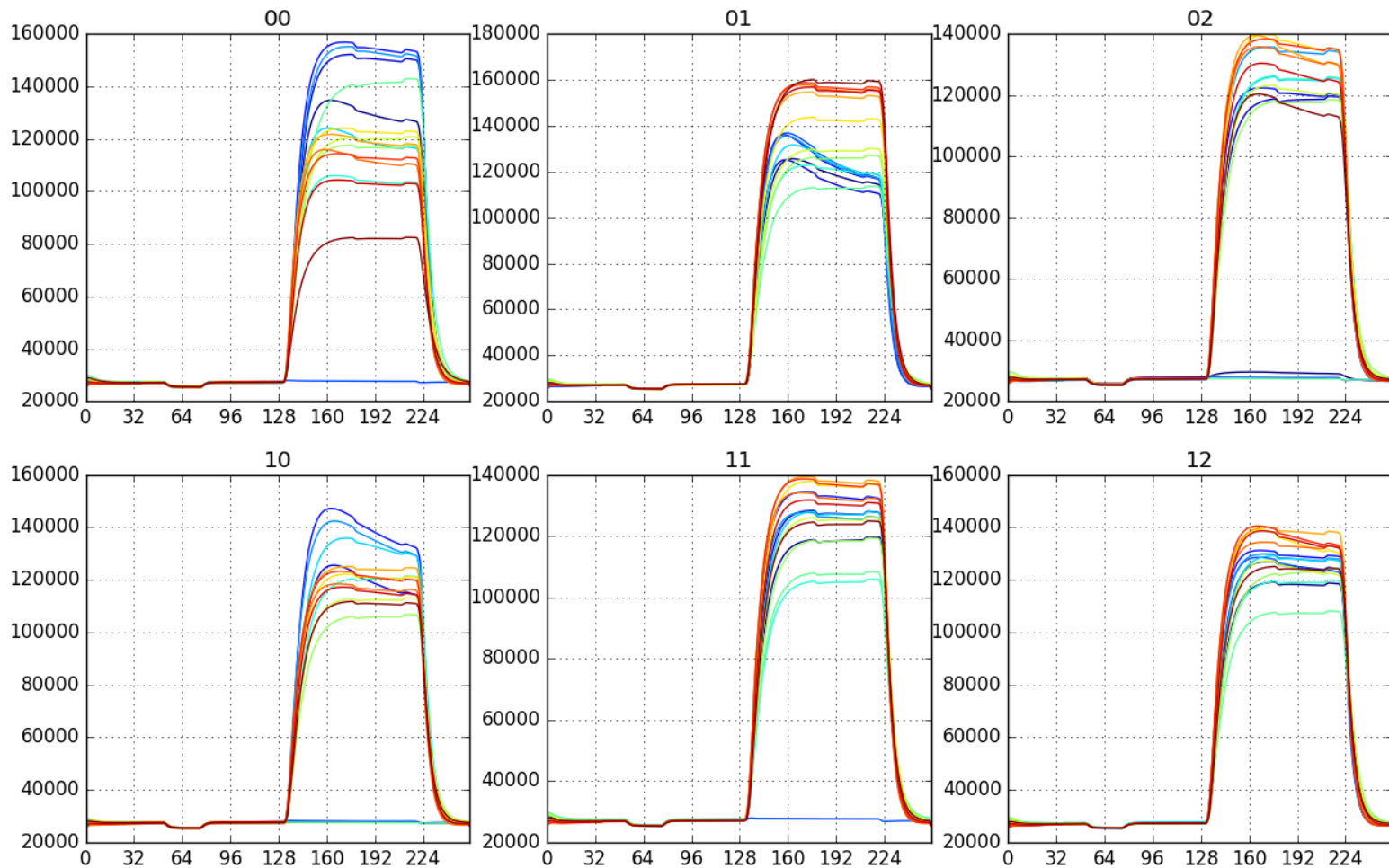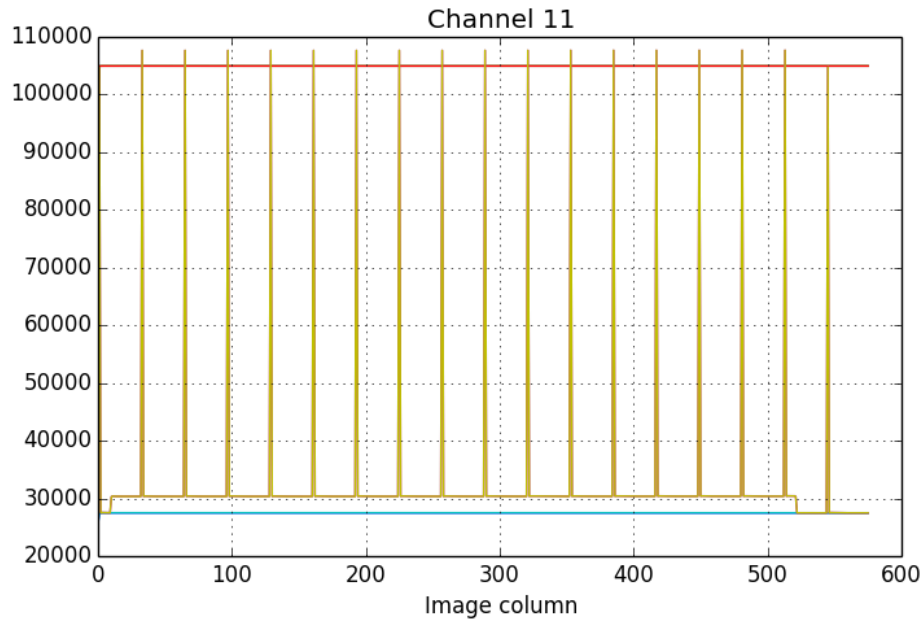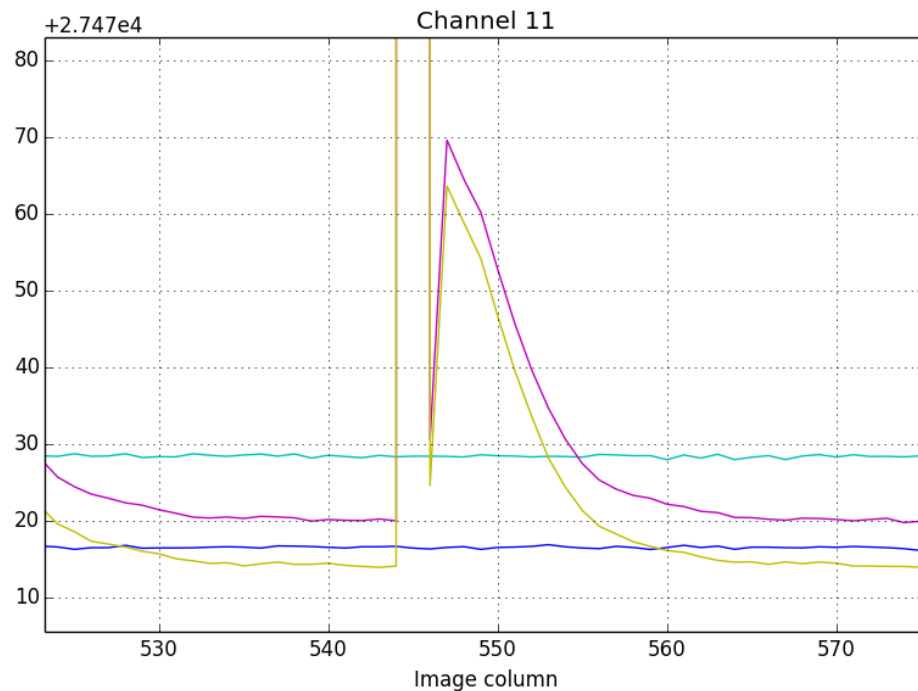
ITL signal with RG

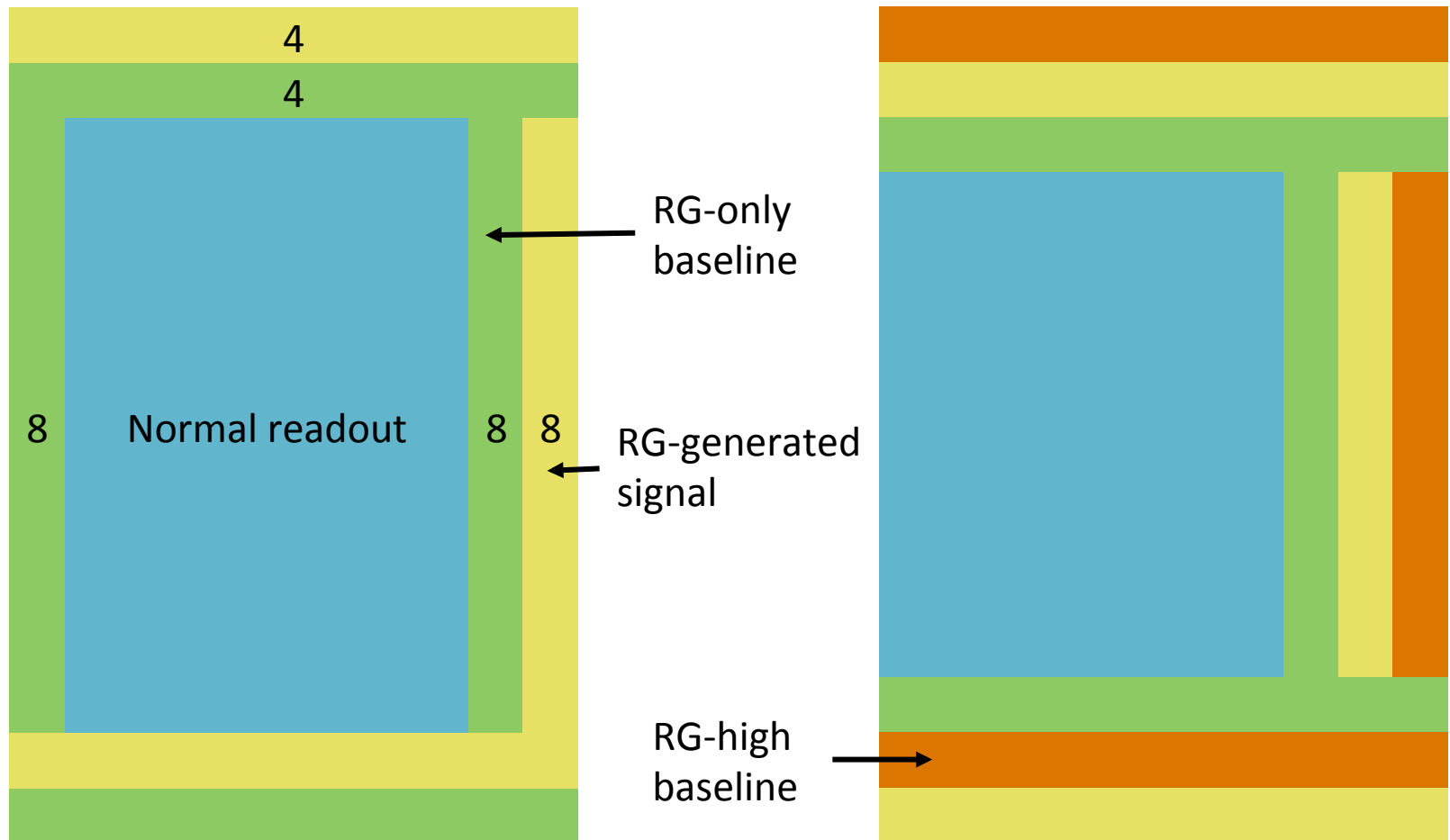- Scans taken on ETU2

Using RG-generated signal

- Trying to make fake stars
- Settling due to the shift of the DC-restore level

Frames with built-in calibration

- Adding calibration rows and columns + baseline

4
4
8   Normal readout   8   8

RG-only baseline

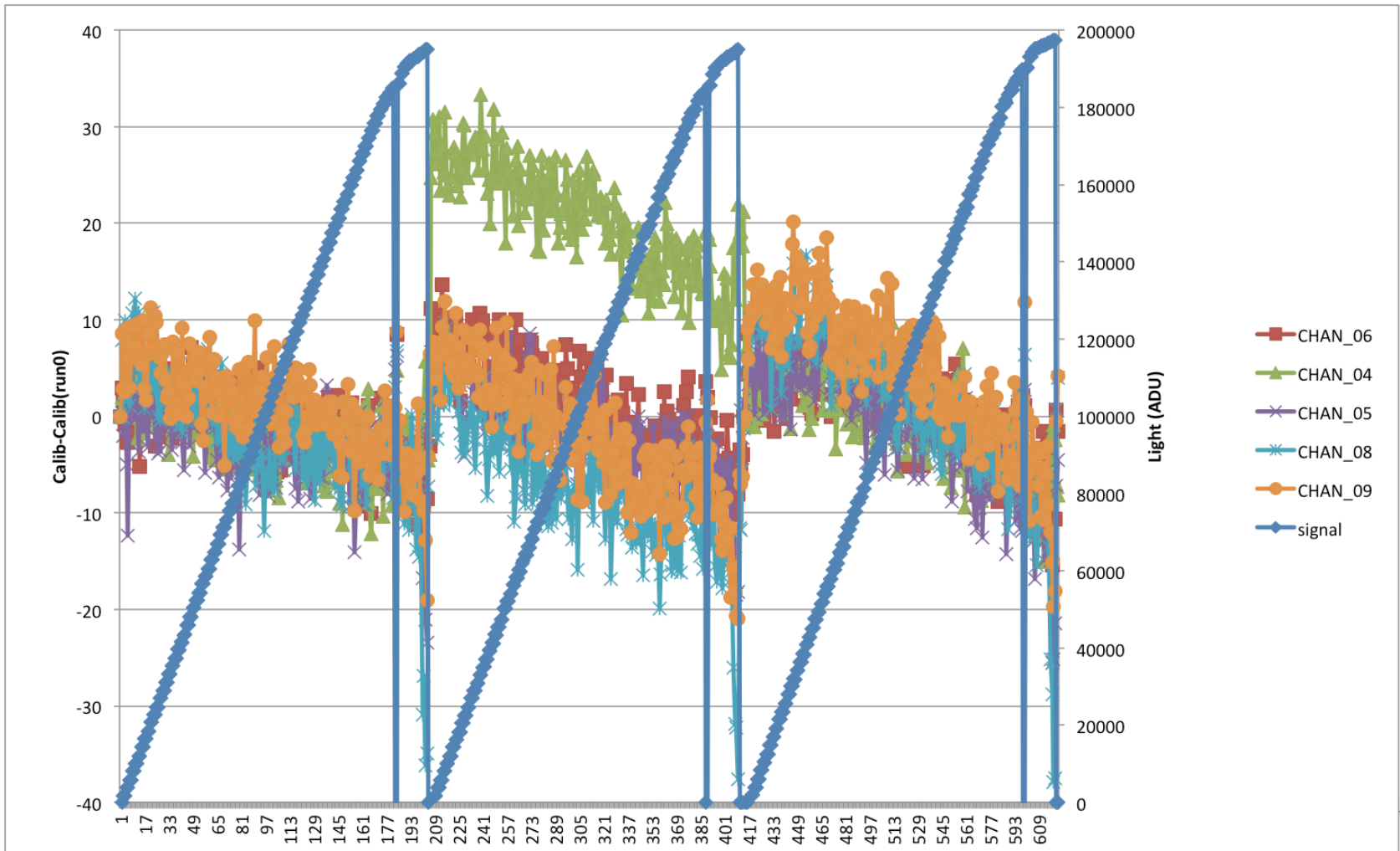RG-generated signal

RG-high baseline

Structure of calibration areas

- Settling issue when shifting to RG-generated signal (symmetrical to issue when shifting back to normal level)

- 8 pixels is too short for settling the calibration injection value

- Transient noise injection, otherwise noise ~ 40 e- (CCD kTC reset noise)

Rows before frame   Columns at end of rows

10
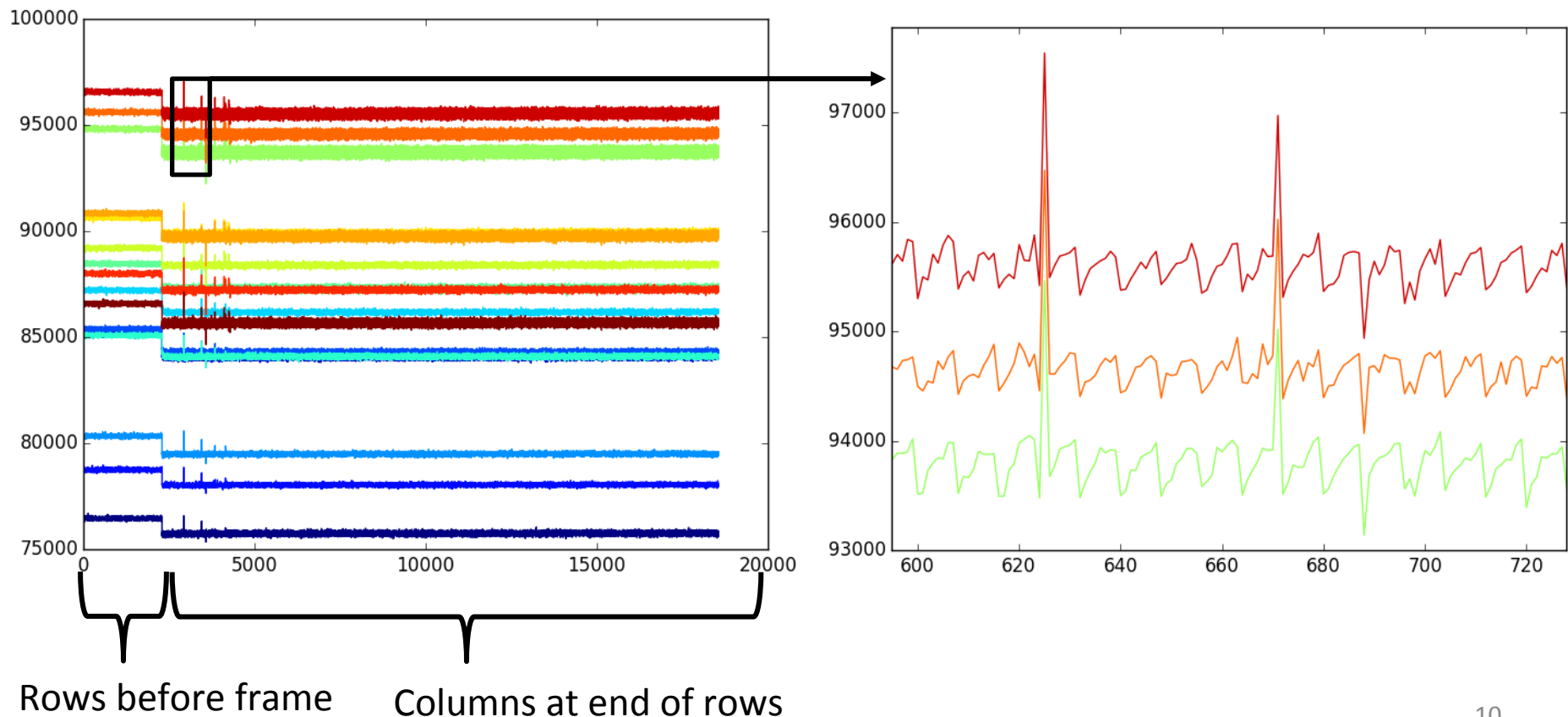
Using RG-generated signal

- Rows post-frame (less contamination, no settling issue),
- Three PTC runs with change of gain for third run

Using RG-generated signal

- Rows post-frame (less contamination, no settling issue)
- Slope ~ 10^-4 over PTC run