# **Slow control**

- Should be OK both in FEV11 and 13.
- Confirmed by vth0
  - Change trigger threshold
  - See the change in the vth0 (trigger threshold)
- All studies in CC mode

## The problem on Raz\_chn

- Raz\_chn is found to be inverted
- Found a FPGA code that it is artificially inverted due to probably mis-routing of SMBv4
- Fixed for SMBv5 (re-inverted)

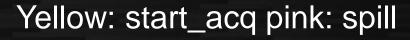
• This enables FEV13 to get some data

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### **Problem on start\_acq**

- Start\_acq only comes > 3.4 sec later than the previous start\_acq
- Regardless of frequency (confirmed in 2/5/10 Hz)
- HDMI input OK (see pulse every 200 msec)
- Reason unknown







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## **Comments on signals**

- SPILL go down → start acq going up
- Start acq going down to end\_readout1: ~150 ms
- Start\_convb: 14 μs after start\_acq going down
- Start\_readout1: 700 μs after start\_acq down

# Data collapse

#### Data at end of each spill collapsed.

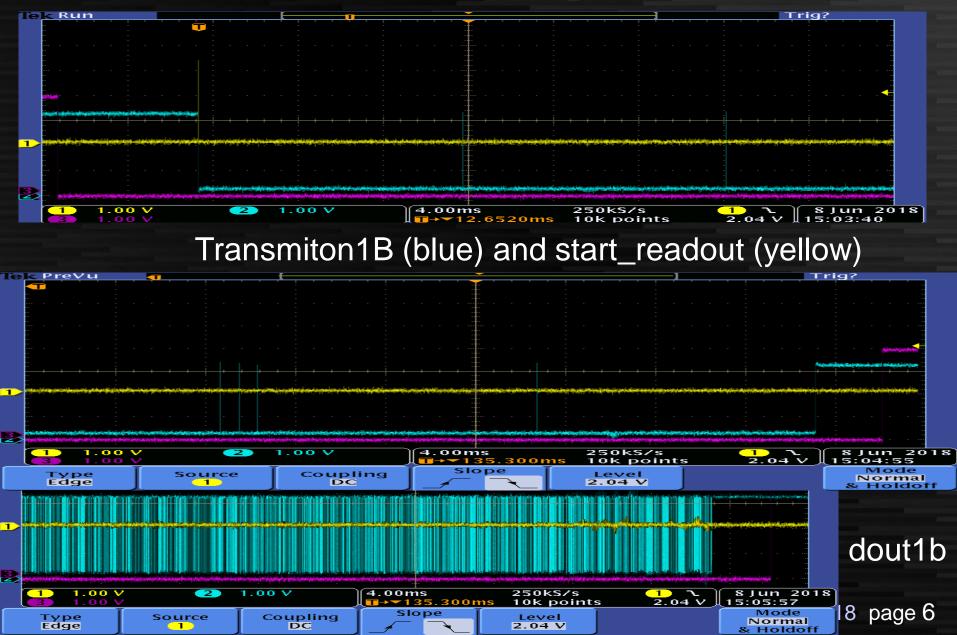
											root@l
0					編集(E	) 表示	示(V)	検索(	5) 歸	(末(T)	ヘルプ(ト
	13			1374	13a6	1384	13a5	1385	1393		
110100	13			013f	0135	0137	0137	0138	0139		
128.10	13			0136	0141	0136	013c		013c		0132
	13			0142	0135	0137	0137	0138	013e	CONTRACTOR OF STREET	
0	13	43	00	0140	0135	0139	0138	0136	013c		0138
0	13	43	20	0134	013b	0134	0138	0143	013e		0135
c 0	13	43	40	0138	013b	0136	0135	0134	0134	0135	0135
	13	43	60	0142	0135	0131	0138	0138	0137		013e
PA	13	44	00	1176	1180	117b	1184	1181	1185	0143	117e
20	13	44	20	077d	074b	0719	06e7	06b5	0683	116d	07af
50	13	44	40	05ed	05bb	0589	0557	0525	0085 04f3	0651	061f
50	13 13 13 13 13 13 13 13 13	11	60	fffc	0000	e5af	5053	4 c 4 9		ffff	0009
50	17	15	aa	e5af	0000	0000	0000	2020	2020	ffff	0000
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2010/10/1	13			2020	a20d	0000	0000	0000	0000	0000	0000
70	13	464	40	ffff	0000	e5af	0000	0000	0000	2020	7c12
60	13 13 13 13 13 13	46	60	0000	0000	0000	0000	0000	0000	fffc	0000
20	13	470	00	e5b0	5053	4c49	2020	fffd	<b>ff</b> 01	4843	5049
20	13	472	20	2020	012C	0129	012e	0126	0130	0126	012b
20	13	47	40	011c	0120	012b	011f	0128	0124		012e
20	13	476	60	0120	0129	0132	0129	012a	012C		0124
50	13	500	30	0125	0125	012C	0125	012a	0126		012C
50	12	101			0107	berg	0177	0129	0124	0123	0120

Section	subsection	field	hex	ascii
SPILL header		Marker	0xFFFC	
		<acqid> msb</acqid>		
		<acqid> lsb</acqid>		
		Ascii tag	0x5053	"SP"
		Ascii tag	0x4C49	"IL"
		Blank space	0x2020	
	CHIP header	Marker	0xFFFD	
		<id></id>	OxFF	
		Ascii tag	0x4843	"CH"
		Ascii tag	0x5049	"IP"
		Blank space	0x2020	
		Raw DATA	binary	
	CHIP trailer	Marker	OxFFFE	
		<id></id>	OxFF	
		Blank space	0x2020	
		Blank space	0x2020	
SPILL trailer		Marker	OxFFFF	
		<acqid> msb</acqid>		
		<acqid> lsb</acqid>		
		<nb chip=""></nb>	0x00	
		<acqid> msb</acqid>		
		<acqid> lsb</acqid>		
		Blank space	0x2020	

SPILL header instead of SPILL trailer found

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# **Data Collapse**



# Plan

- Finalize to investigate issues by next Tuesday
- Gluing at Wed-Fri next week
- Test and bias board on the week of 18<sup>th</sup>
- Test @ LLR on the week of 25<sup>th</sup>
- Move to DESY