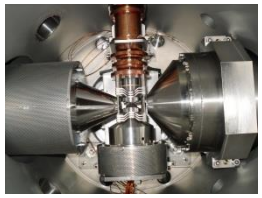
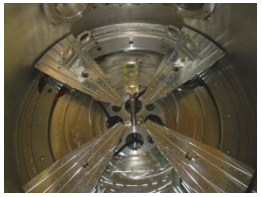
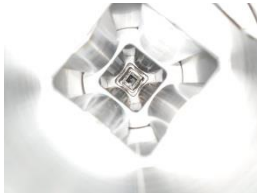



laboratoire de physique corpusculaire

FASTER

DAQ Network May 16th 2018

Clermont-Ferrant

Carniol Benjamin, **Chaventré** Thiérry, **Cussol** Daniel, **Etasse** David, **Fontbonne** Cathy, **Fontbonne** Jean-Marc, **Harang** Julien, **Hommet** Jean, **Langlois** Jérome, **Poincheval** Jérome

ENSICAEN École Nationale Supérieure d'Ingénieurs de Caen

Normandie Université

AGENDA

FASTER-V2

1. FASTER OVERVIEW
2. FASTER REAL TIME ALGORITHMS
3. FASTER SOFTWARE
4. MASTER BOARD

FASTER-V3

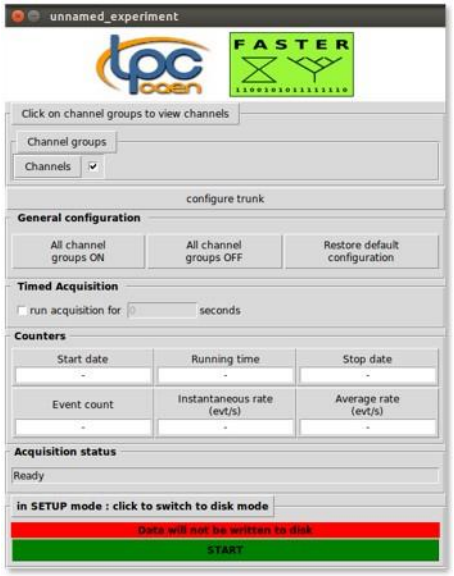
1. MMC (FASTER_V2)
2. CLOCK
3. PROTOCOL
4. PROCESSOR MANY CORES
5. CONCLUSION

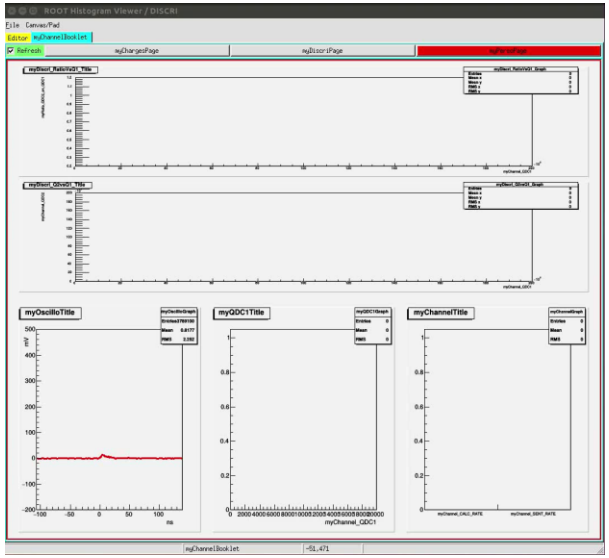
FASTER-V2 OVERVIEW

Offline Analysis

RHB

Real Time Algorithms





Modular Electronic

Ubuntu repository

Based on Root

FASTER-V2 OVERVIEW

STANDALONE SYSTEM

- 1 VITA 57 slot,
- 1 FPGA (C5 140 LE)
- 1 Gb/s Ethernet

MULTI-CHANNEL SYSTEM

- 2 VITA 57 slots,
- AMC.2 full size module,
- 3 FPGA(s) (C5 140 LE)
- 1 and 10 Gb/s Ethernet
- 10 MHz Clock synchronization

FPGA firmware loading by Ethernet

FASTER-V2 OVERVIEW

STANDALONE SYSTEM

MULTI-CHANNEL SYSTEM

- 4 FADC (125MHz@14bits)
- ±1V, ±2V, ±5V, ±10V input range
- 25 MHz Bandwidth

- 2 FADC (500MHz@12bits)
- ±1V input range
- ±1V input adjustable Offset
- 100 MHz Bandwidth

- DDC316 from TI
- 32 channels
- I-TO-V conversion front end
- 3pC to 12 pC (full scale)
- Integration time range from 10us to 10 ms

- ISEG BPS-Serie - 4W
- ± 500 V to ± 6 KV

- FMC project (CERN)
- 5 I/O ports
- 200 MHz Bandwidth
- LVTTL

AGENDA

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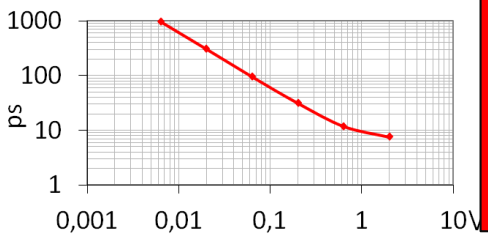
FASTER-V2 REAL TIME ALGORITHMS



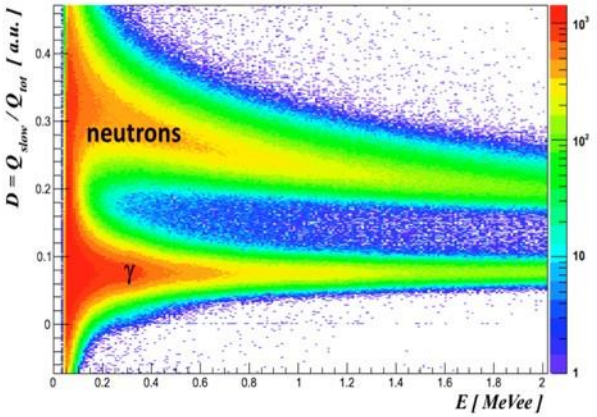
Time resolution VS signal amplitude

FASTER-CRRC4
FASTER-TRAPEZ-TDC

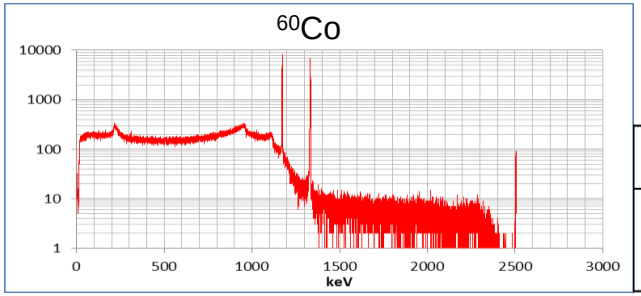
FASTER-QDC-TDC$_{HR}$
FASTER-RF
FASTER-SCALER
FASTER-SAMPLER

FASTER-ELECTROMETER

FASTER_HV



Demon detector, CARAS board,
FASTER-QDC-TDC$_{HR}$



pic keV	FWHM keV
1173,21	1,71
1332,48	1,90
2505,69	2,41

HPGe detector, MOSAHR board, FASTER_ADC

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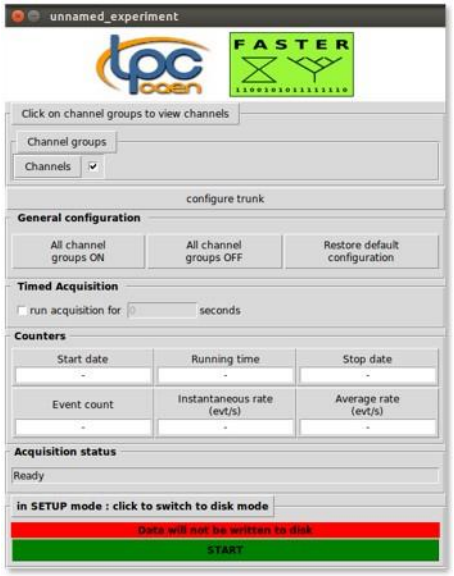
FASTER-V2 SOFTWARE

Offline Analysis



Ubuntu repository

- Ubuntu 16.04 (production)-> 18.04 (Dev) LTS 64 bits
- ADA and Python
- Software trigger (multiplicity or Boolean trigger)
- 5.10^6 measurement/s per computer (~100 MB/s)
- Faster repository on LPC Server
    - sudo apt_get install fasterv2
- Update the software and the FIRMWARE at the same time
- Offline analysis package
- List of available packages
    - fasterv2, fasterac, rhb,
    - faster-rhb-xxx-demo (xxx=qdc, crrc4, trapez, rf, ……)

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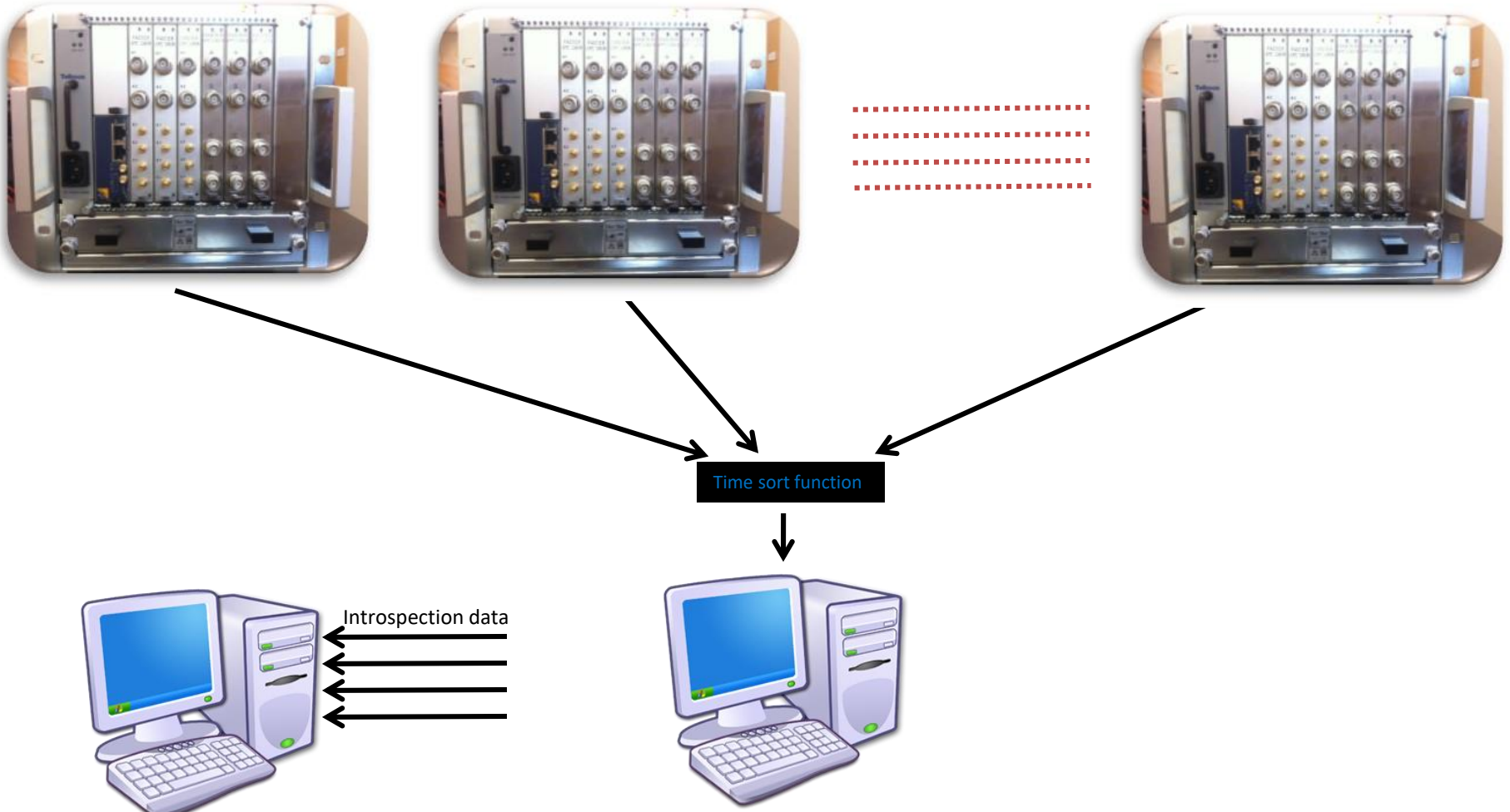
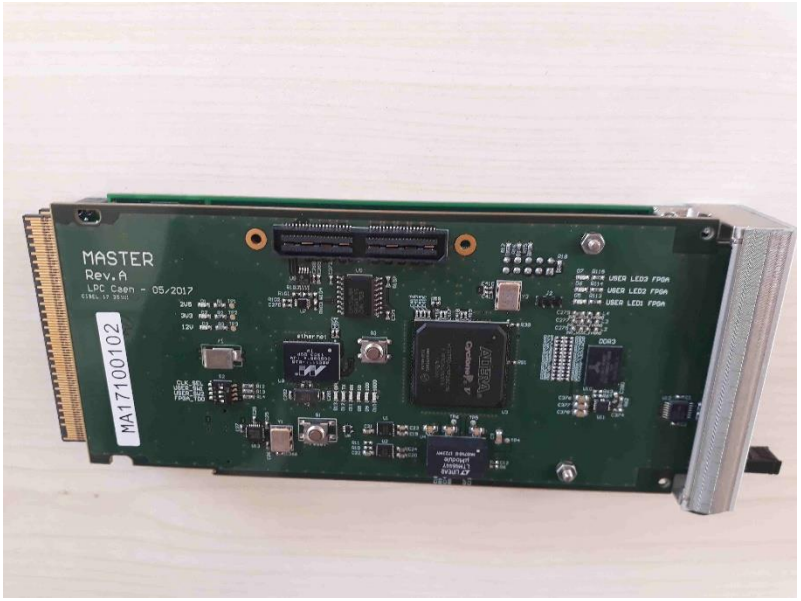
MASTER BOARD



MASTER BOARD



MASTER

- Cyclone 5
- 128 MB DDR3
- 1 Gbe
- 12 unsorted data streaming -> 1 sorted data streaming

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MMC (FASTER-V2)

MMC IN2P3
- Damien TOURRES (LPSC)
- ATMEGA128

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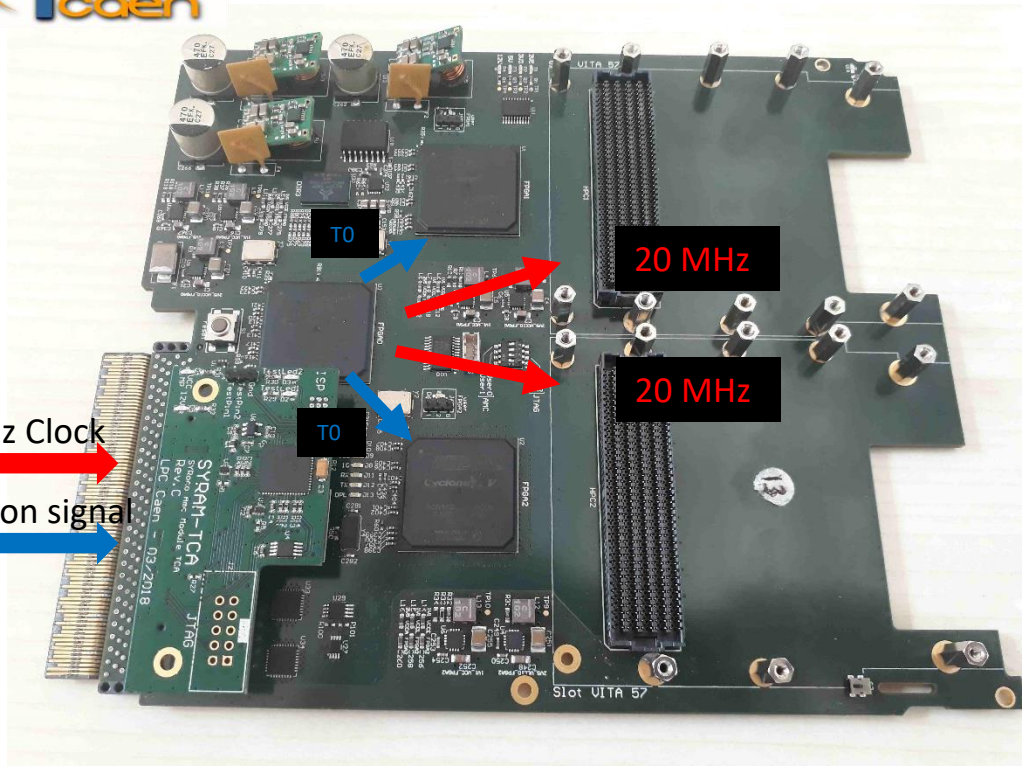
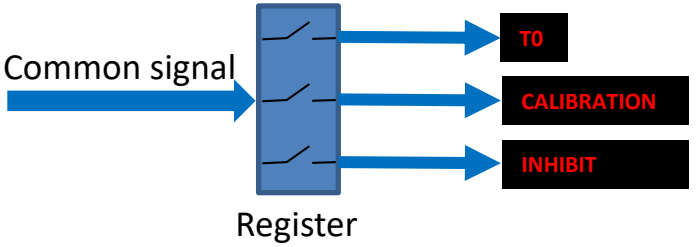
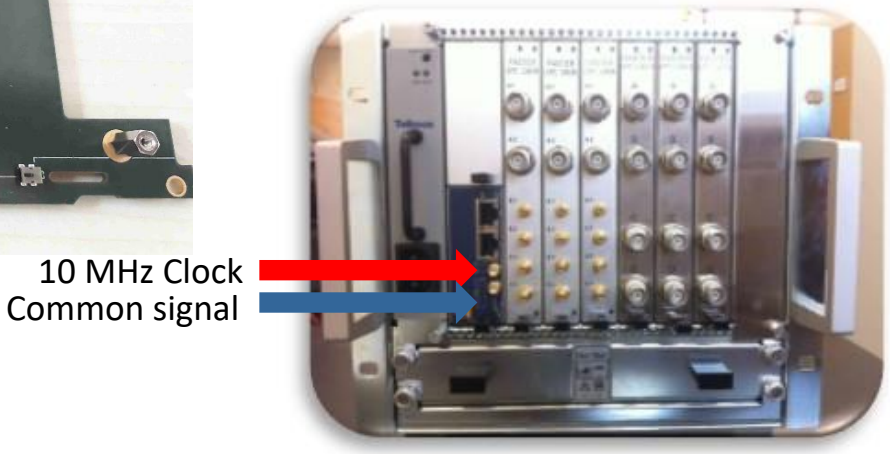
CLOCK







White Rabbit

AGENDA

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PROTOCOL

FASTER-V2

Slow Control -> ETHERNET -> UDP/IP -> FASTER PROTOCOL

DATA -> ETHERNET -> UDP/IP -> FASTER PROTOCOL

FASTER-V3

Slow Control -> ETHERNET -> UDP/IP -> IPBUS PROTOCOL

DATA -> ETHERNET -> ?????

AGENDA

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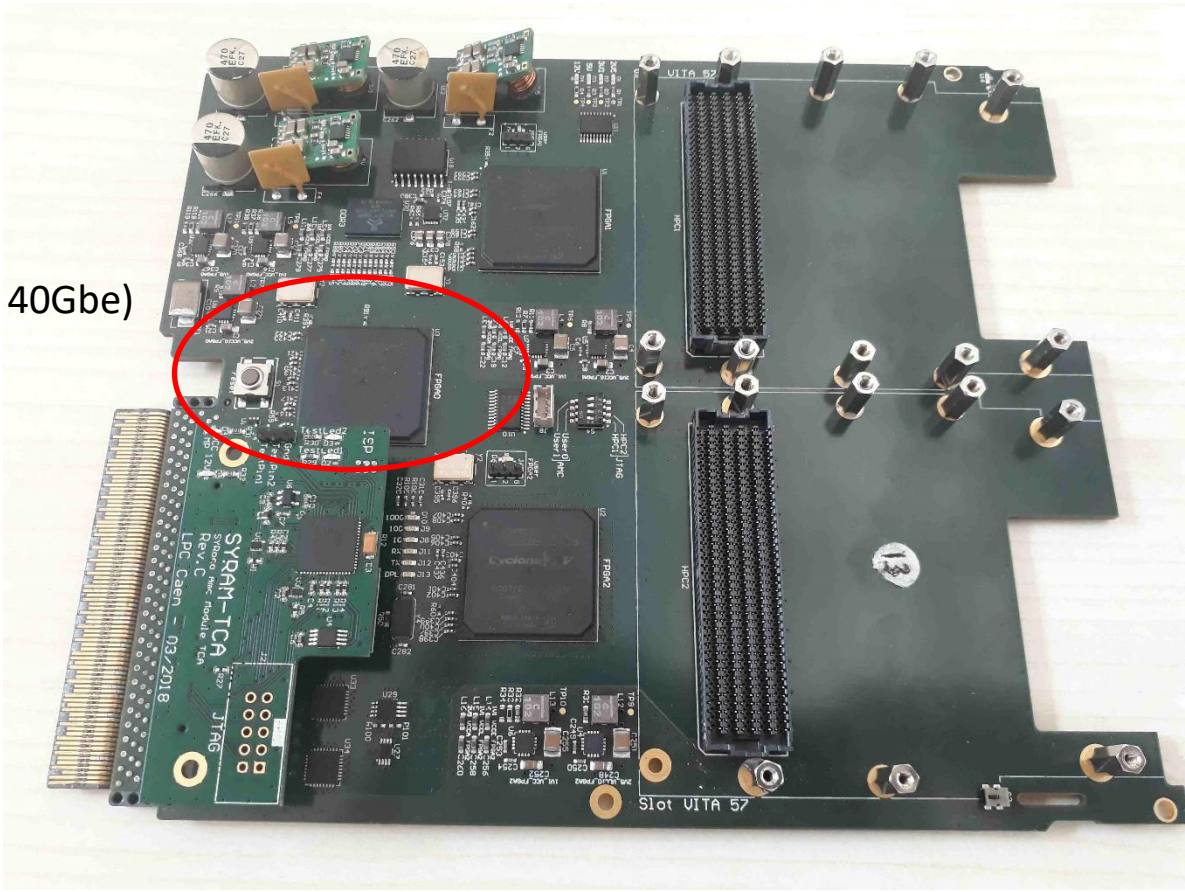
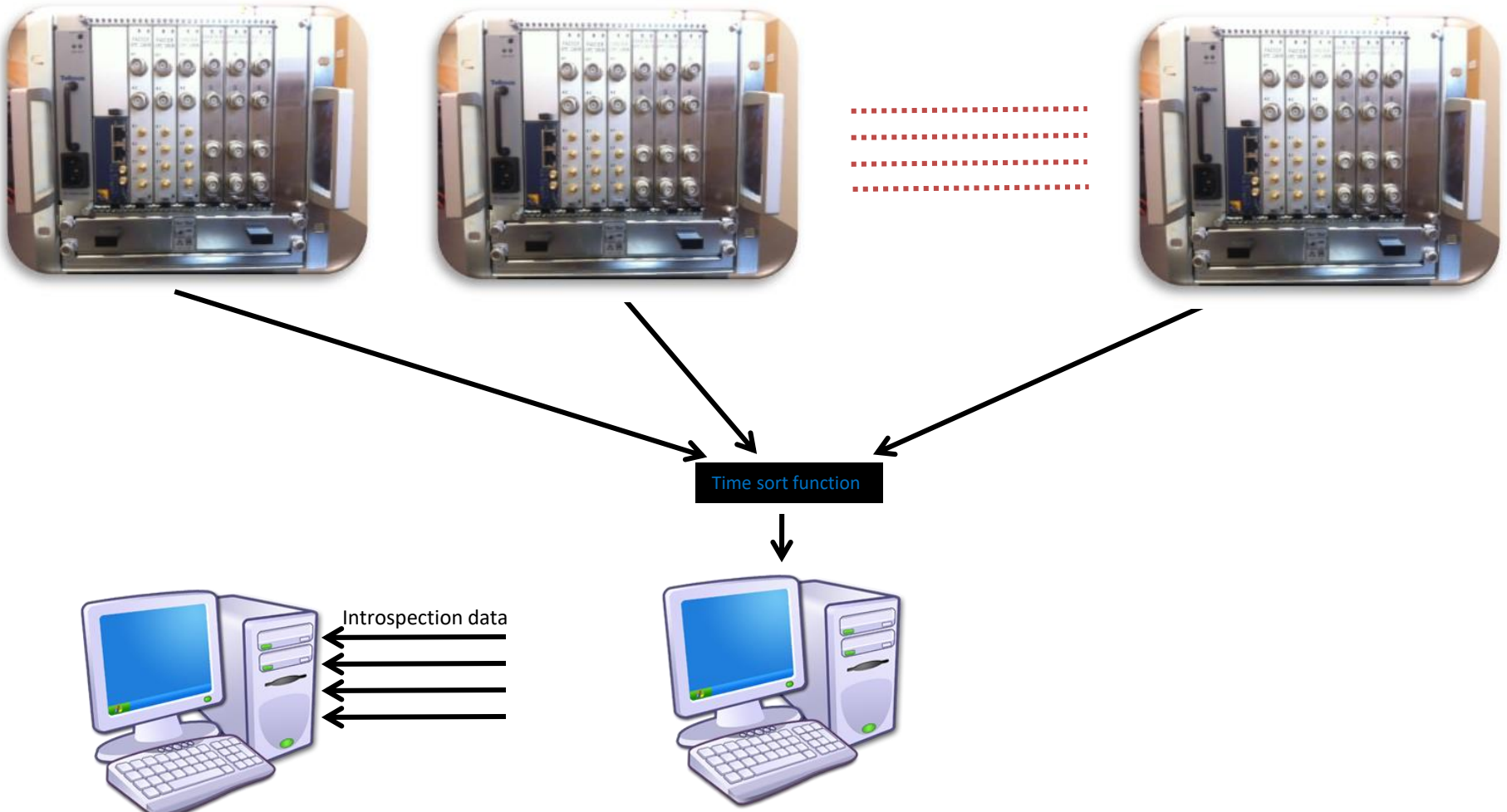
PROCESSOR MANY CORE

KALRAY MPPA COOLIDGE

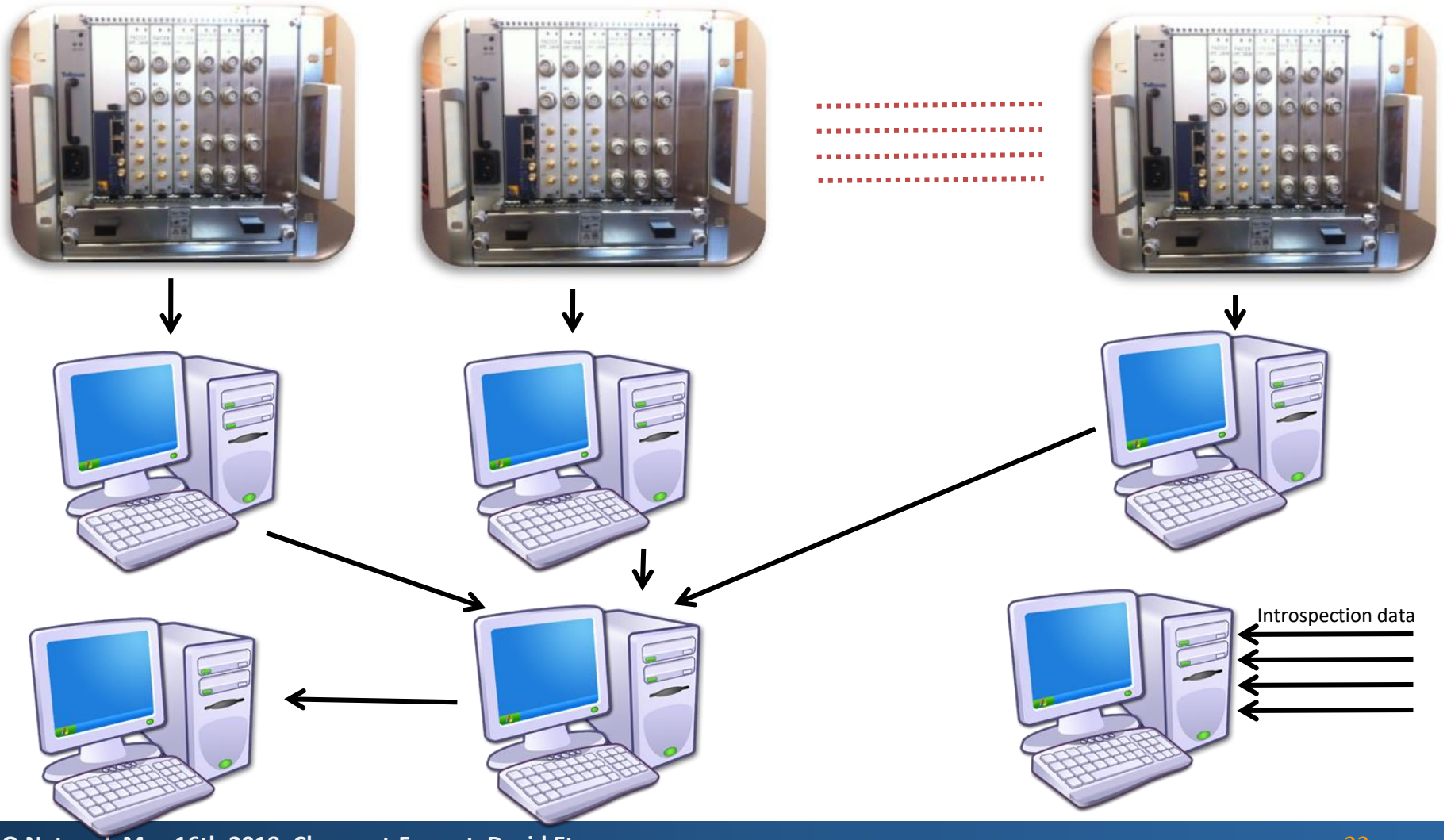
- 600/900/1200 MHz frequency modes
- 5 or 10 Compute Cluster
- 4 MB -> 1 Cluster (20/40 MB)
- 16 CPU cores 64 bits -> 1 Cluster
- 80 or 160 CPU cores
- 3 or 6 TFLOPS
- 2 * 100 Gbe (x->10Gbe, y->1Gbe, w-> 40Gbe)
- 2 * 8 lane PCIe Gen4
- 5 - 15 W / 5-30 W



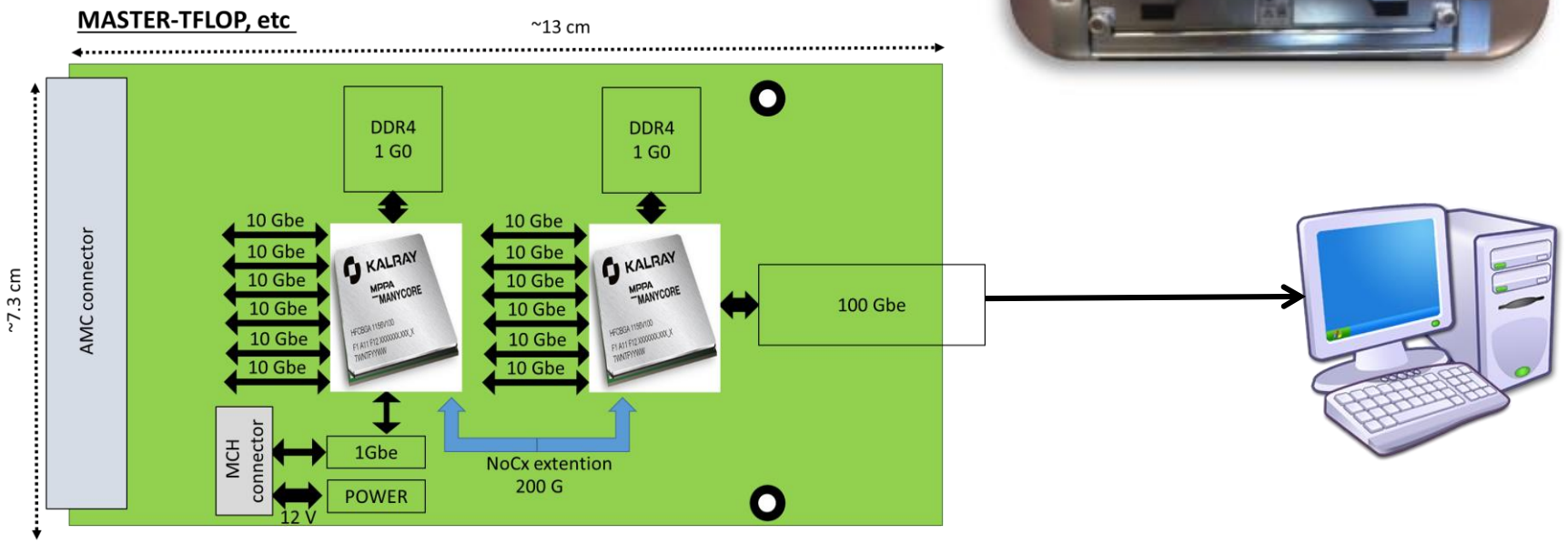
PROCESSOR MANY CORE



PROCESSOR MANY CORE



PROCESSOR MANY CORE



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CONCLUSION

FASTER is a digital modular acquisition system from the electronic front end to the histogram builder software developped at LPC.
FASTER is very easy to install, to use with great performances.
FASTER is able to perform the main nuclear functions with a set of hardware very reduced.
FASTER is wireless ☺.
FASTER is designed to handle medium size experiment (from one to few hundred channels).
FASTER is used in 10 Countries (More 60 FASTER systems has been manufacturing)

FASTER-v3 will be designed to handle large size experiment (from one to few thousand channels).

FASTER-v3 will be able to manage many TFLOPS in a small system.

FASTER-v3 will be compatible with a DAQGEN system