

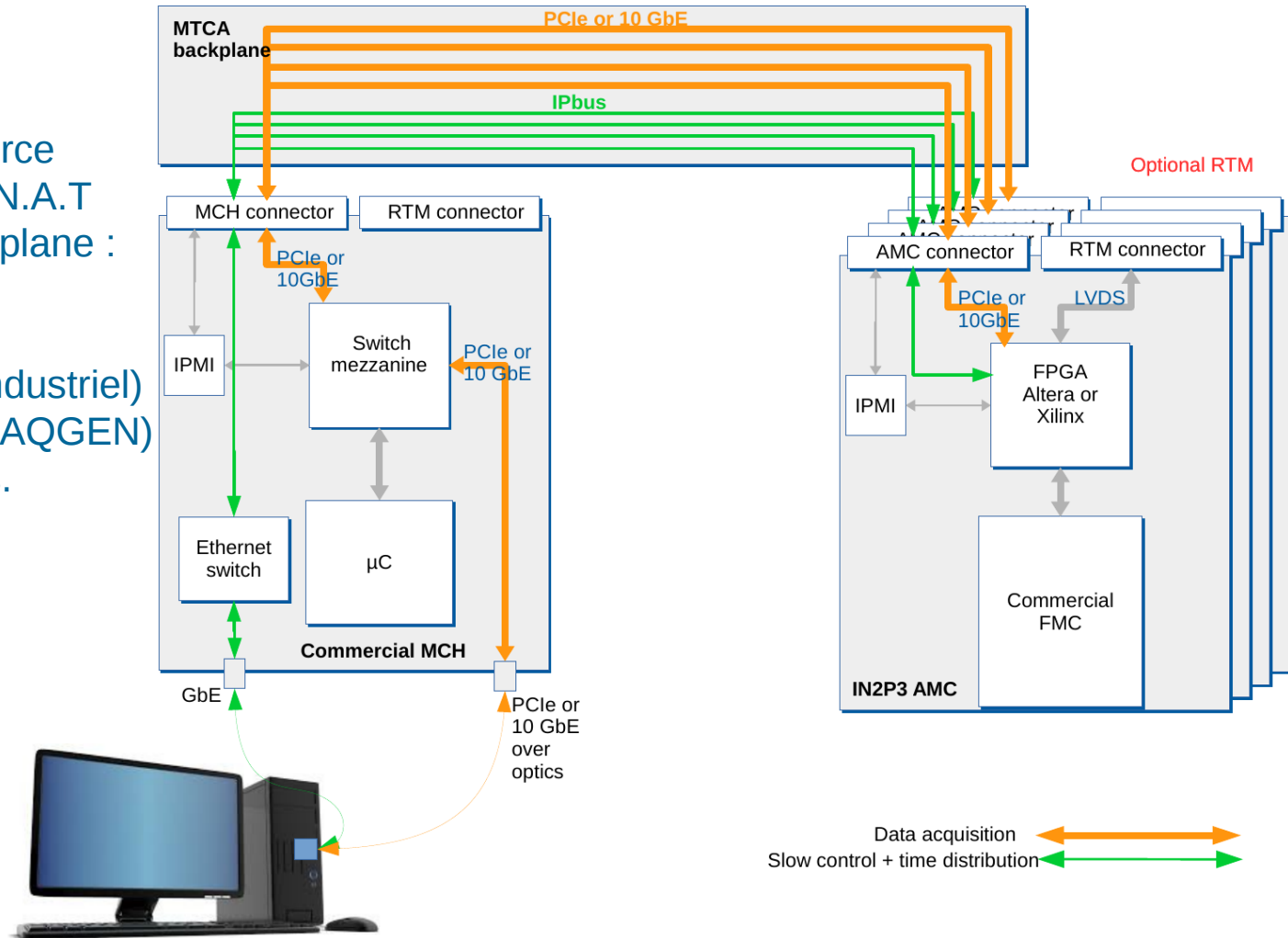
PROJET DAQGEN



- DAQGEN
- NEBULA
- IDROGEN
- White Rabbit

ARCHITECTURE

- Standard : xTCA for Physics
- Basée sur du matériel du commerce
- Contrôleur de châssis : MCH de N.A.T
- Lecture des données par le Backplane : PCIe 4x Gen3 ou Eth10G.
- Transfert des données :
 - Eth10G, PCIe-over cable (industriel)
 - 100GEth (developpement DAQGEN)
- Configuration : 1GEth par IP bus.

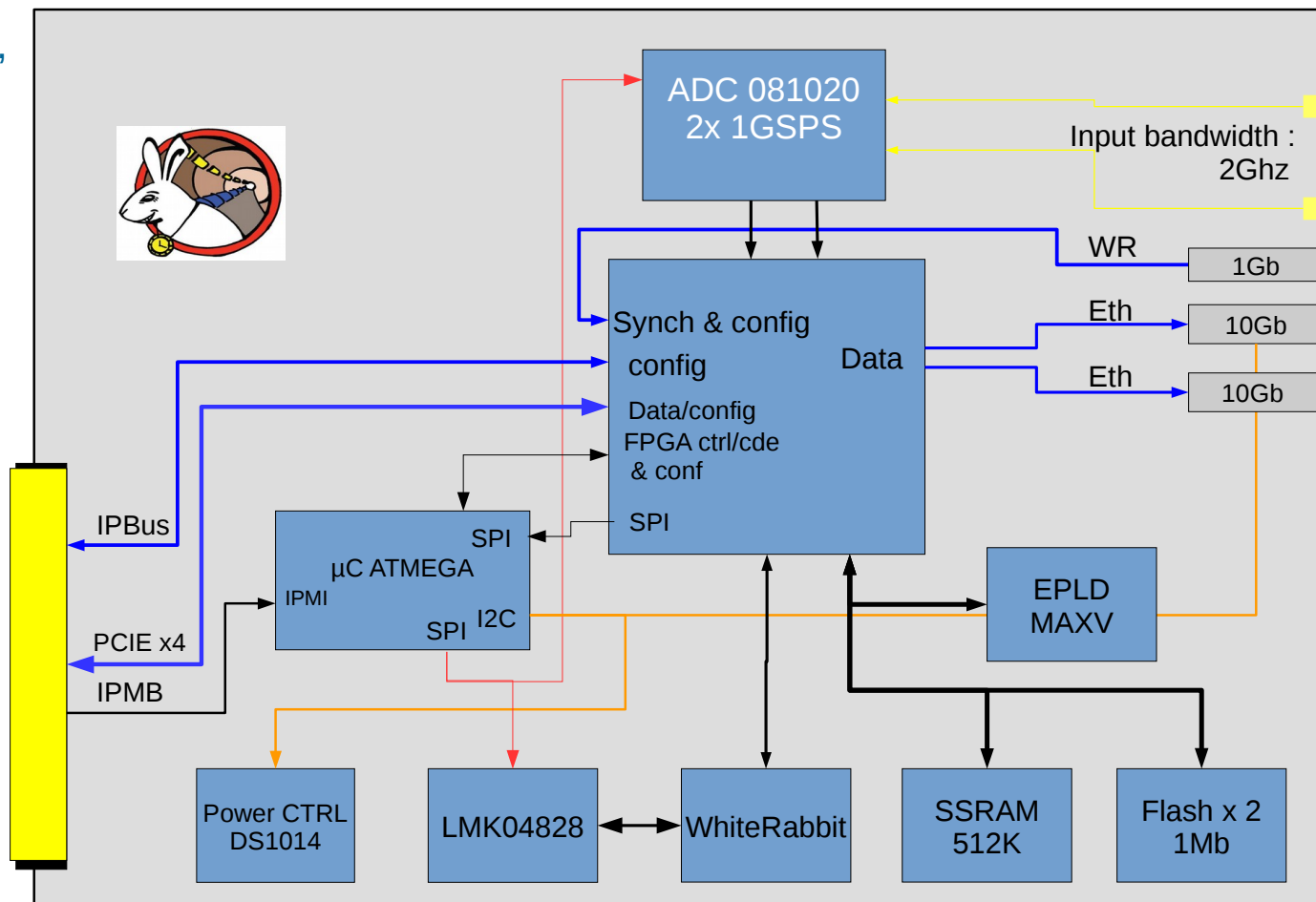




Carte NEBULA

Carte NEBULA

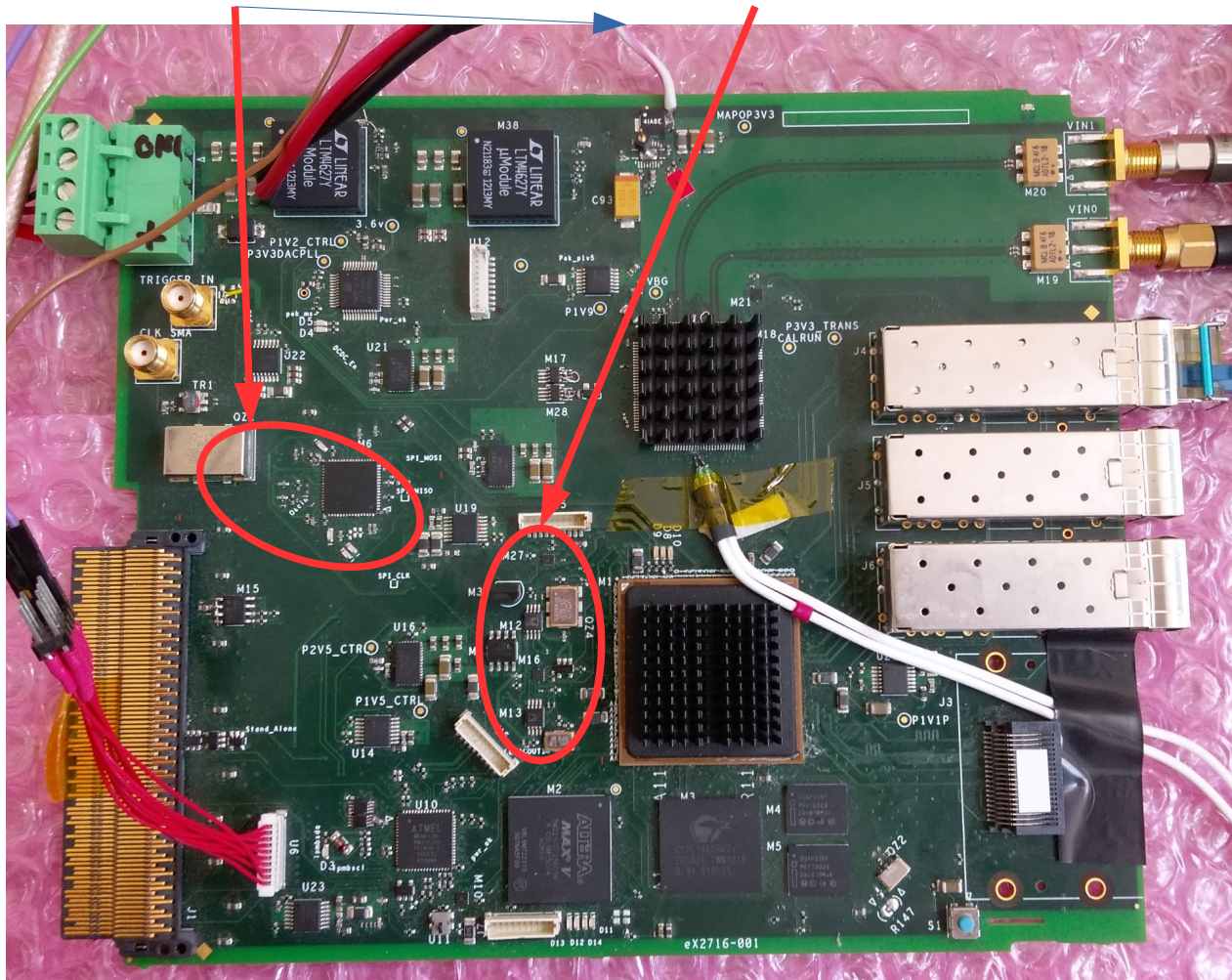
- MTCA 4.0 standard, Double-width, full size AMC.
- FPGA : 5AGTMC7G3F31
- Stand alone mode (power)
- ADC 2 channels 1GSPS.
- White Rabbit compliant.
- On board configuration (μ C)
- Very low noise synthesizer PLL synthesizer cleaner (LM04828)
- Front panel : WR SFP+ 2x SFP+ 10GbEth
- Backplane connectivity : Gbe IP bus, PCI 4x Gen3, IPMB, CLK & trigger lane.



Carte NEBULA

PLL Cleaner

WR components

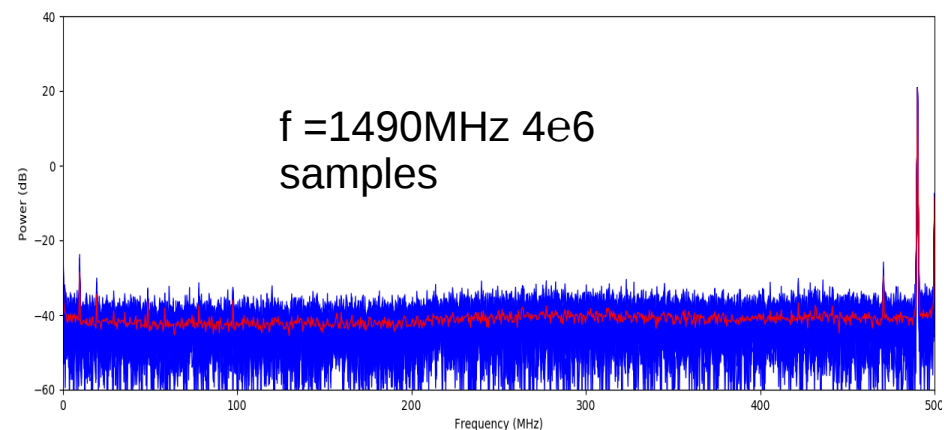
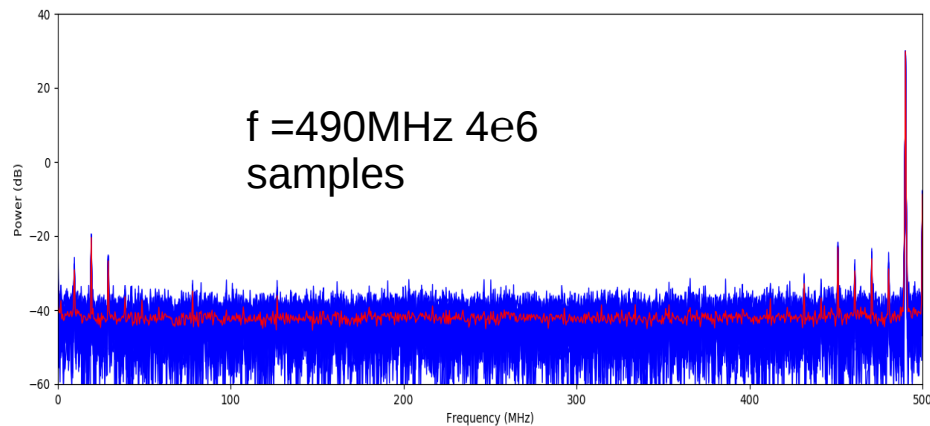




Carte NEBULA, Test ADC

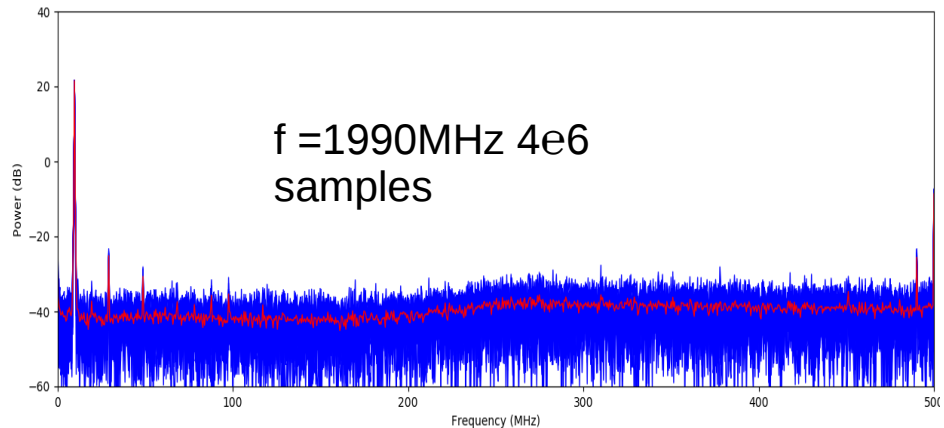
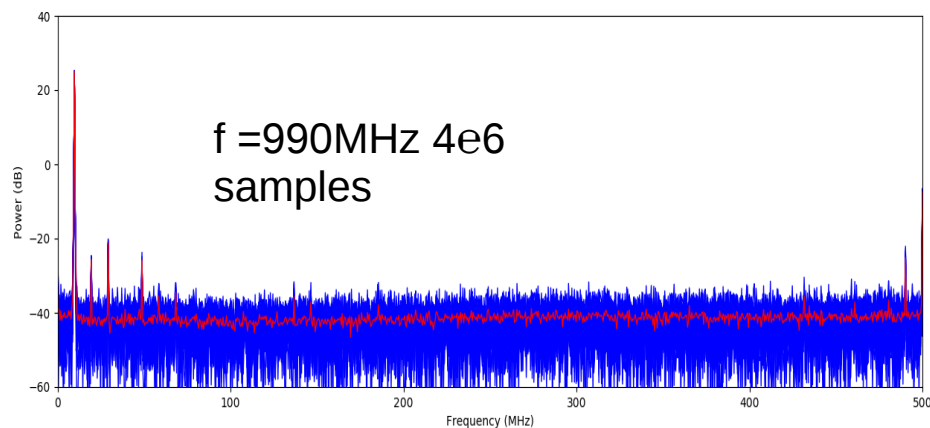
test_490M234375, Acc = 20

test_1490M234375, Acc = 20



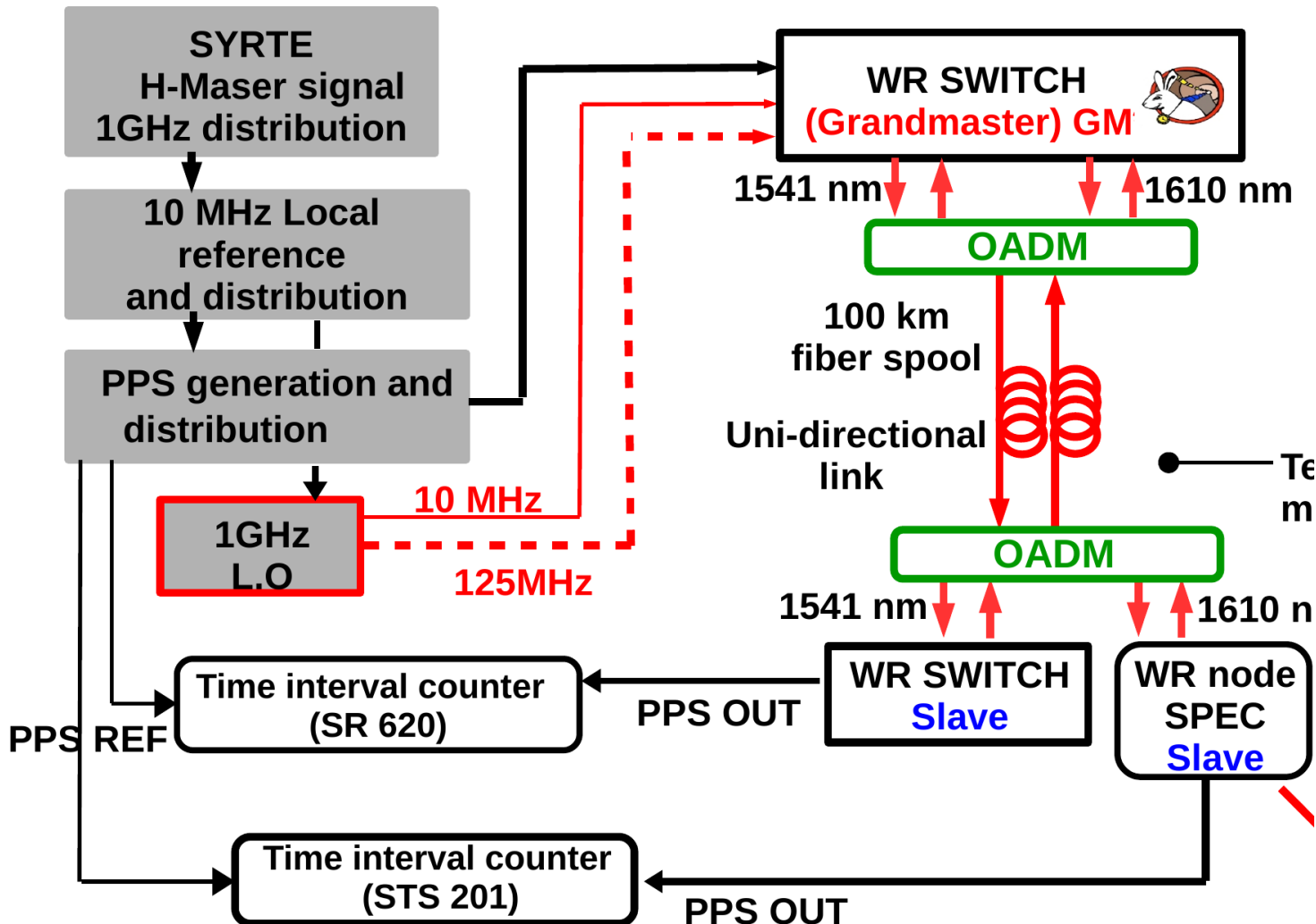
test_990M234375, Acc = 20

test_1990M234375, Acc = 20





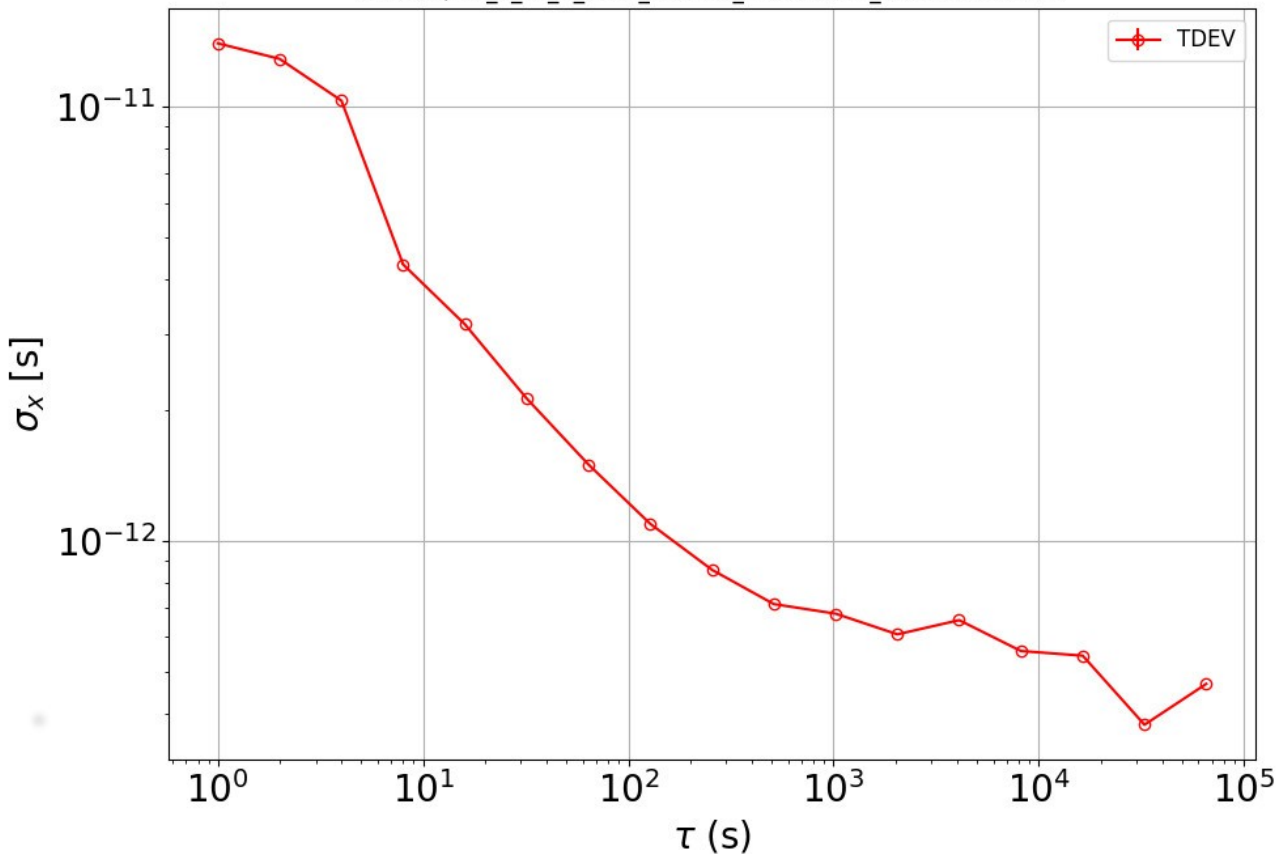
Carte NEBULA, système de test WR





Carte NEBULA, Test PPS

dataGT\site_0_ch_B_Time_Interval_24-11-2017_12.11.11.346.txt



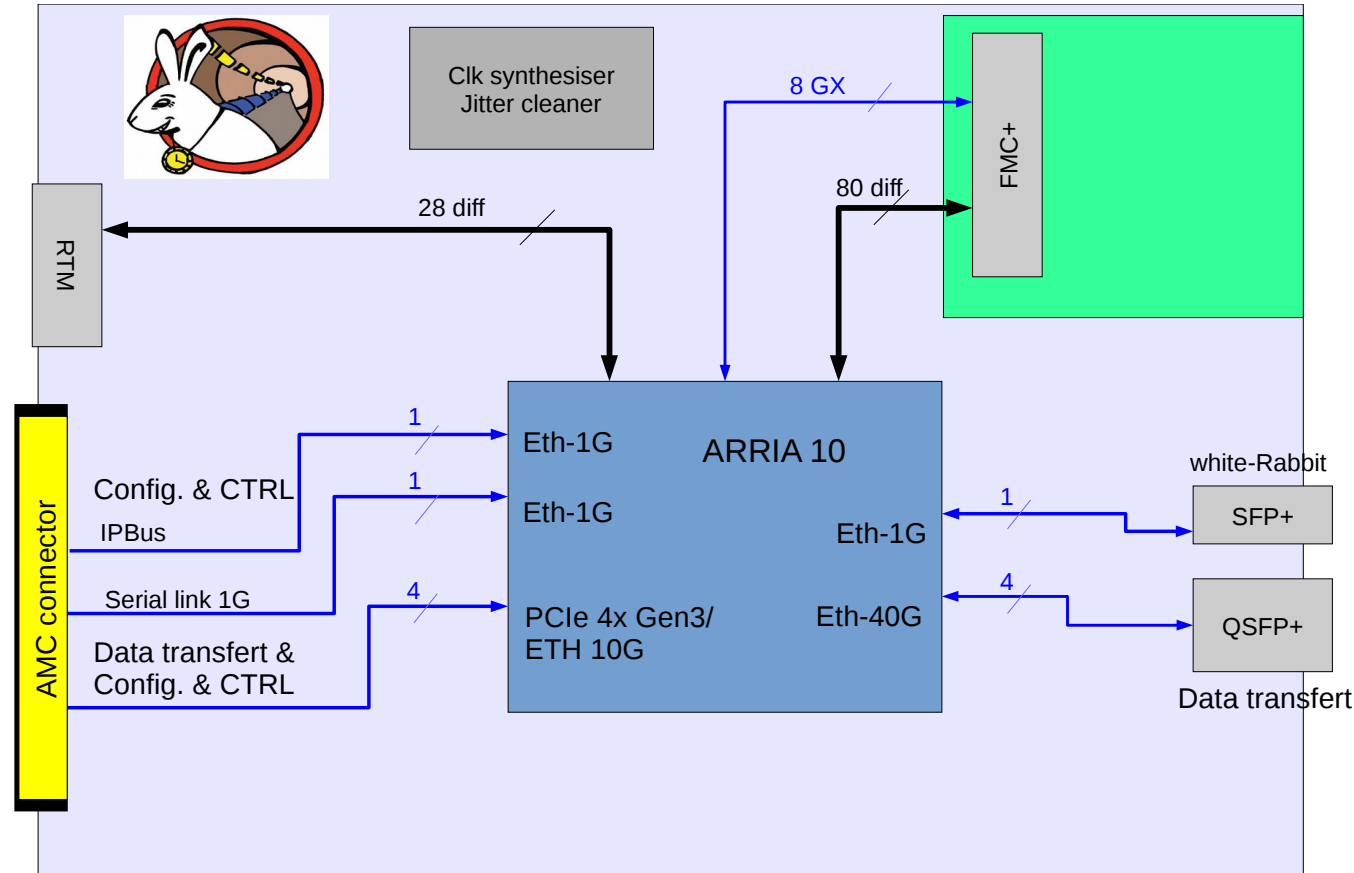
- En collaboration avec le laboratoire SYRTE (Obs Paris INSU).
- 400 Fs après 1000s et 100 Km fibre
- Tests à venir :
 - long période d'analyse (Etude des dérives lentes)
 - Reproductibilité de l'IP WR en fonction des firmwares.
 - Modification des fréquences de la DDMTD.
 - Modification de la soft PLL



Carte IDROGEN

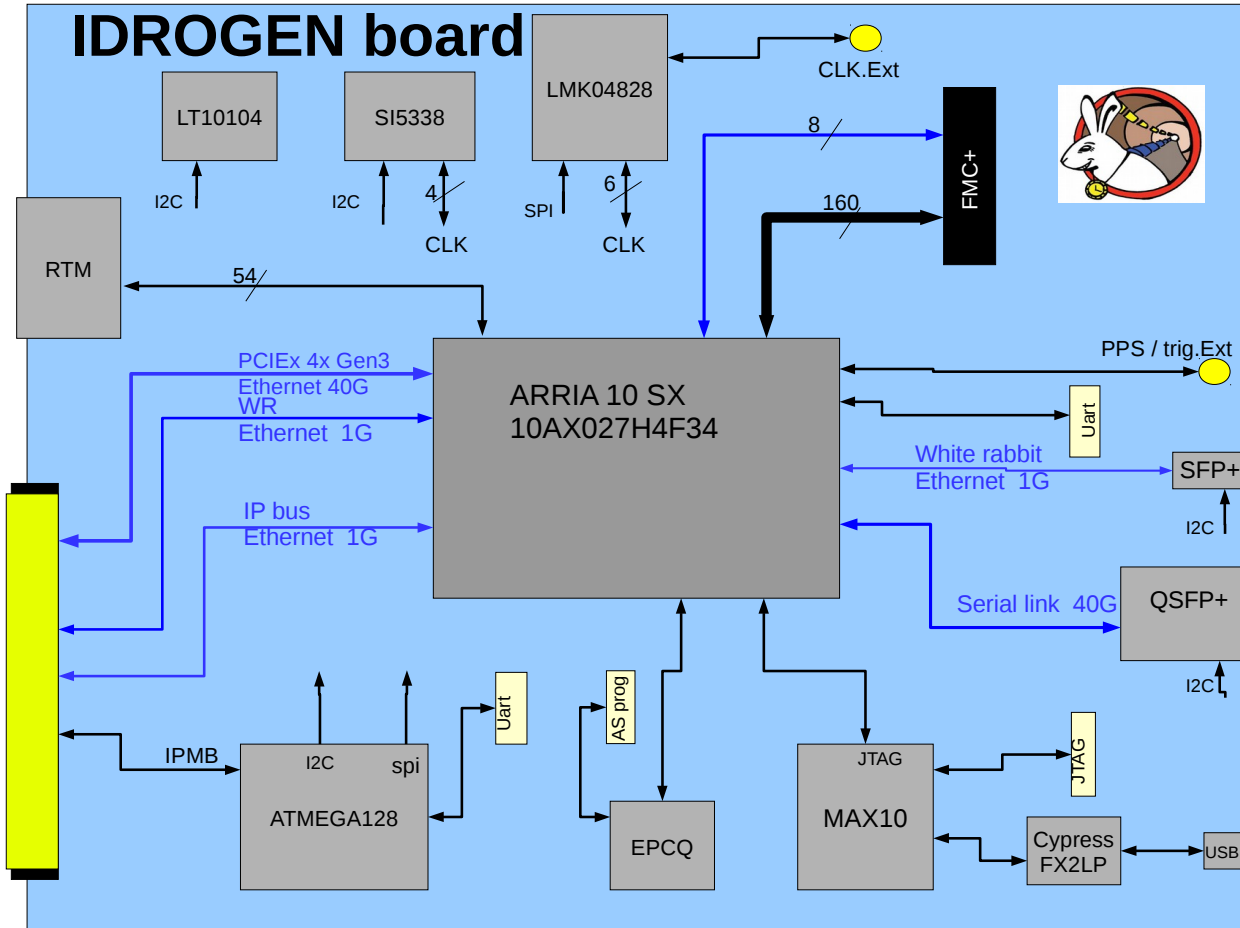
Carte IDROGEN

- MTCA 4.0 standard, Double-width, full size AMC.
- FPGA : 10GX027H4F34
- Stand alone mode (power 12v)
- HighPinCount FMC slot.
- White Rabbit compliant.
- Front panel connectivity : WR SFP+ QSFP+ 40G, USB
- Backplane connectivity : 1Gbe IPbus, PCI 4x Gen3, IPMB, CLK & trigger lane.
- RTM connector : J30.
- Low cost



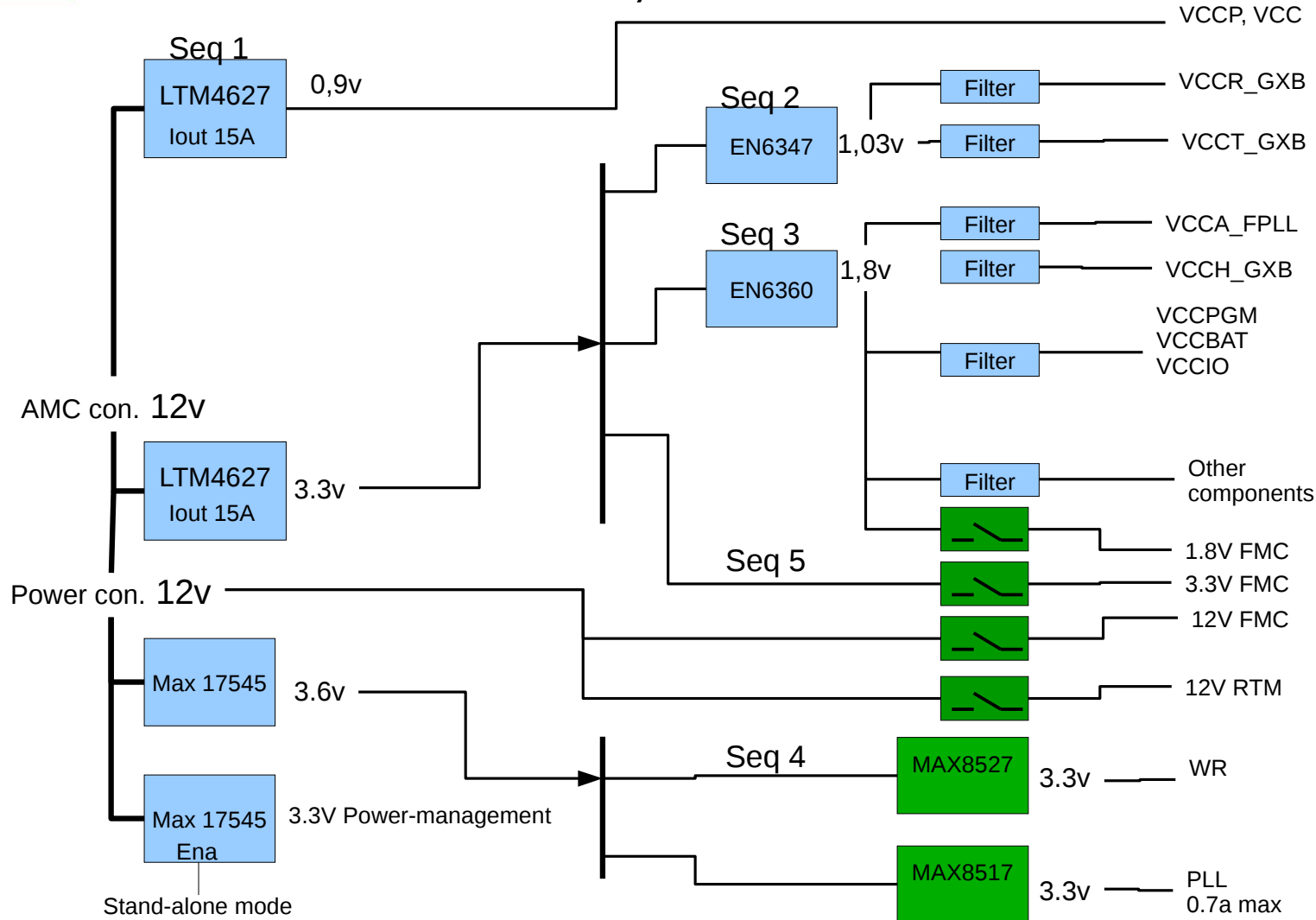
Carte IDROGEN

- On board configuration (μC)
- Very low noise synthesizer PLL synthesizer cleaner (LM04828) for WR clk and derived clk.
- Dedicated PLL for serial links
- Integrated USBBlaster II.
- FPGA configuration : Active serial, IP bus.
- External connectivity : PPS, Trigger, Ext CLK.



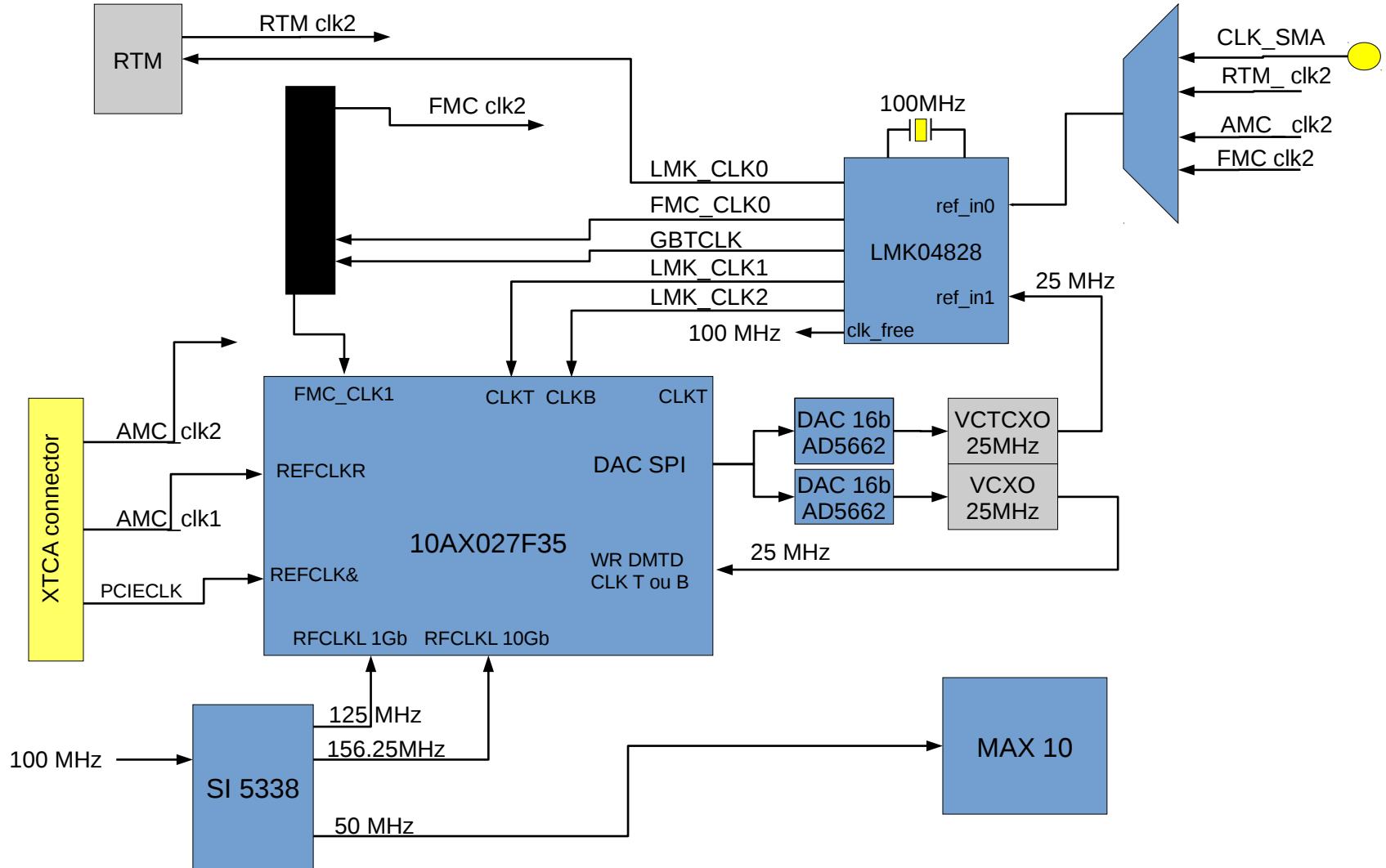


Carte IDROGEN, arbre des alimentations



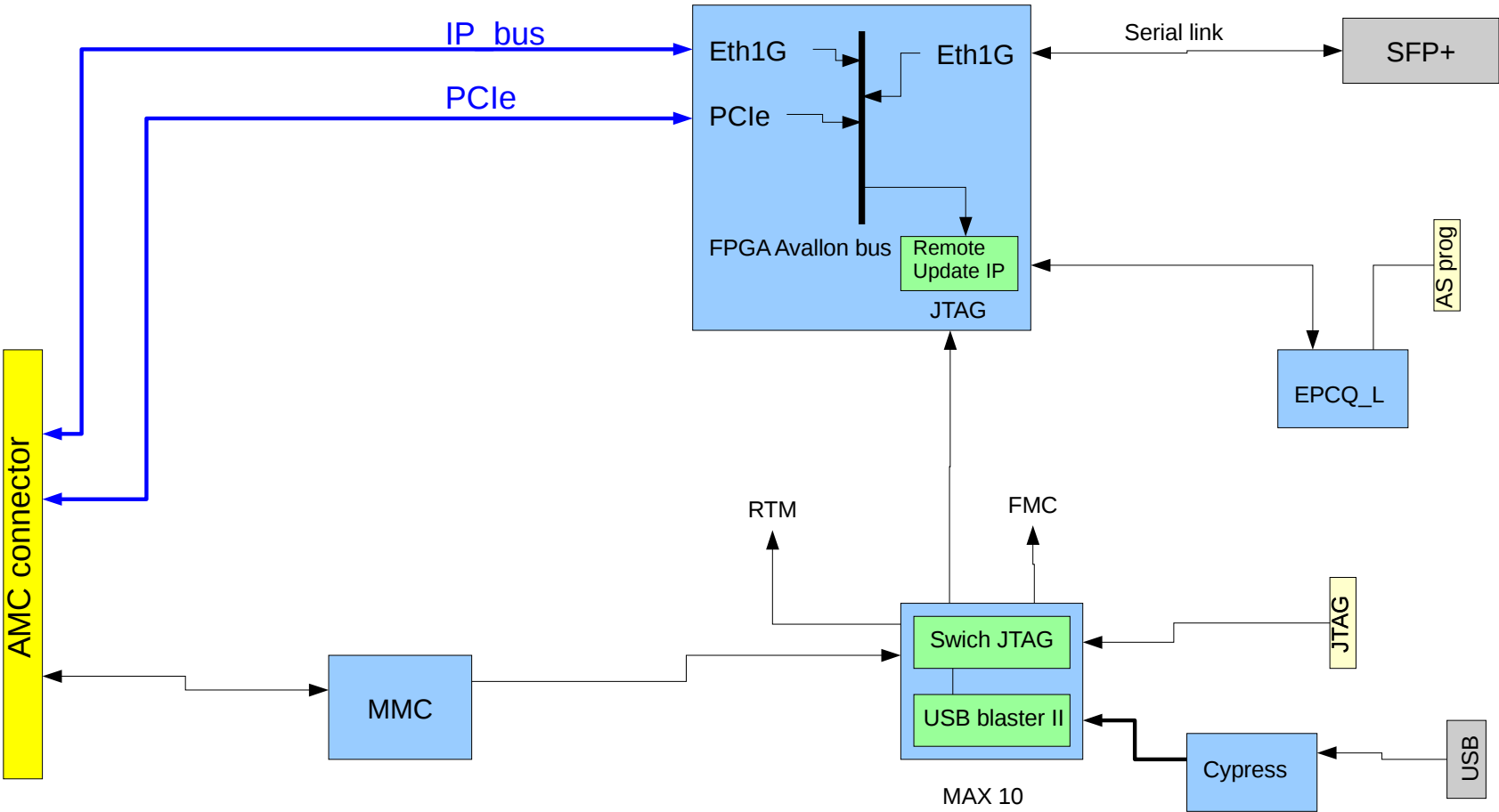


Carte IDROGEN, arbre d'horloges



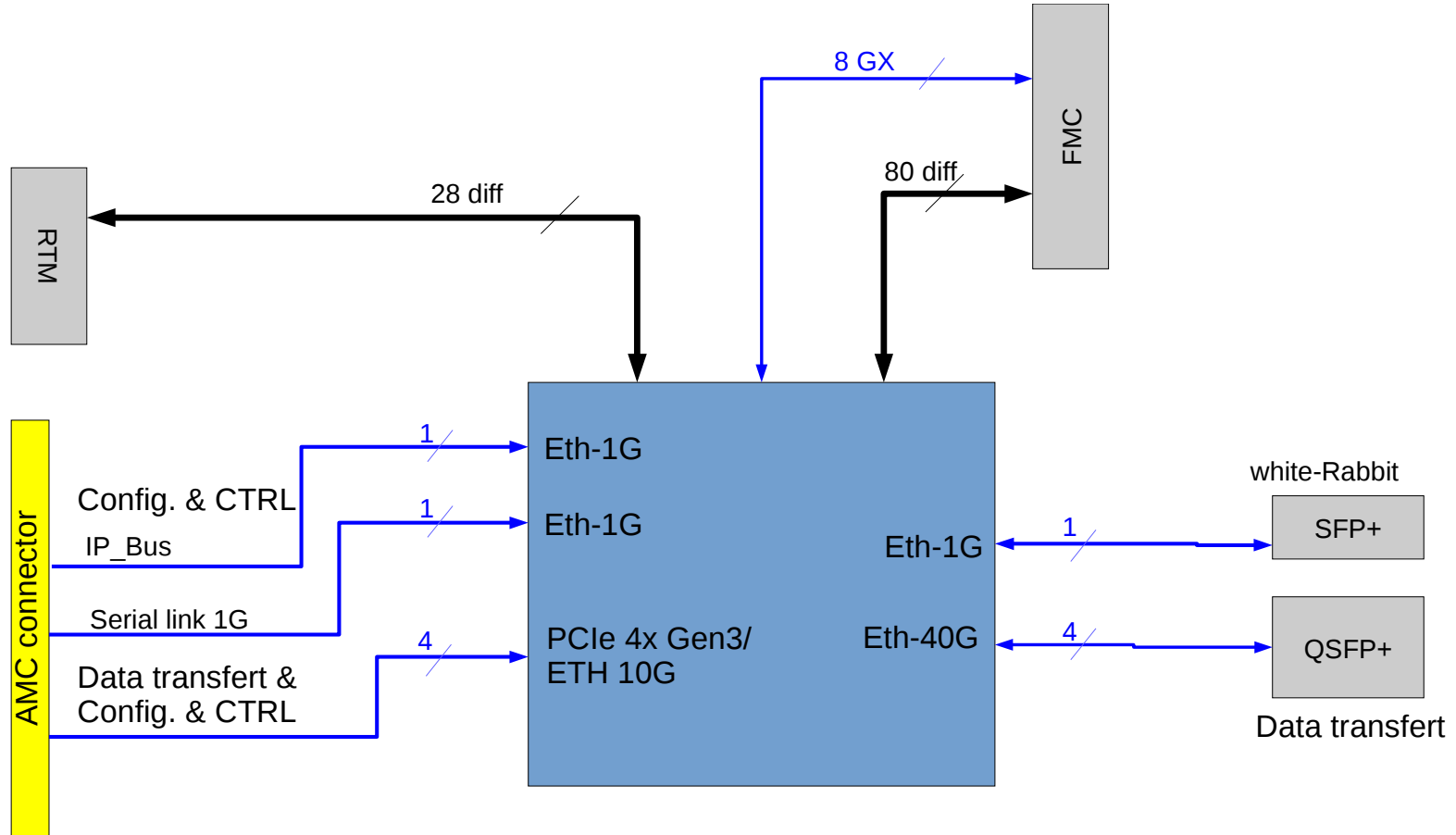


Carte IDROGEN, configuration FPGA



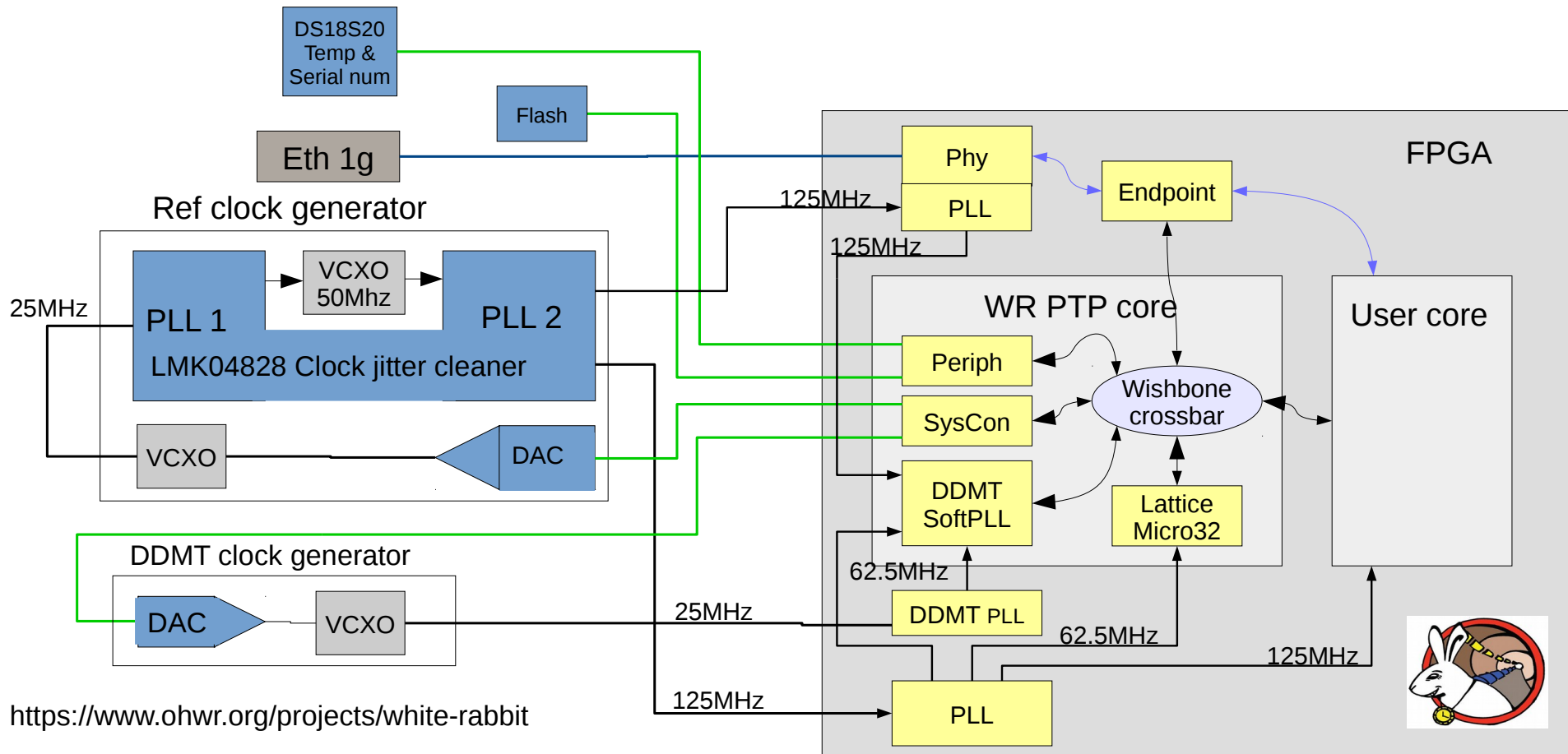


Carte IDROGEN, bus





Carte IDROGEN, arbre horloge WR

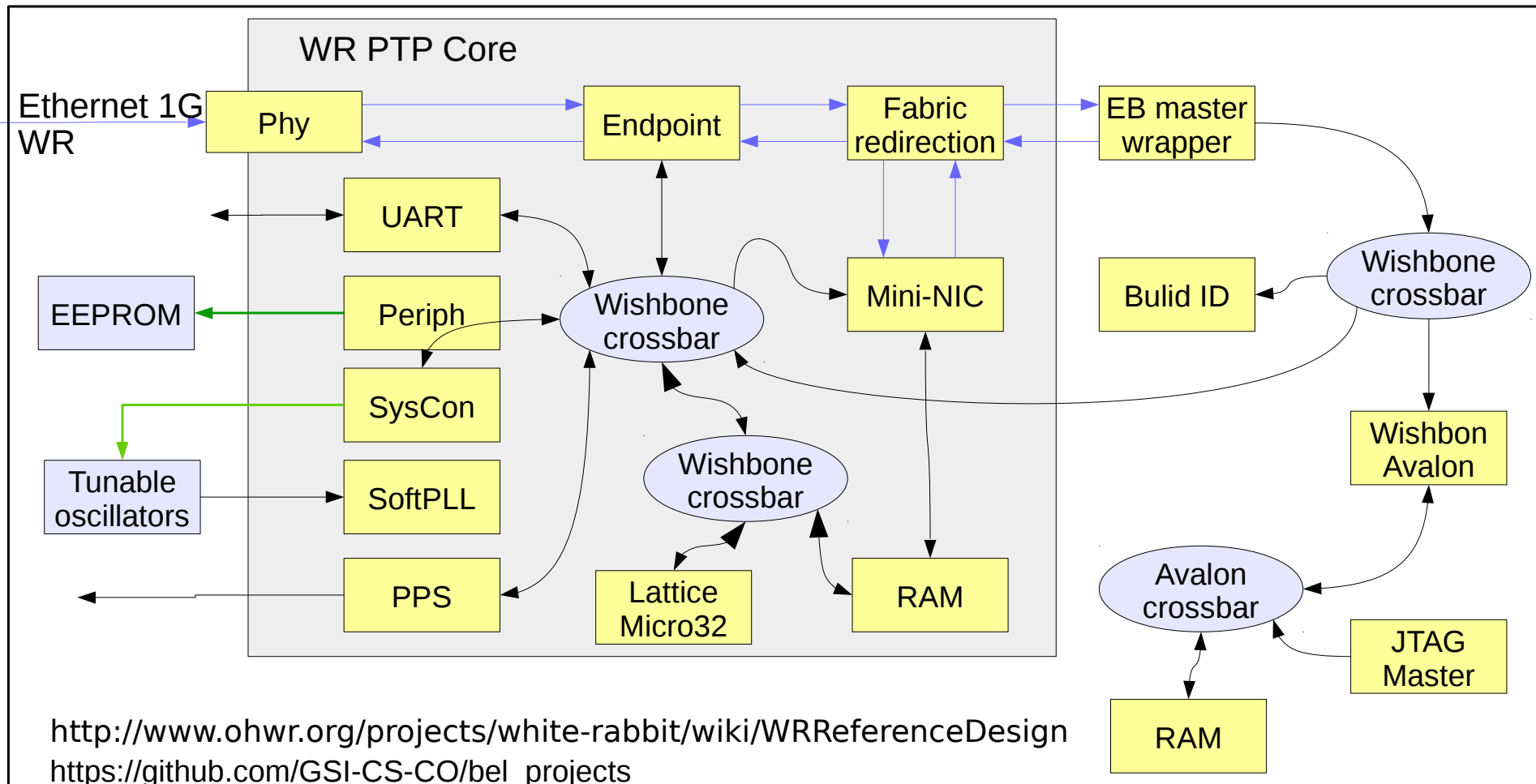


<https://www.ohwr.org/projects/white-rabbit>



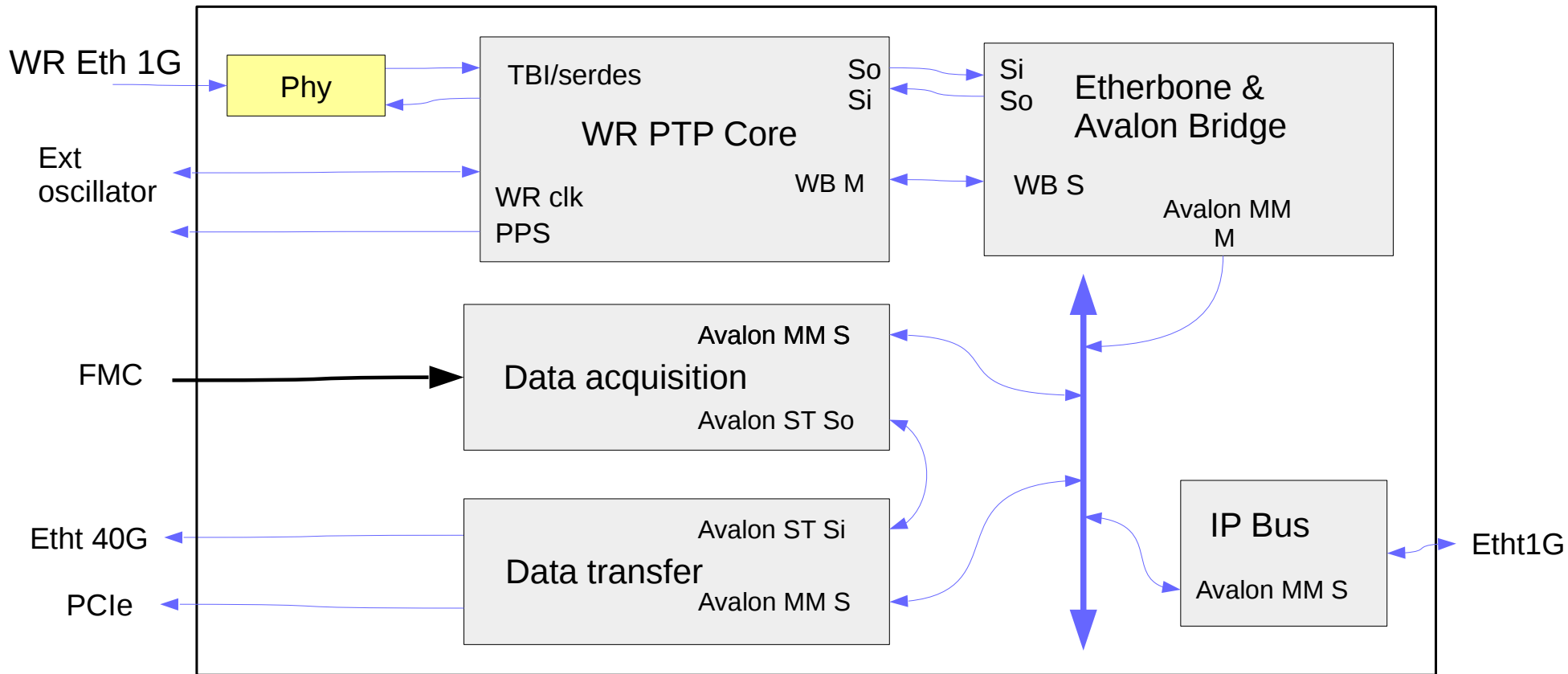


Firmware White Rabbit

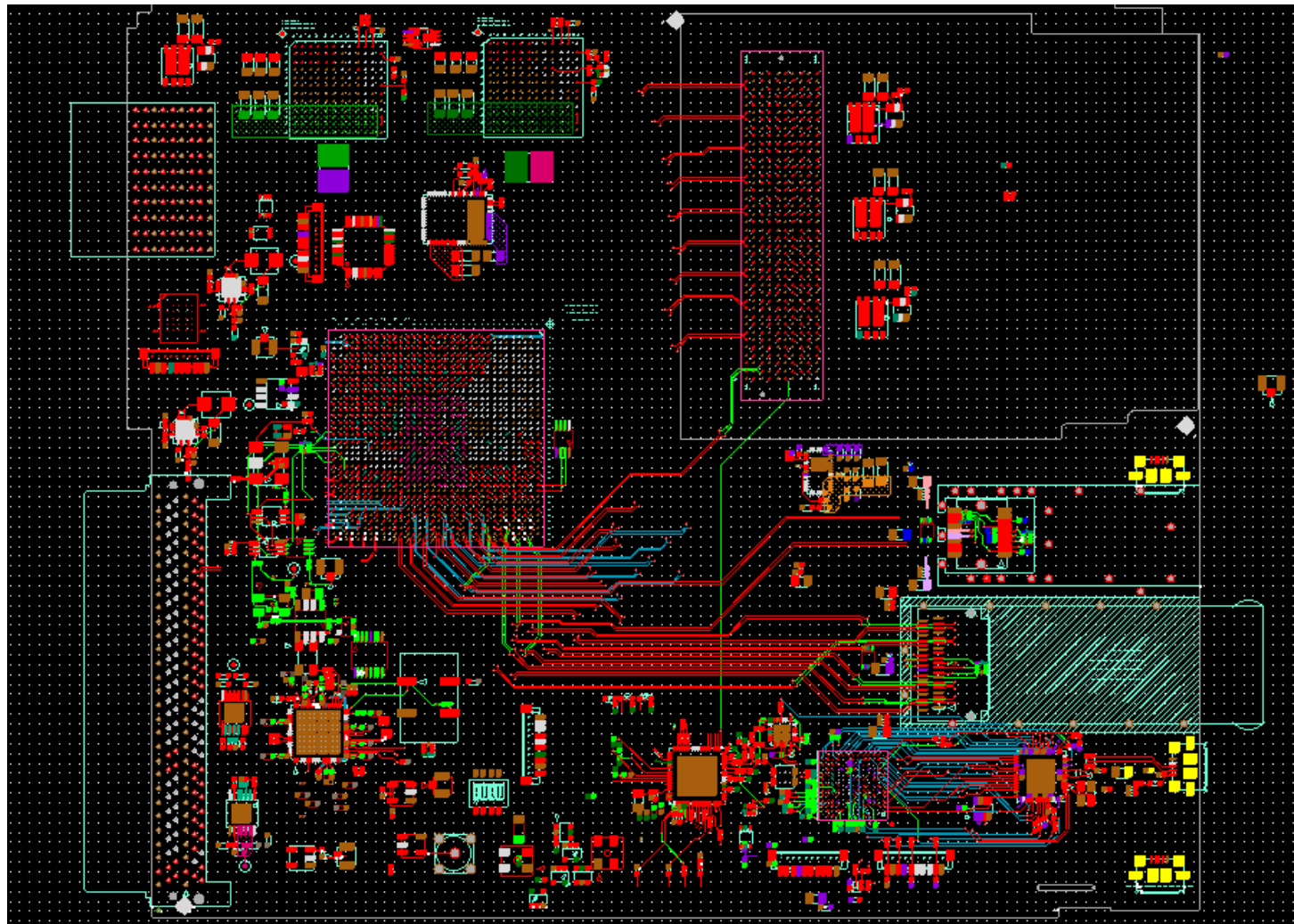




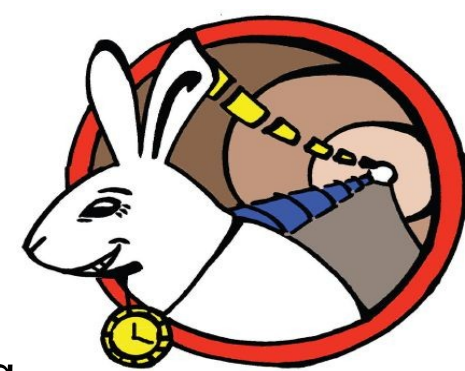
Firmware IDROGEN



Carte IDROGEN



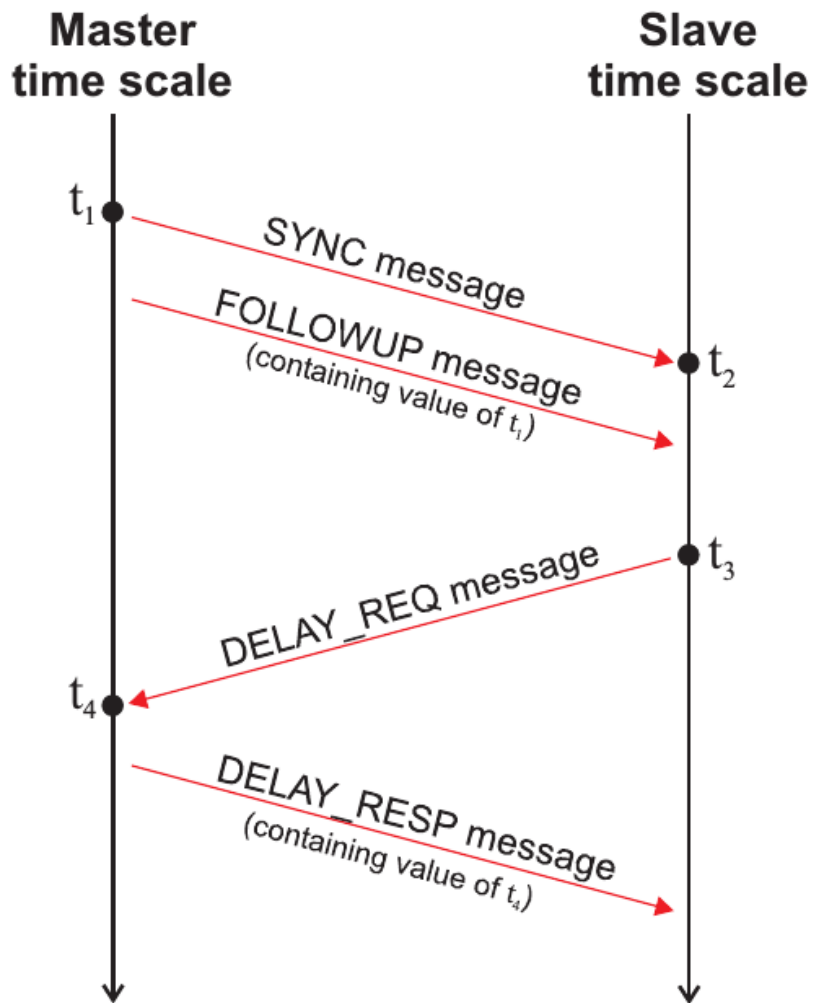
WHITE RABBIT



- An **extension** to **Ethernet** which provides:
- Synchronous mode (Sync-E)
 - Deterministic routing latency
 - Sub-nanosecond synchronization in WR is achieved by using the following three technologies together:
 - Precision Time Protocol (IEEE1588).
 - Synchronous Ethernet.
 - DMTD phase tracking.

Open hardware (CERN)

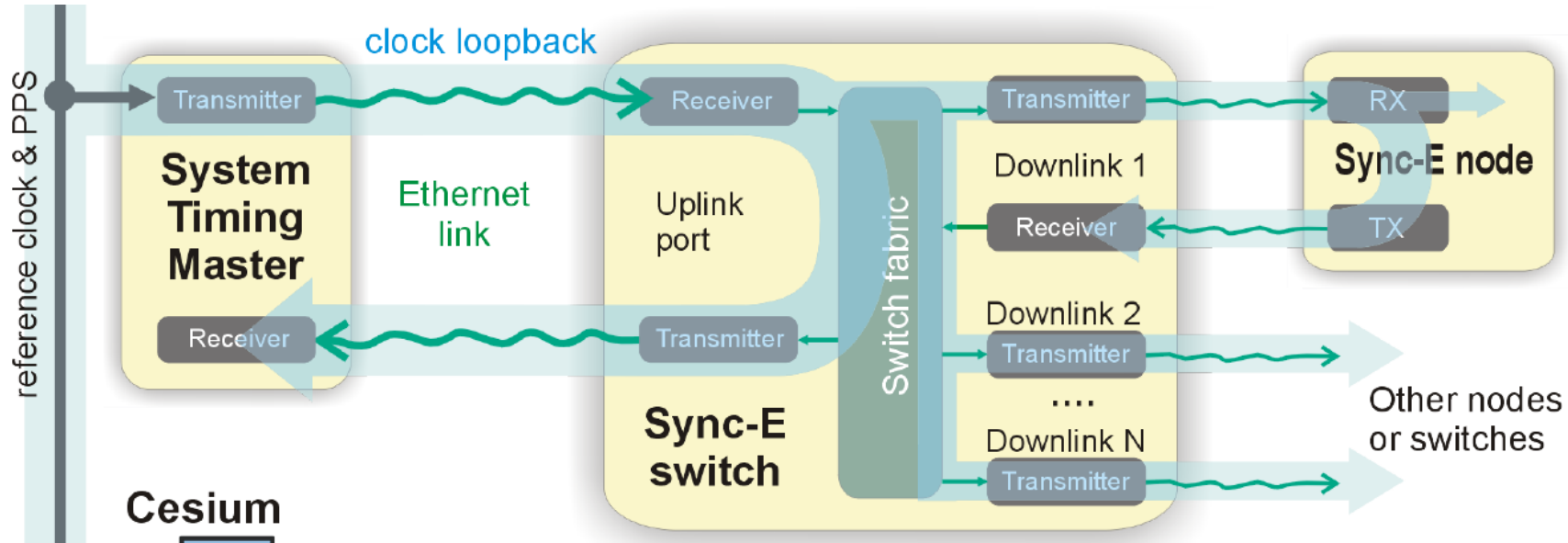
Precision Time Protocol (IEEE1588)



- Synchronizes local clock with the master clock by measuring and compensating the delay introduced by the link.
- Link delay is measured by exchanging packets with precise hardware transmit/receipt timestamps.

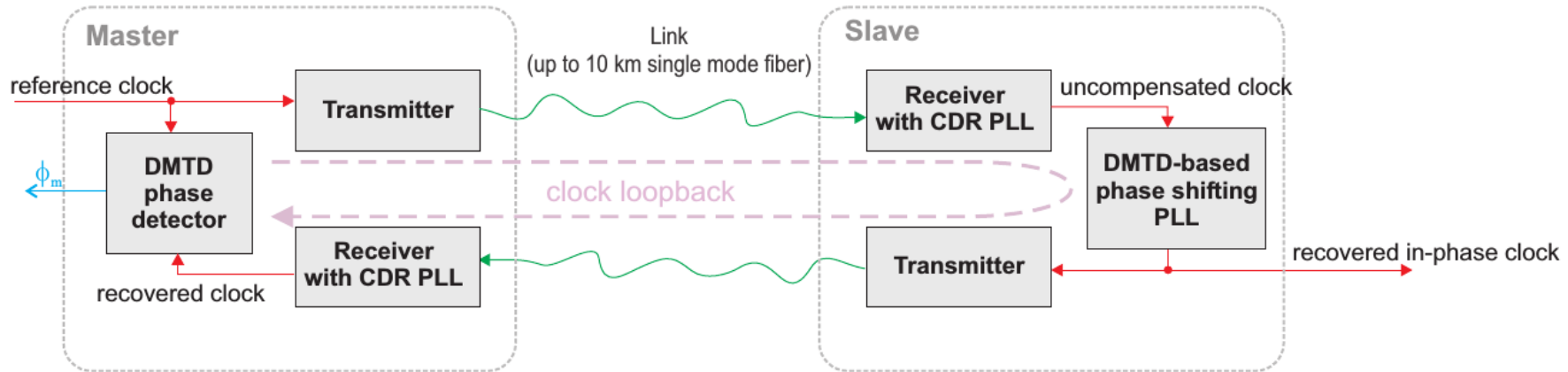
Synchronous Ethernet

- All network nodes use the same physical layer clock, generated by the System Timing Master.
- PTP is used only for compensating clock offset.
- Having the same clock frequency everywhere enables phase detector technology as the means of measuring time.



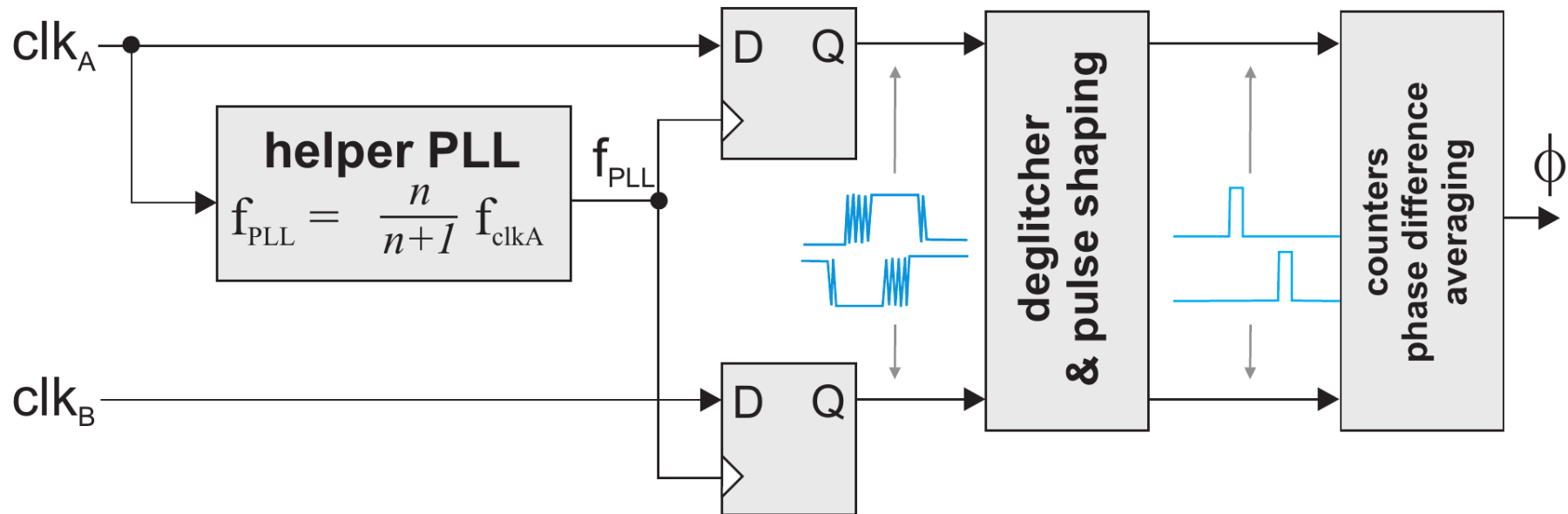
Phase tracking

Measure the phase shift between transmit and receive clock on the master side, taking the advantage of Synchronous Ethernet.

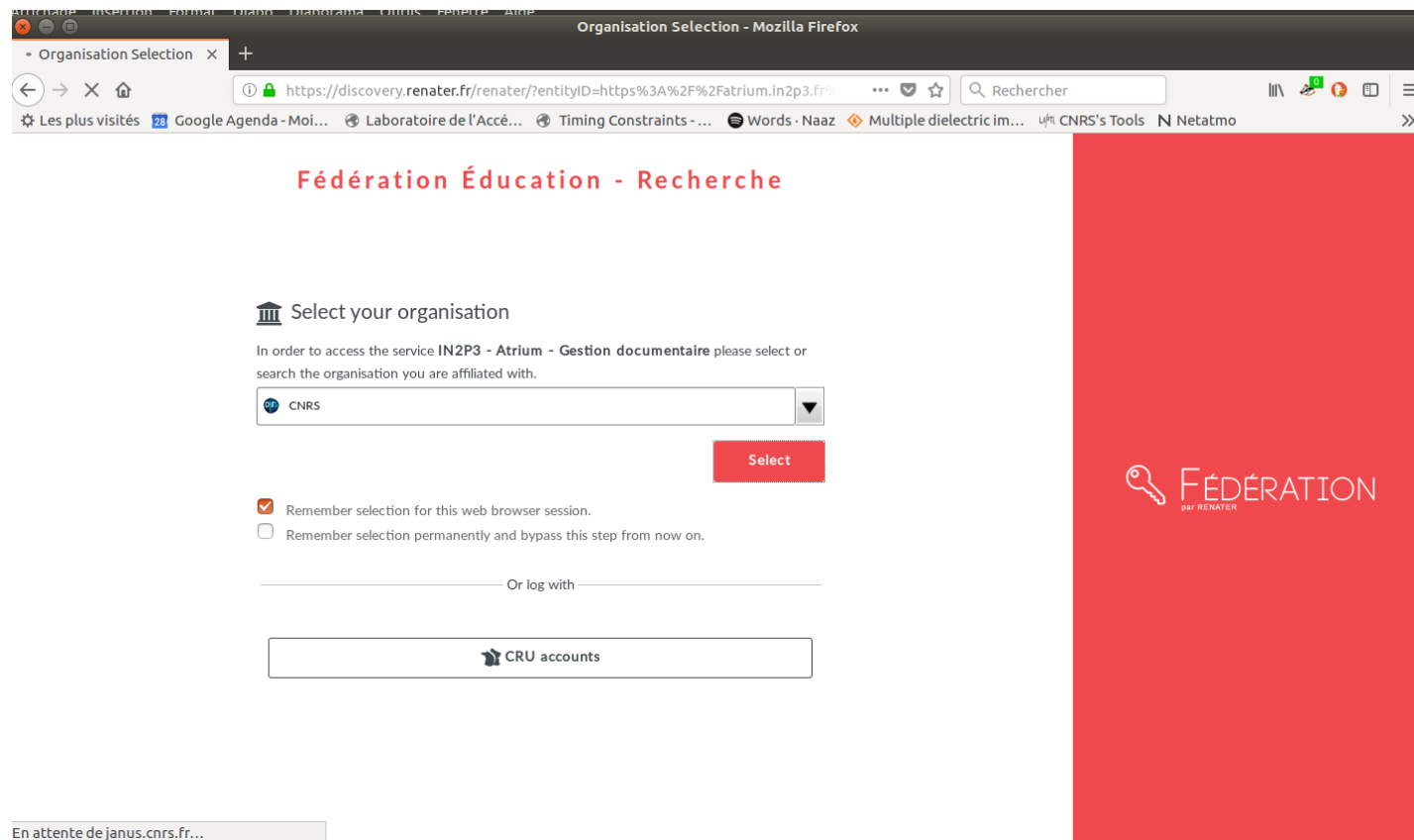


Monitor phase of bounced-back clock continuously.
Phase-locked loop in the slave follows the phase changes measured by the master.

Digital Dual Mixer Time Domain phase detector



Documentation



Organisation Selection - Mozilla Firefox

https://discovery.renater.fr/renater/?entityID=https%3A%2F%2Fatrium.in2p3.fr%...

Les plus visités 28 Google Agenda - Moi... Laboratoire de l'Accé... Timing Constraints - ... Words - Naaz Multiple dielectric im... CNRS's Tools Netatmo

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Software DCOD framework

- DCOD Framwork

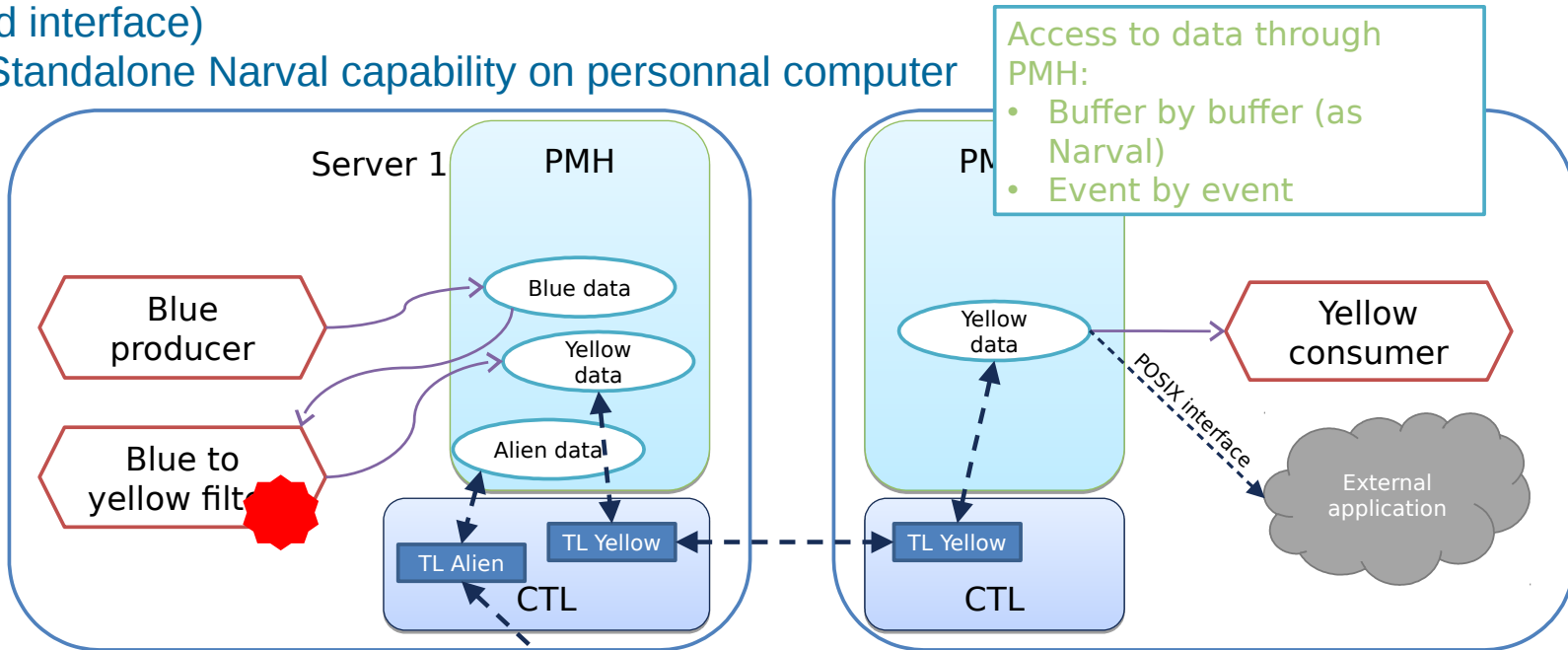
- PMH – Posix Memory Handler
- CTL Common Transport Layer
- Narval acquisition : distributed acquisition system
- ENX : slow control et configuration (unified interface)

- DCOD tools :

- DCOD lancer : a process to control them all
- DCOD monitor (Distributed framework)
- Implemented on further detectors : AGATA, VAMOS,

....

Standalone Narval capability on personal computer

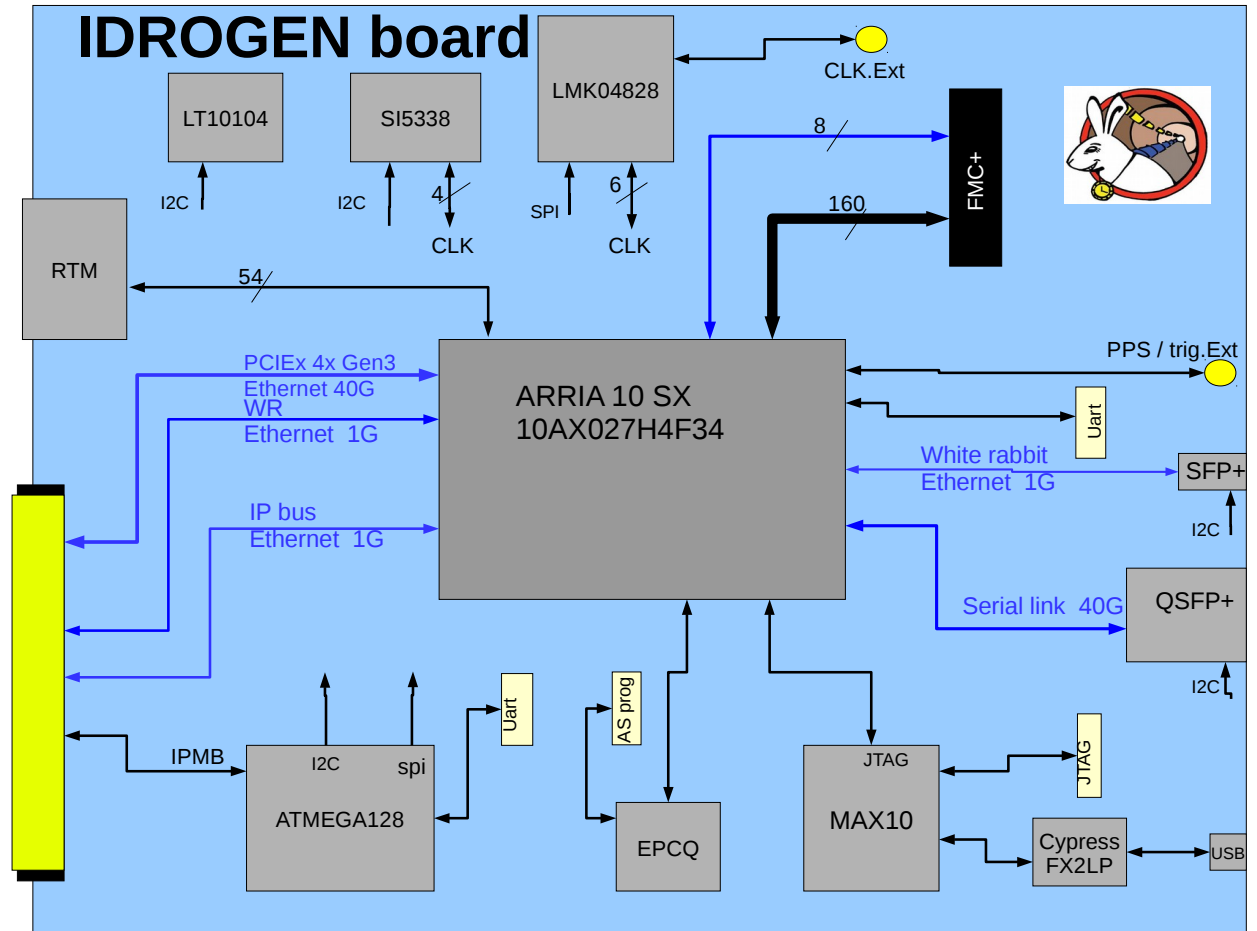


Conclusion

- Carte en cours de routage, test en fin d'année.
- Firmware développé sur la carte d'évaluation (ATILA sce REFLEX).
- Le portage de DCOD sur IDROGEN sera testé sur la carte d'évaluation par le CSNSM.
- IDROGEN Disponible début 2019.
- Mezzanine FMC basée sur open hardware IDROGEN sera développée pour projet AGATA.

Carte IDROGEN

- MTCA 4.0 standard, Double-width, full size AMC.
- FPGA : 10GX027H4F34
- Stand alone mode (power 12v)
- HighPinCount FMC slot.
- White Rabbit compliant.
- On board configuration (μ C)
- Very low noise synthesizer PLL synthesizer cleaner (LM04828)
- Front panel connectivity : WR SFP+ QSFP+ 40G, USB
- Backplane connectivity : 1Gbe IP bus, PCI 4x Gen3, IPMB, CLK & trigger lane.
- RTM connector : J30.
- Integrated USBBlaster II.
- FPGA configuration : Active serial, IP bus.
- External connectivity : PPS, Trigger, CLK.
- ²⁾ Low cost



Empilement

1	55	Signaux	100 Ohm
2	35	GND	
3	17	Signaux	100 Ohm
4	35	PWR	3.3v
5	17	Signaux	50 Ohm
6	70	GND	
7	70	PWR	0,9v/12v /1,8v
8	17	Signaux	50 Ohm+ PWR
9	35	GND	
10	17.	Signaux	100 Ohm
11	35	GND	
12	55	Signaux	100 Ohm



75	1
100	2
100	3
90	4
75	5
64	6
75	7
90	8
100	9
100	10
75	11
954	