The WaveCatcher Systems: fast multi-purpose digitizers for instrumentation

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Introduction

- The WaveCatcher systems are **fast multi-purpose digitizers** based on the SAMLONG full custom ASIC
- They can **replace oscilloscopes** in many cases with a lower cost per channel and offer smart functionalities
- The number of channels of desktop systems ranges between **2 and 64**
- A powerful **software and C libraries** are available
- Their main use is for **test benches or detectors requiring high precision** with a limited number of channels, but larger systems based on WaveCatcher boards have also been developed for **physics experiments** (currently close to 1000 channels)

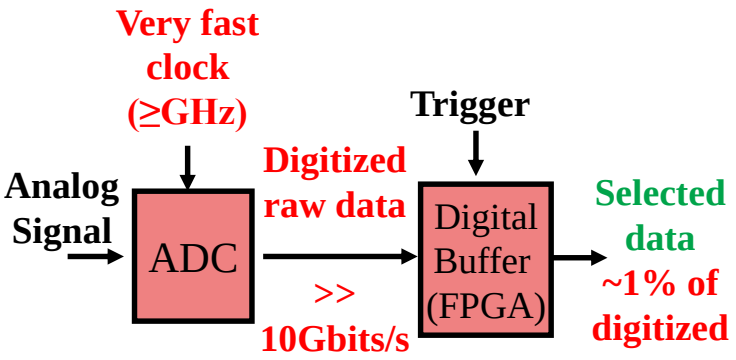
State of the art: digitization

- New trends in data acquisition are to digitize the signal as soon as possible in the chain and to perform a digital treatment of information
  - Waveform indeed **contains all information** (if properly digitized)
  - Depending on the information requested (amplitude, charge, time, FFT, …), **different types of algorithms** will be used for its extraction
  - A very challenging goal has now become to find the **simplest effective algorithms** which could be integrated within companion FPGAs
  - Waveforms can be used for designing **high performance TDCs**
  - **Signal to noise ratio** is always an issue, even for a for TDC

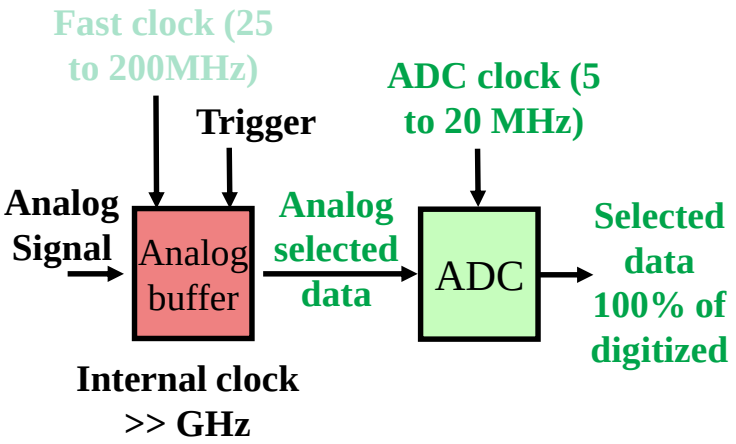
- In some cases, it is mandatory to use fast flash ADCs
  - When the **trigger** is performed on digitized data (oscilloscopes, …)
  - When a **constant data stream** is necessary (even if the latter will just end up in the companion FPGA) => real time FFT for instance
  - But whenever a short time window and a « reasonable » hit rate are present, **analog memories** really seem to be a good answer…

Analog Memories vs ADCs

- In terms of digitizers, high-end oscilloscopes are the costly grail (>25k€/ch) but with only 4 channels …
- They are based on fast interleaved ADCs
- High precision measurement implies high sampling rate (>> GS/s) => huge amount of data (10 to 100 Gbits/s per channel), high power
- Digitizers based on analog memories (SAMLONG, DRS4, TARGET, BLAB…) are a nice solution because:
  - they can sample the signal as fast as the ADCs
  - they digitize only useful data at lower speed => smaller cost and power
  - TDC is "built-in" (position in the memory gives the time)
  - but their readout dead-time (~2 to a few 100's µs) limits the rates and all channels are usually triggered together (oscilloscope like)
- Analog memories are a widely used solution for high precision measurements at large scale



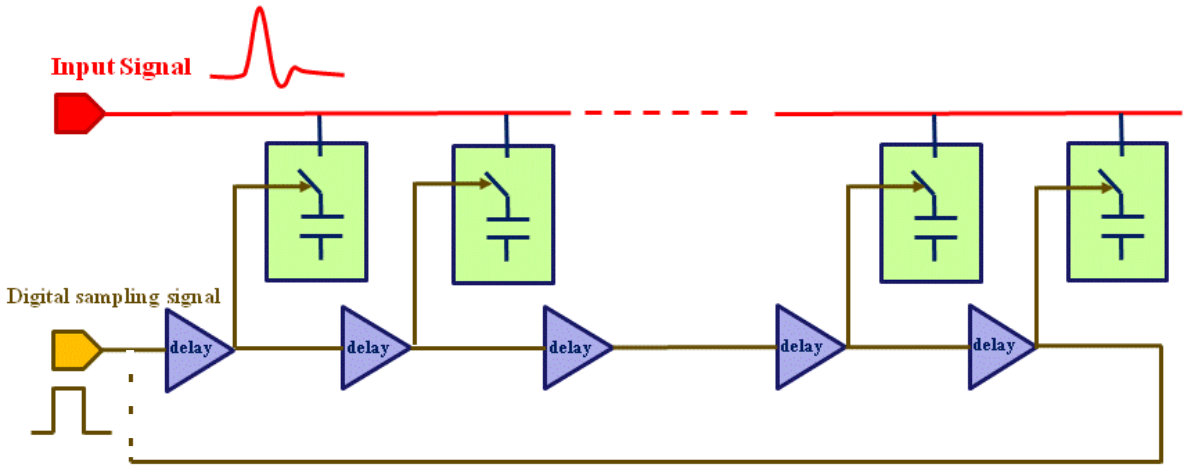
ADC-based digitizer



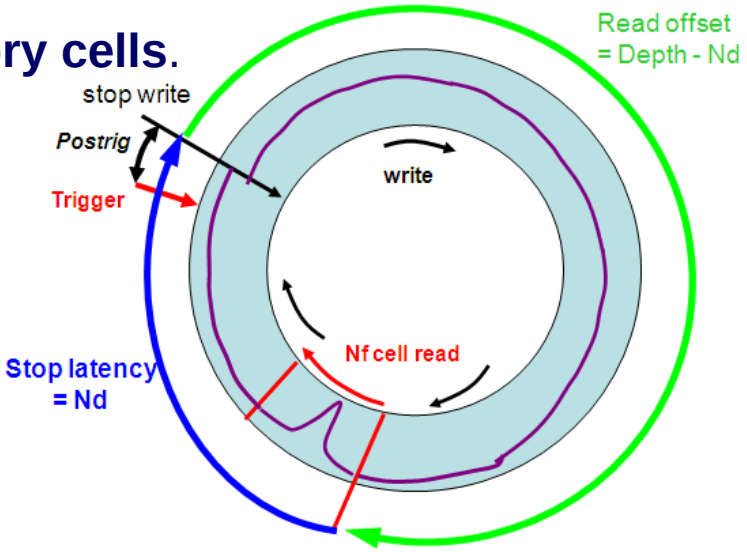
Analog_memory-based digitizer

Circular analog memories: basic principles

An analog memory can record waveforms at very high sampling rate (>>GS/s)
After trigger, they are digitized at much lower rate with an ADC (5/10/20/… MHz)



- A write pulse is running along a **delay line** (DLL).
- It drives the recording of signal into **analog memory cells**.
- Sampling stops upon a **trigger signal**.
- **Readout** can target an area of interest, which can be only a **subset** of the whole channel
- **Dead time** due to readout should remain as small as possible.

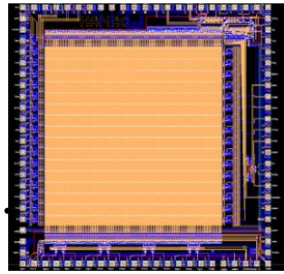


Our favourite solution: a Sampling Matrix

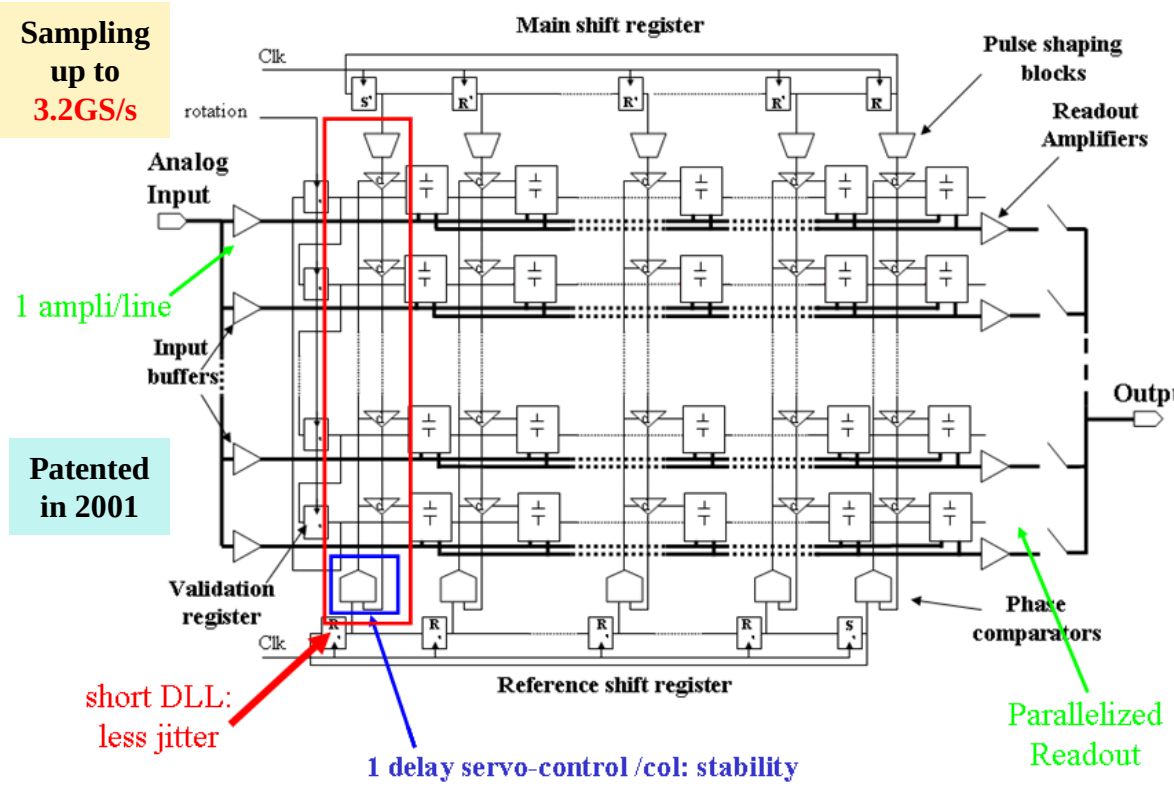
• We started designing analog memories in 1992 with the first prototype of the Switched Capacitor Array (SCA) for the ATLAS LARG calorimeter. 80,000 HAMAC chips produced in 2002 and mounted on the boards which **measured the Higgs energy**. They are still on duty on the LHC for long…

• Since 2002, many new generations of fast samplers have been designed (ARS, MATACQ, SAM/SAMLONG, SAMPIC): more than 50,000 chips in use.

HAMAC
1998-2002



Sampling up to 3.2GS/s

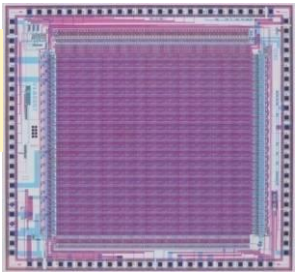


Readout 12/14 bits 5/10/20 MHz

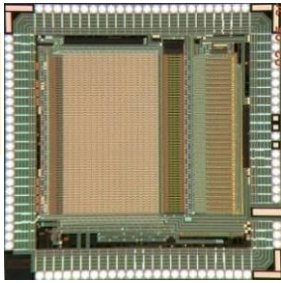
ADC

Patented in 2001

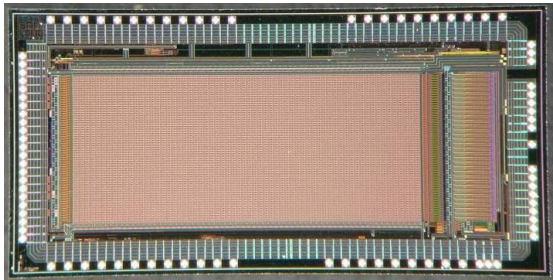
MATACQ
2000-2003



SAM
2005

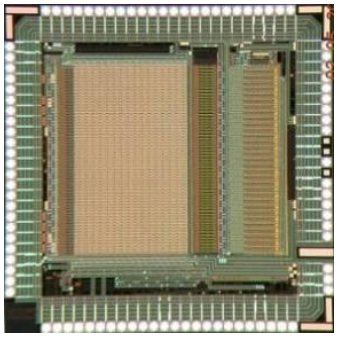


SAMLONG
2010-2012-2018

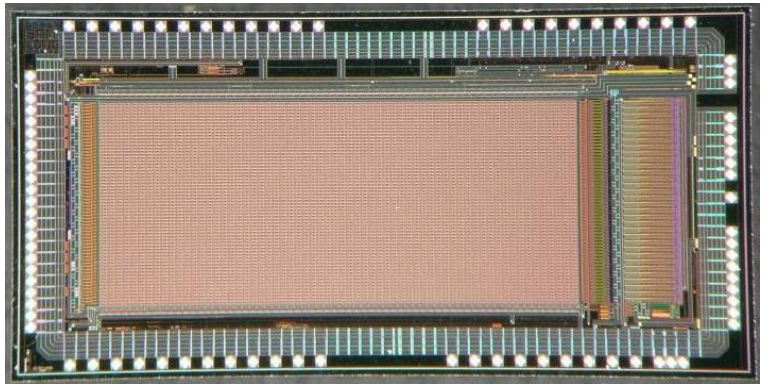


SAM & SAMLONG chips

- Technology: AMS CMOS 0.35µm
- SAM (2x256 cells) submitted in 2005 for HESS experiment.
- First version of SAMLONG submitted in 2010.
- Currently used version submitted in 2012.
- **2 fully differential channels, 0.4 to 3.2GS/s, 500 MHz bandwidth, 1024 sampling cells, 12 bits of dynamic range, readout at 10 MHz (125 µs for the full waveform) or 20 MHz (66µs)**
- 300mW @ 500MHz-BW down to 100mW @ 200 MHz
- Packaged in 100-pin PQFP, pitch of 0.5 mm
- An **updated version** has been designed this summer:
    - better SNR targeting 14 bits of dynamic range
    - integrated DAC for automated time INL calibration



SAM



SAMLONG

The USB_WaveCatcher board (V6)

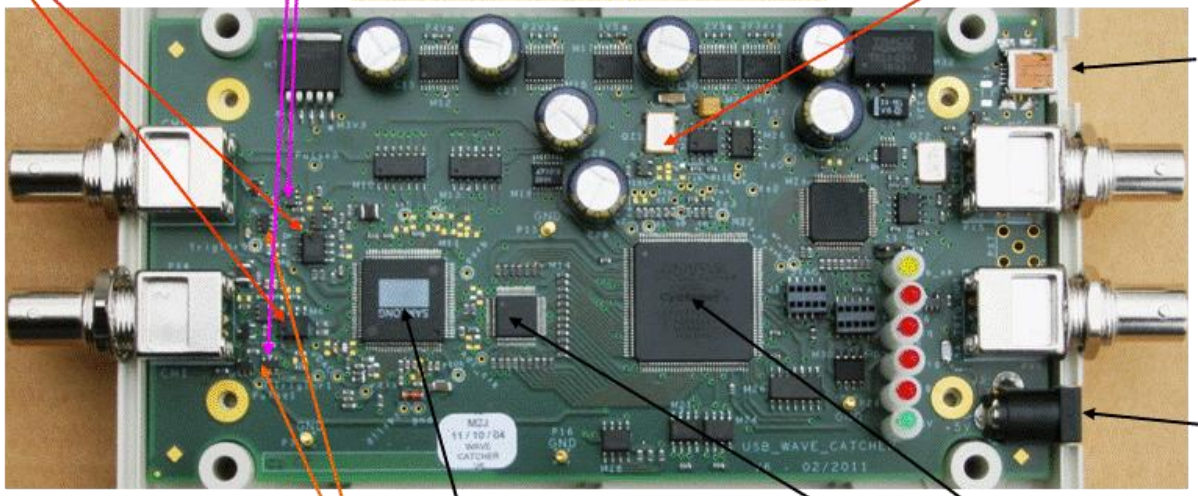
Pulsers for reflectometry applications

1.5 GHz BW amplifier.

Board has to be powered by USB => power consumption ≤ 2.5W

Reference clock: 200MHz => **3.2GS/s**

2008/2011



µ USB

Trigger input

Trigger output

+5V Jack plug

2 analog inputs. DC Coupled.

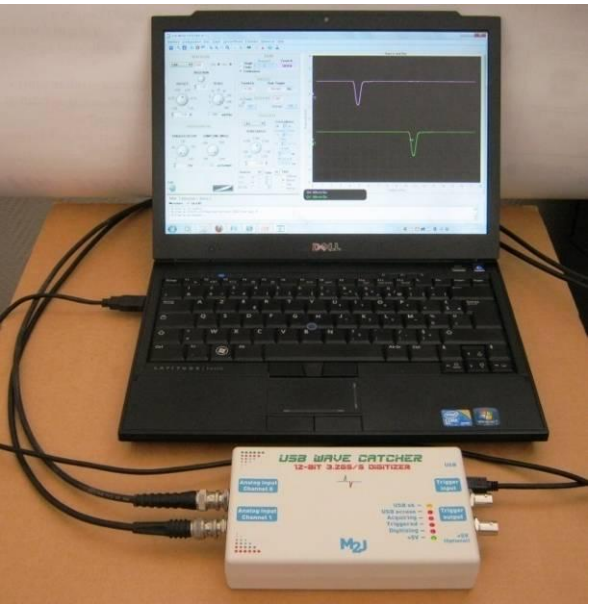
SAM Chip

Cyclone FPGA

Trigger discriminators

Dual 12-bit ADC

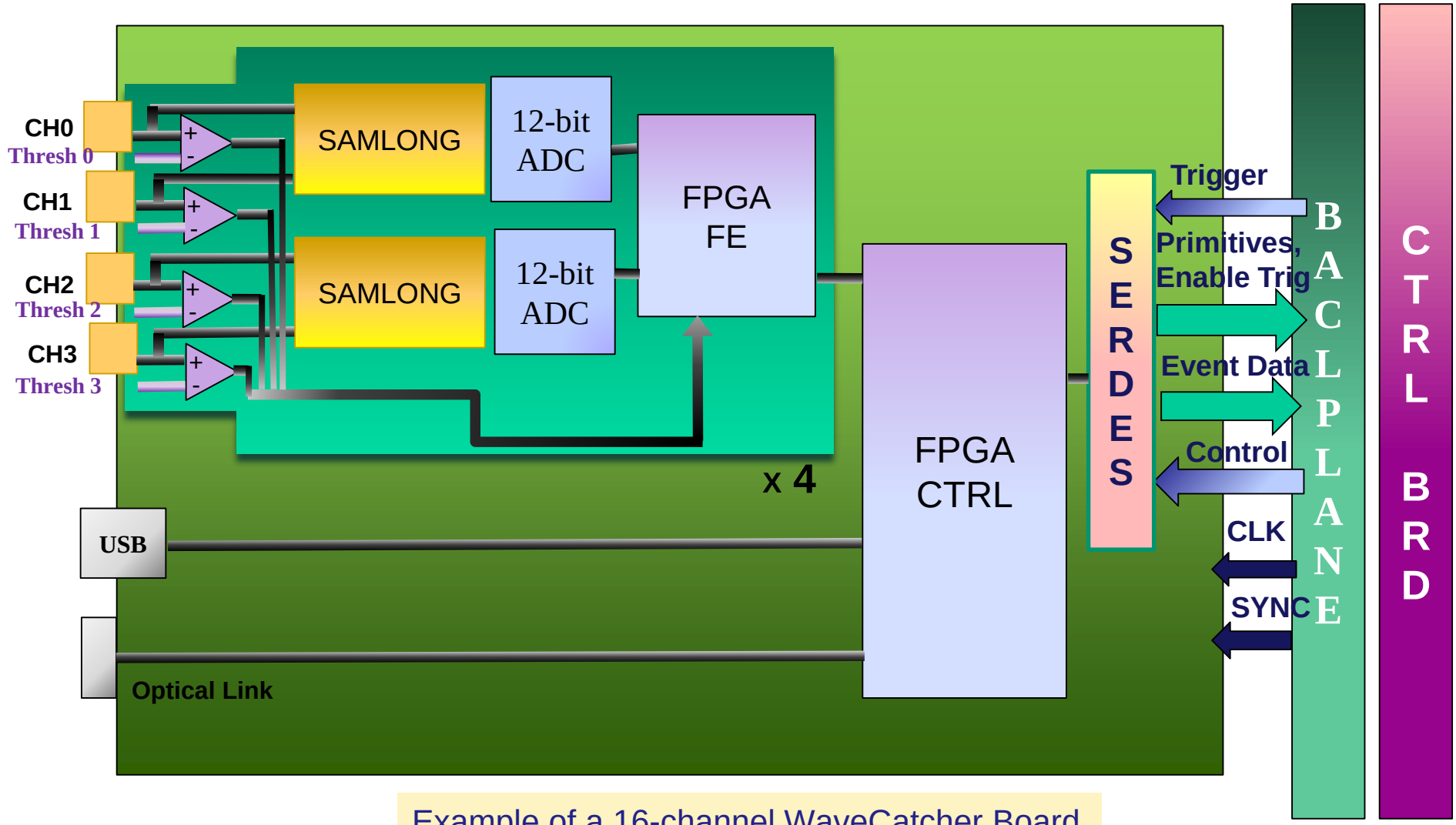
The autonomous test bench



The historical 2-Channel module

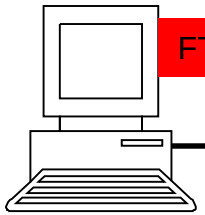
D.

WaveCatcher Front-End Block Diagram



Example of a 16-channel WaveCatcher Board

Control/Readout Protocol: LP-bus Multi-Layer



FT2232H or DP83865DVH

USB/Gbit Ethernet Interface

udp_full_interface

Protocol adatpted to Multi-Layer ''Tree-Like'' Systems

Layer 1

internal registers, Fifos, RAMs …

FPGA

Interface block

LP-in

Reg

Fifo

RAM

LP-out 0

LP-out 1

LP-out N

Libraries : LalUdpML/ LalUsbML by C.Cheikali

A secured version of UDP has been developed (firmware + C library) => No byte loss !

LP-Bus 0

LP-Bus 1

LP-Bus N

FPGA

LP-in

Reg

Fifo

RAM

LP-out 0

LP-out 1

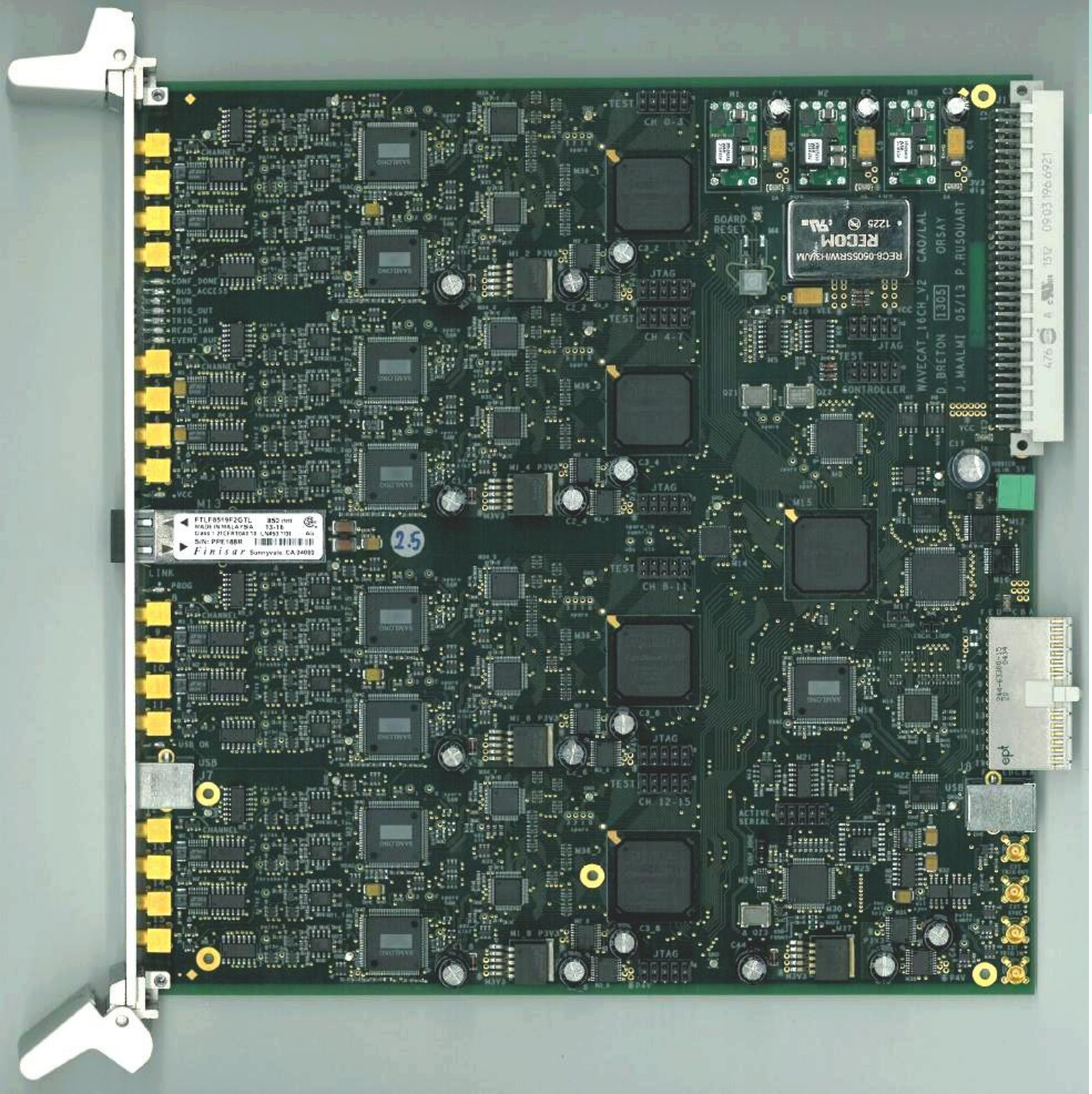
LP-out M

Layer 2

Layer 3

etc …

2011/2013



The 16/18-channel board

- 1.6mm thick
- 10 layers
- 233 x 220 mm²
- **3200 components**
- 25 power supplies (5 global, 20 local)

- Four **4-channel blocks** (can be used as **mezzanines** on other boards)

- **2 extra channels dedicated to « digital » signals**

The 64+8-channel digitizer

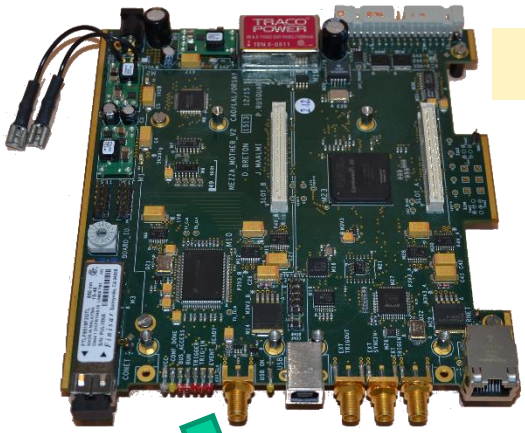
2013

Up to 4 16-channel boards

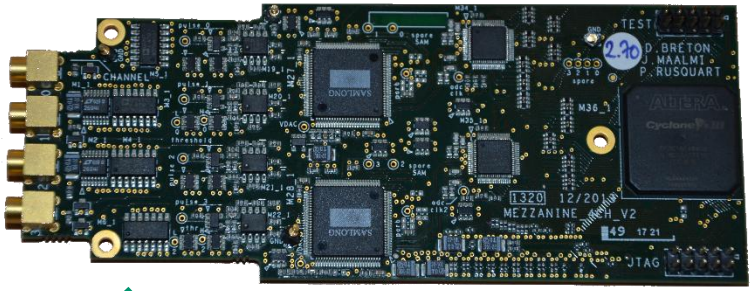
Custom backplane for fast trigger & DAQ links

Controller board: interface with trigger and DAQ

The 8-channel and 16-channel modules



Motherboard



4-channel mezzanine

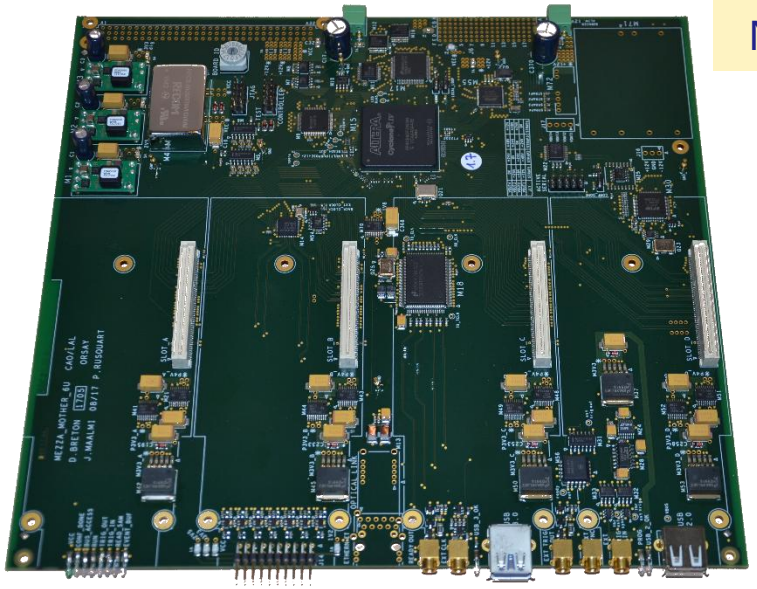
2014

x2

2016

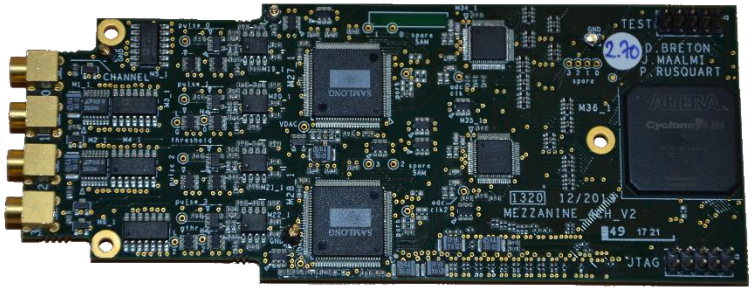
- **Autonomous plug and play desktops** with USB (both) and secured Gbit UDP interfaces (copper (8-channel) or optical link).
- Fully designed and cabled at LAL
- 8-channel module is the most demanded.
- In constant firmware and software evolution thanks to users' feedback.

New module development



New Motherboard

4-channel mezzanine



2017

x4

- A new motherboard has been developed
- It permits housing 4 mezzanines.
- It gives access to copper Gbit UDP
- But the external inputs (Trigger & Sync) are not recorded as waveforms.

System features (not exhaustive)

- Possibility to add an **individual DC offset** on each channel
- **Individual trigger discriminator** on each channel
- Integrated **hit rate counter** on each channel
- External & internal trigger + many smart modes for **coïncidence triggering (like any multiplicity up to 16 channels)**
- **2 extra memory channels** for « digital » signals on 16-channel board => **can be used as additional analog inputs**
- One individual **pulse generator** on each input
- **External clock** input for multi-board applications (8, 16 & 64-channel)
- Embedded **USB,** and **secured Gbit UDP** (8 & 64-channel)
- Possibility to upgrade the firmware via **USB**
- **Embedded feature extraction** (see next slide)

Feature extraction by firmware (1)

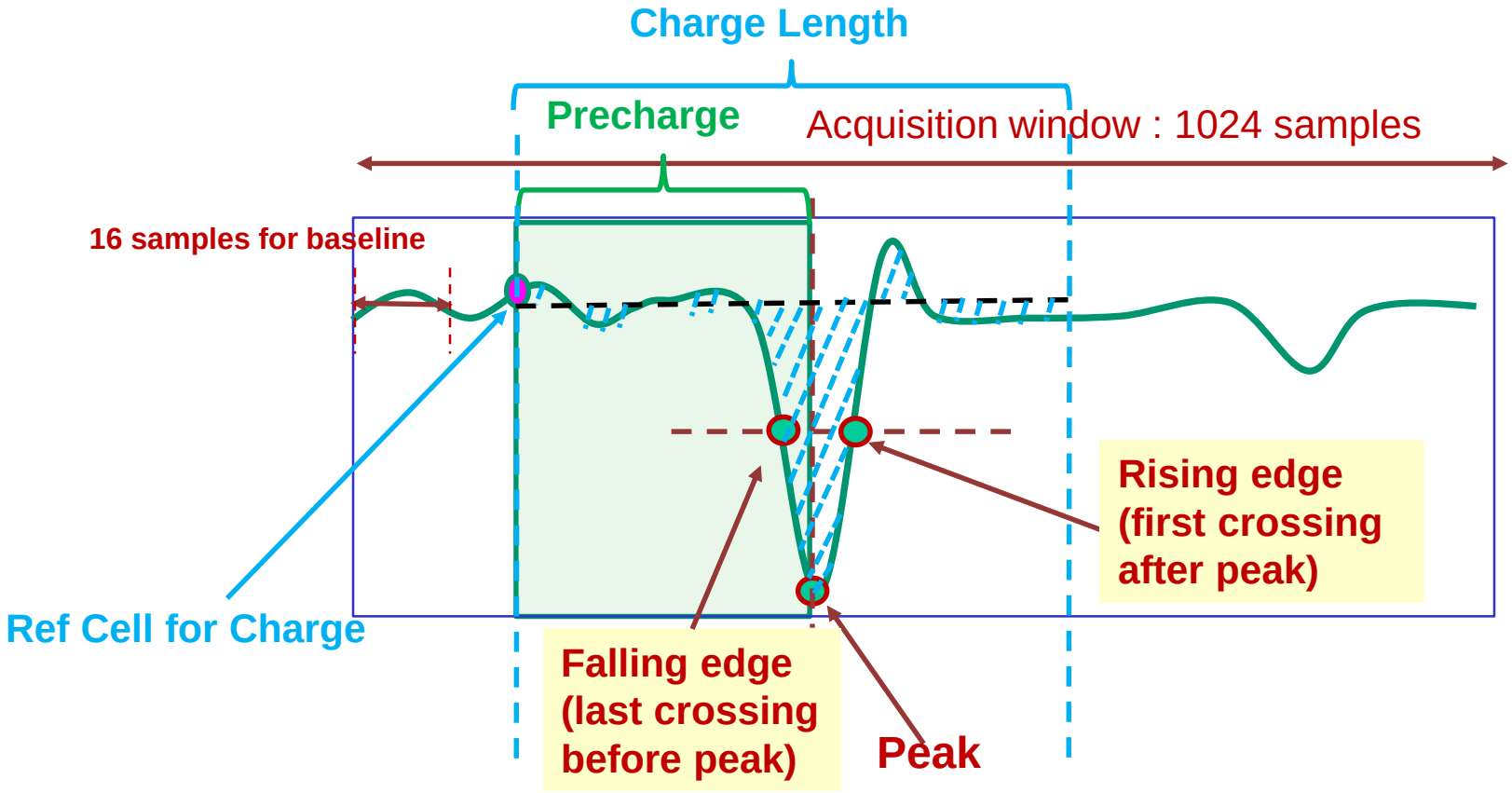
- **The very good level of performance of the SAMLONG chip without external correction permits implementing an effective on-the-fly calculation directly on the board (in its companion FPGA)** :

  This information is extracted from raw data directly coming from SAMLONG (after factory on-chip adjustment of the line offsets)

  - **Baseline** (16 bits)
  - **Peak** (16 bits)
  - **Peak time** (10 bits)
  - **Charge** (23 bits)
  - Real Digital CFD on Rising and Falling edge Time: (18 bits: bin of **1.22 ps**)
  - **Absolute Time**: given by the FPGA **40-bit TDC timestamp**

- When using the extracted parameters**, waveform transmission can be suppressed,** thus permitting **very high trigger rates (up to 30 kHz for 8 channels with reduced sampling depth)**

Feature extraction by firmware (2)



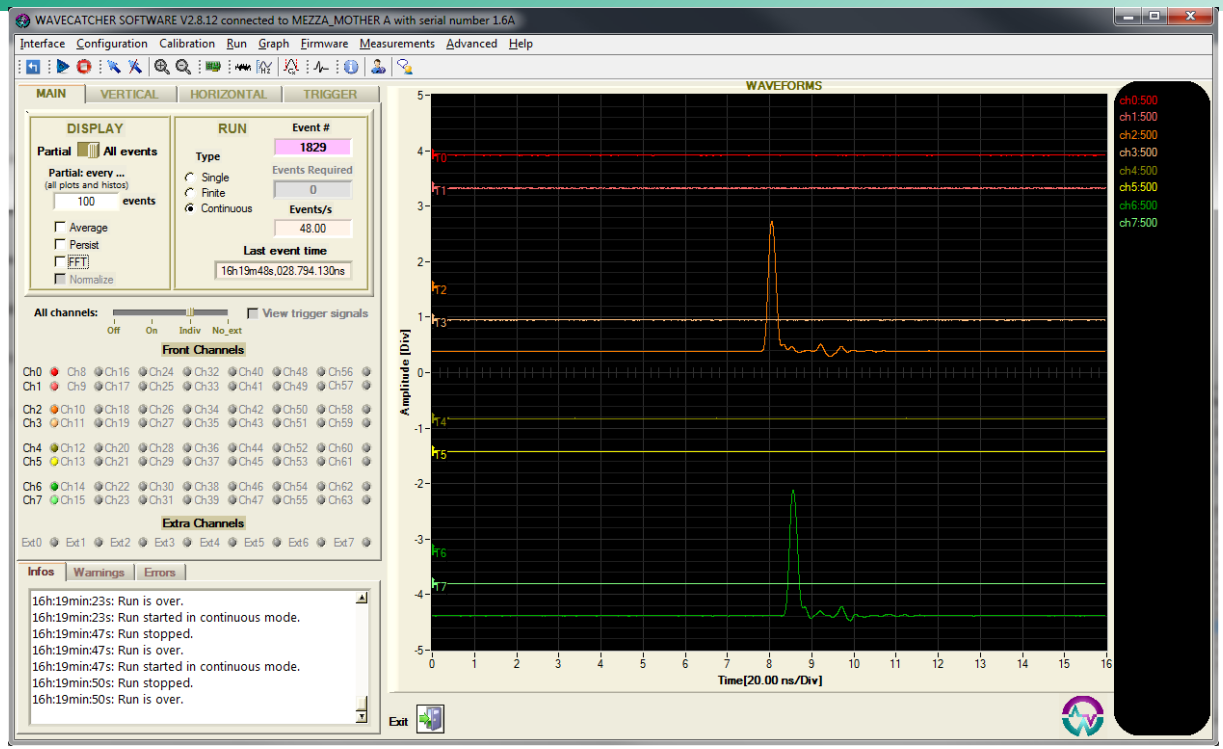
Programmable options :

- Peak polarity: Pos/Neg
- Forced/Extracted baseline
- CFD/Fixed Threshold
- CFD ratio (steps of 1/16)

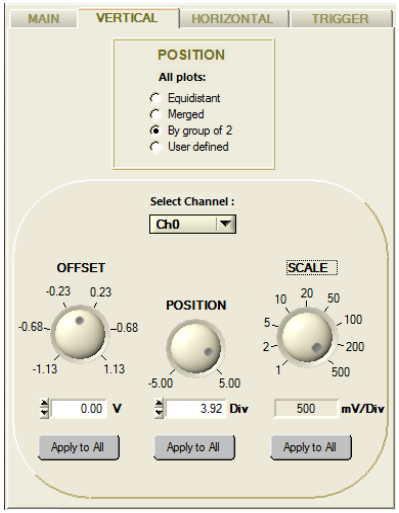
Charge Options :

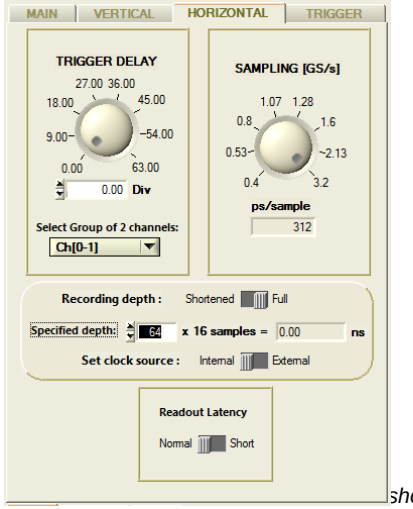
- Start from **Ref cell for Charge** or from **(Peak – Precharge)**
- PreCharge
- Ref Cell for Charge
- Charge Length

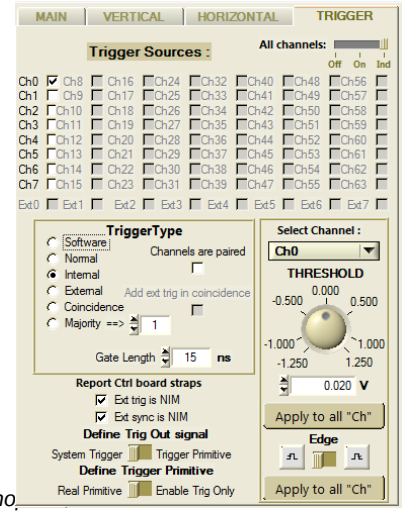
The WaveCatcher software



Main panel: oscilloscope like, but up to 64 channels !



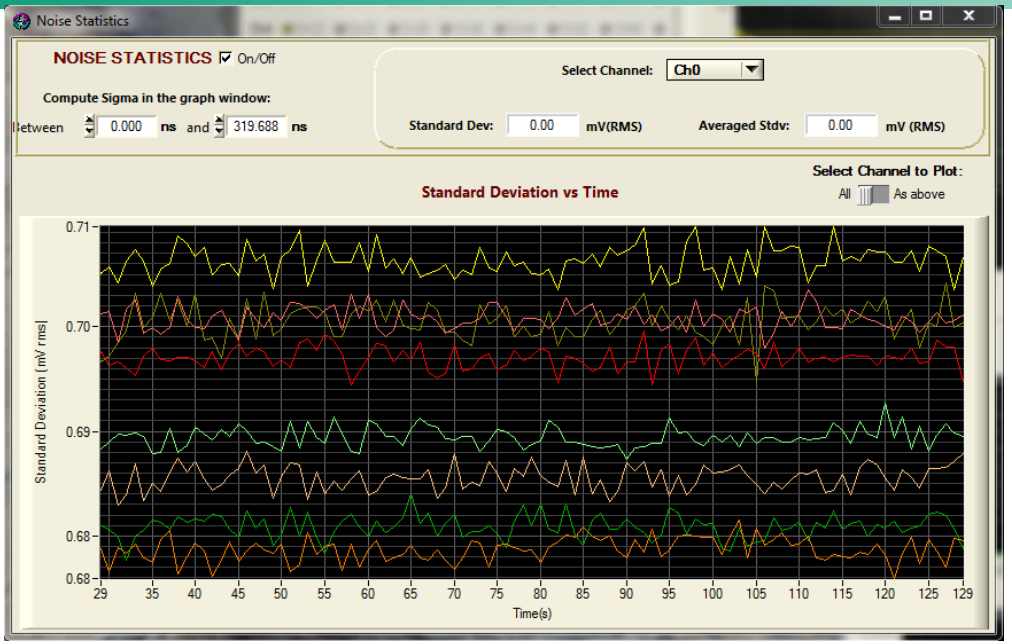




Vertical, Horizontal, and Trigger panels

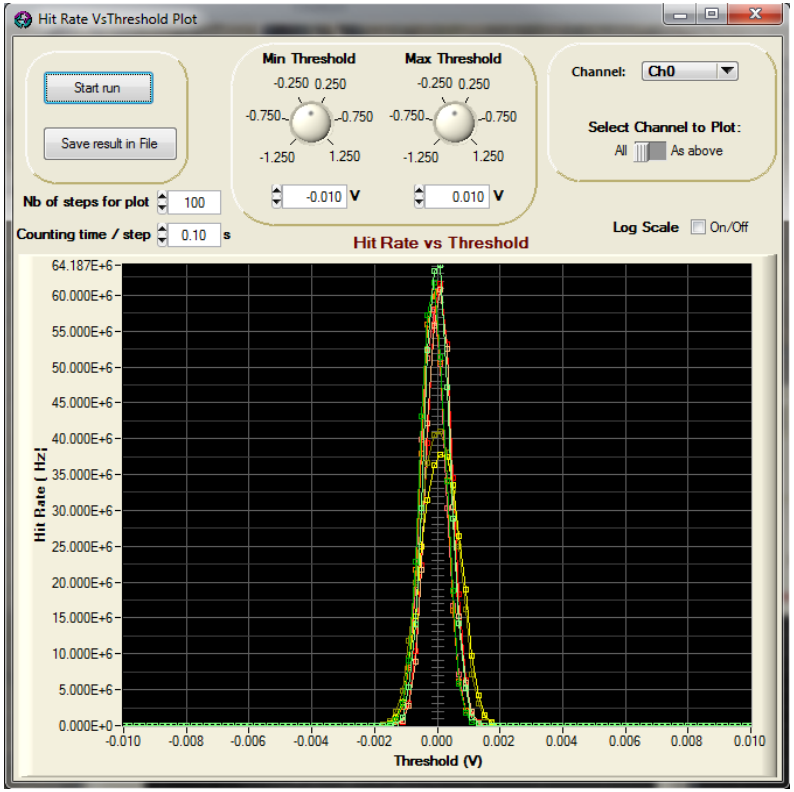
sho

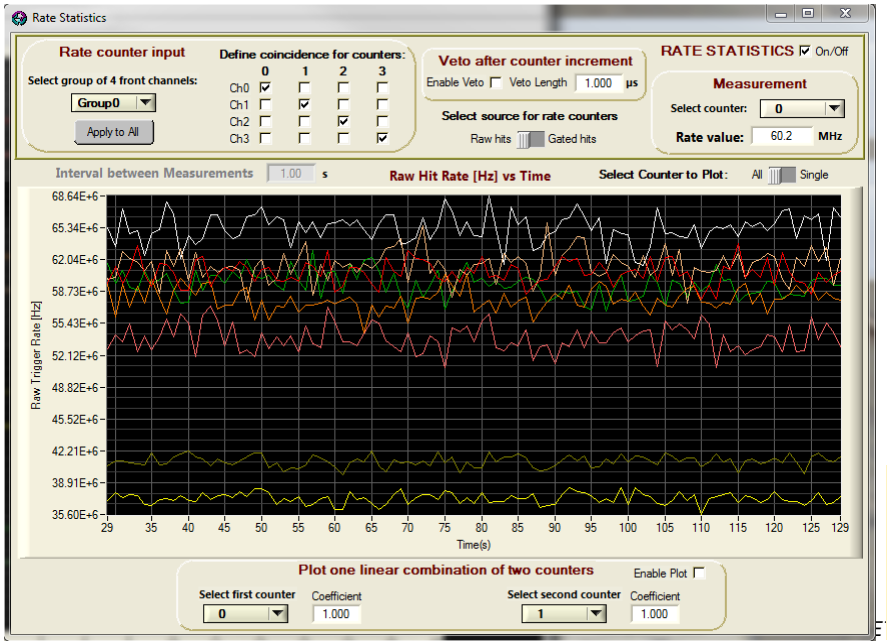
Real-time measurement display (1)



Noise statistics panel

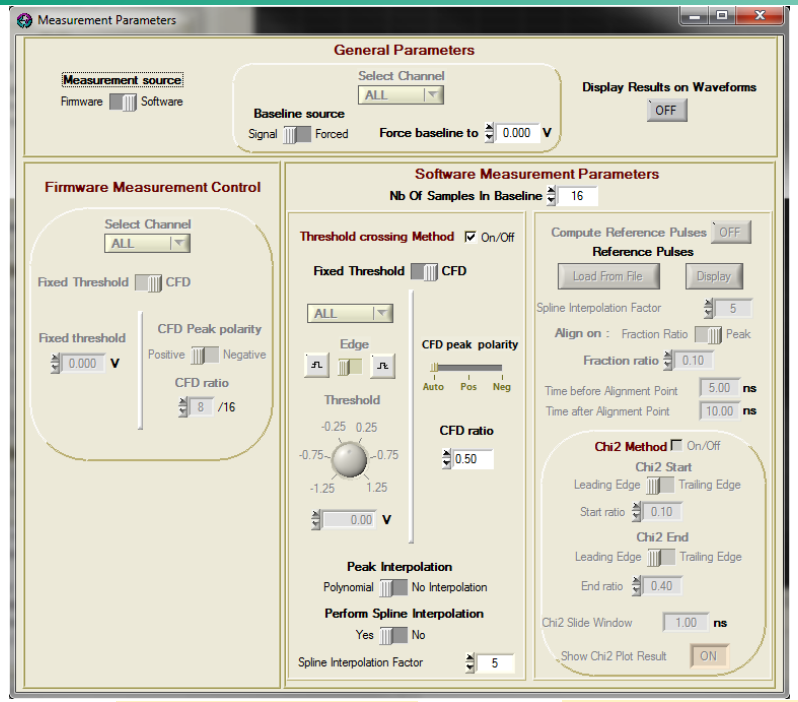
Rate vs Threshold plot





Rate statistics panel

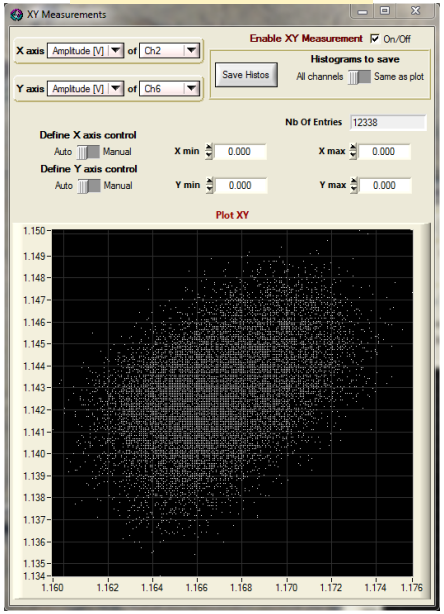
Real-time measurement display (2)



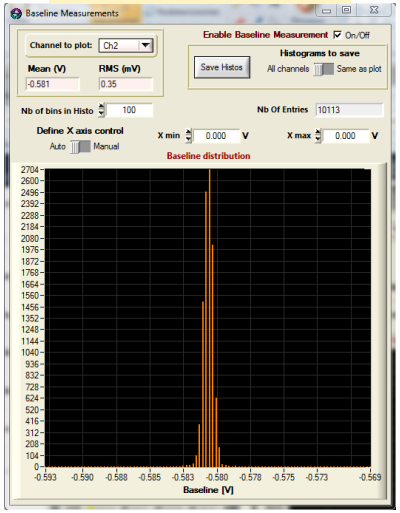
Measurement parameters panel

- Software also comprises a powerful time measurement panel (next slides)

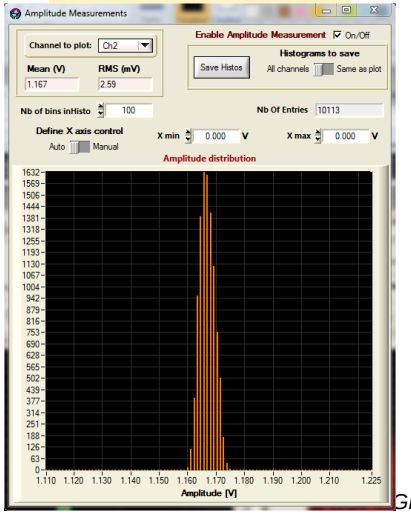
XY plot



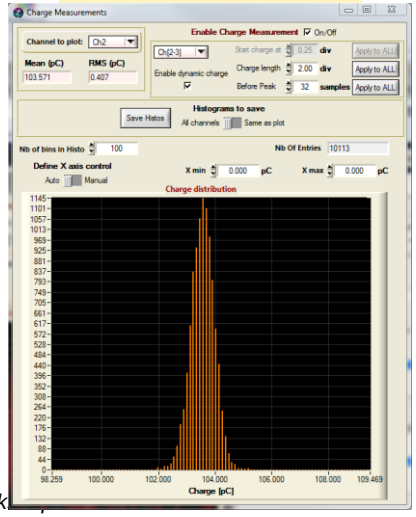
Baseline



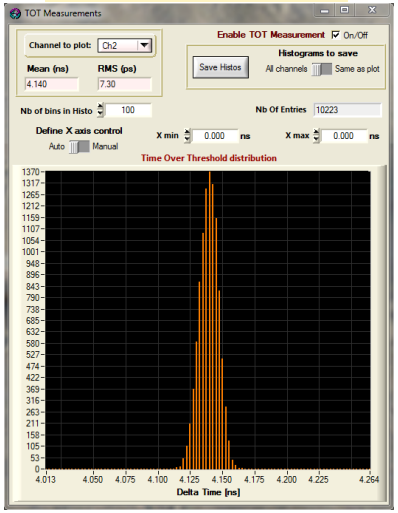
Amplitude



Charge



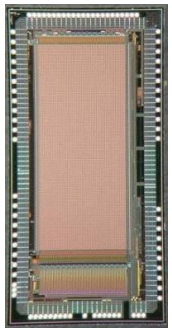
TOT



Jitter results with WaveCatchers

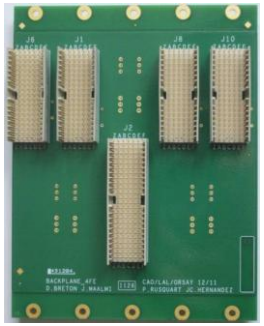
Delays are performed with cables to limit jitter. Trigger on signals.

- **Design difficulty here is the use of a backplane to distribute the clock.**
  - In the crate, the central control board is the source of the 200 MHz clock



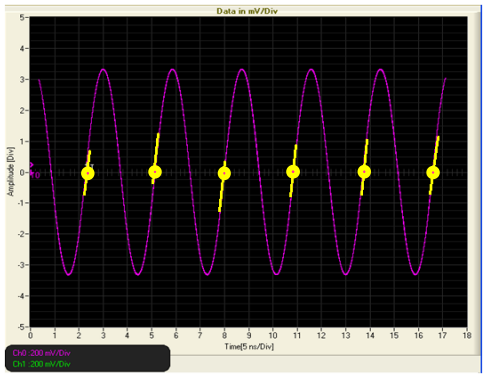
Ch0-Ch1

Ch0-Ch2 to Ch15

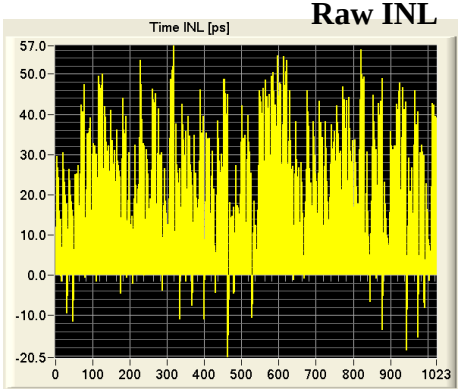


All other pairs

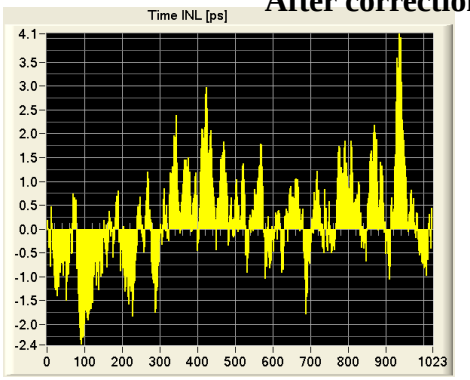
For time INL calibration, we use a method we introduced in 2009: zero-crossing segments of a sinewave (or equivalent) are considered like straight lines and their length give the time DNL, from which we can extract the INL…



Raw INL

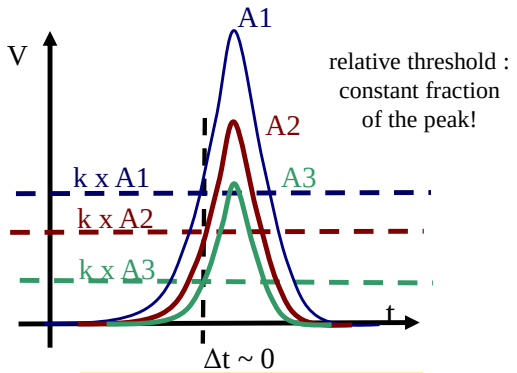


After correction



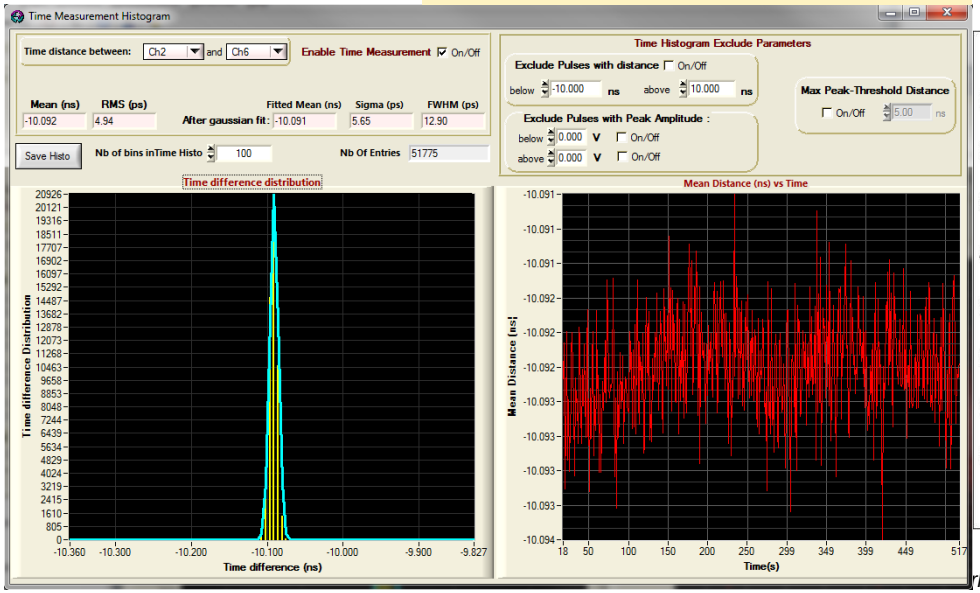
Jitter results with WaveCatchers

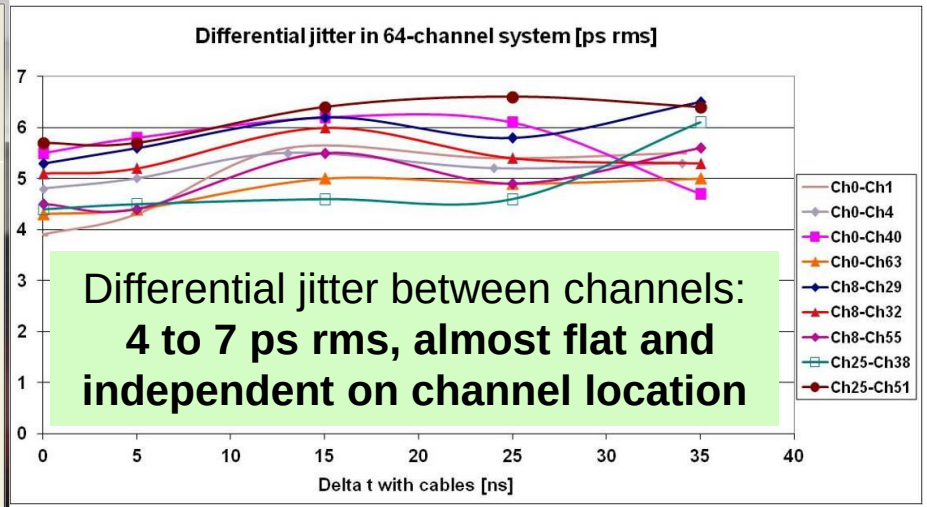
- Different methods can be used for time measurement:
  - Fixed threshold
  - Constant Fraction Discrimination (CFD)
  - Correlation…
- The most effective and still simple to implement after digitization is the CFD
  - It is embedded in firmware, software and libraries



Constant Fraction Discriminator

Time Measurement Panel





Differential jitter between channels:
4 to 7 ps rms, almost flat and independent on channel location

Usual applications

- **WaveCatcher modules** are widely used around the world. A lot of examples were presented at the WaveCatcher and SAMPIC workshop the 7th and 8th of February 2018 in Orsay => http://wpsist.lal.in2p3.fr/wasiw2018/

- Used for **all types of physics** with **all types of fast detectors**: PMTs, MCPPMTs, APDs, SiPMs, fast Silicon Detectors, Diamonds, MRPCs, GEMs, MicroMegas... Performances are equivalent to those with high-end oscilloscopes.

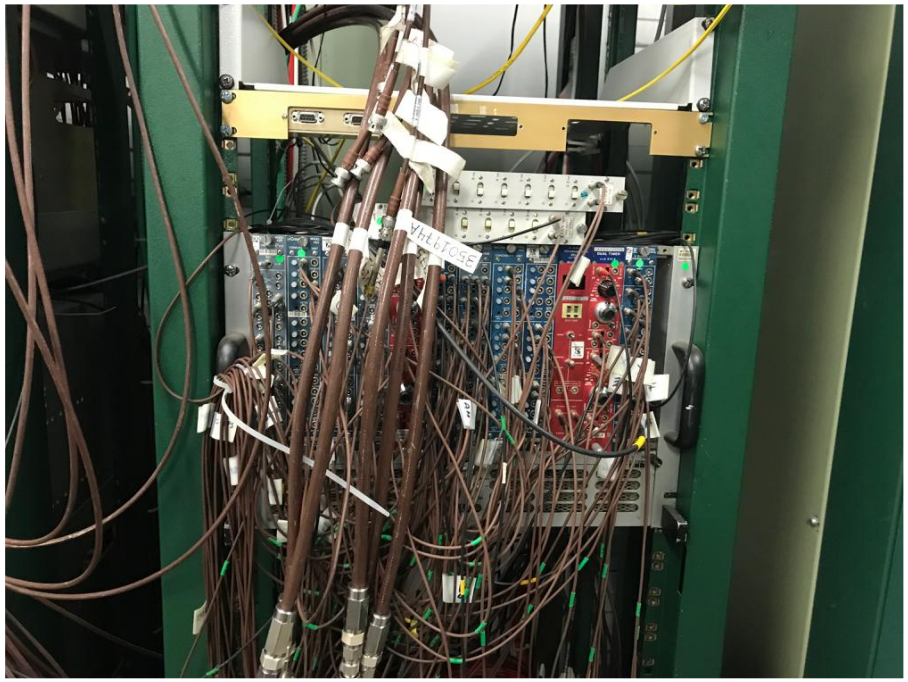
- The modules permit a **cheap replacement for these oscilloscopes** while offering more high resolution channels: the main potential limitation is the sampling depth of 1024 samples and the readout rate for the biggest systems

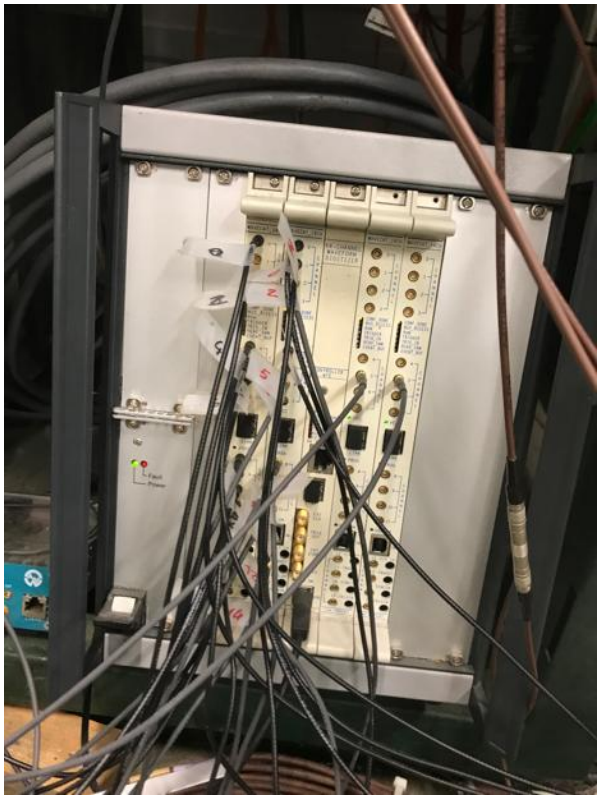
Used worldwide by many projects, universities, labs and companies:
BiPo, SUPERNEMO, Codalema, CORTO, UA9, PHIL, Eli_NP, ThomX, SHIP, PRAE, Roma Univ, Osaka Univ, Barcelona Univ, Dublin Univ, Geneva Univ, Zurich Univ, Berlin Univ, CEA/IRFU, CERN, INFN, PSI, BNL, Rochester, SLAC, LPSC, IPNO, IPHC, APC, CENBG, IMNC, Subatech, Nançay, GANIL, CEA/Cadarache, SENSL, GE, Hamamatsu, Solayl,…

Example of upgrade …

- The WaveCatcher modules can be used for replacing a wide range of VME boards, digitizers boards and spider-web-like NIM trigger logics

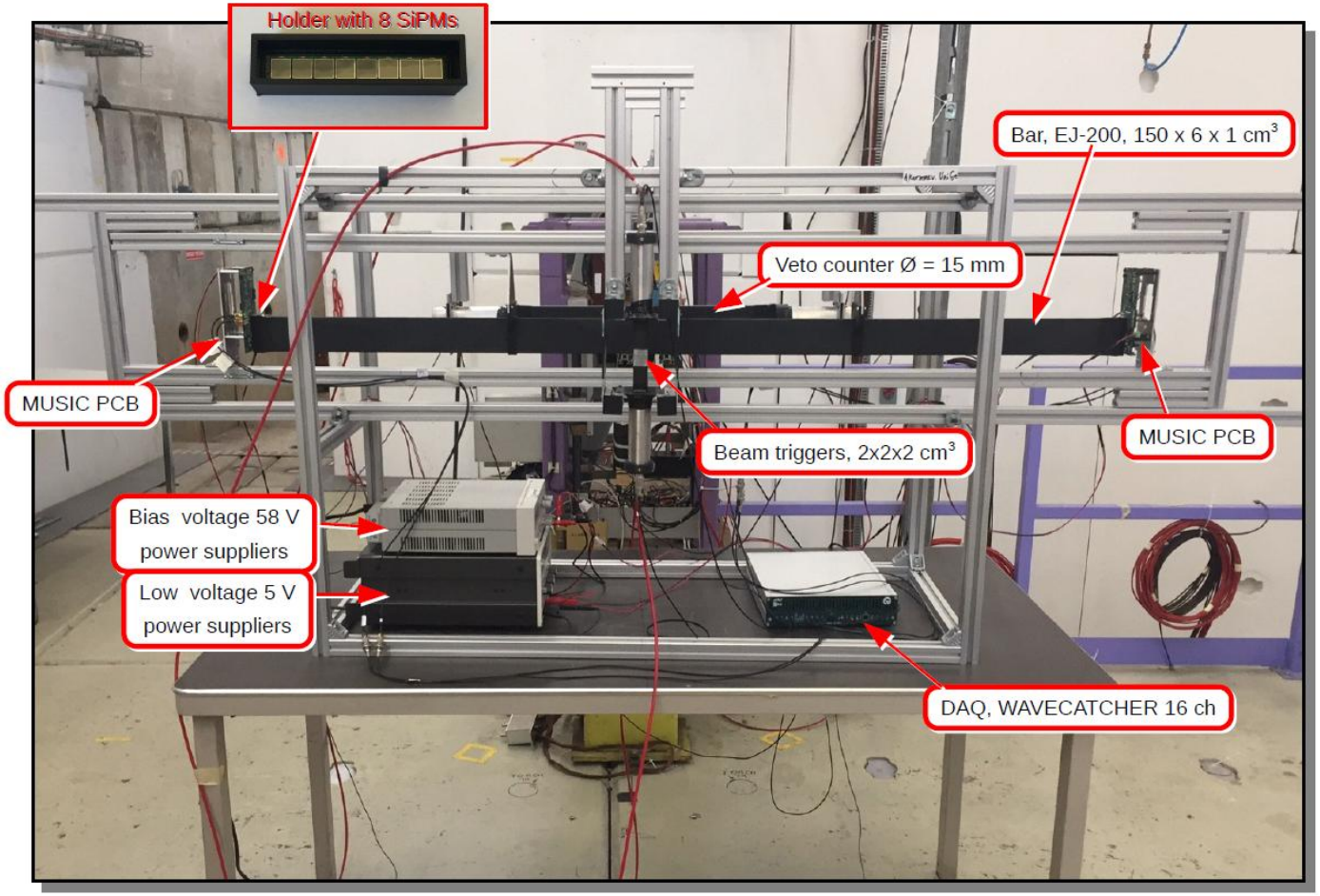
=> example of Beam Luminosity Monitor electronics on the SPS at CERN (UA9 experiment) where old logics included fixed threshold discrimination, analog and digital delays, coincidences (pairs of scintillator detectors, machine timing), VME scalers (40 channels), VME CPU computing rates and publishing to DIM





Small system: detector characterization

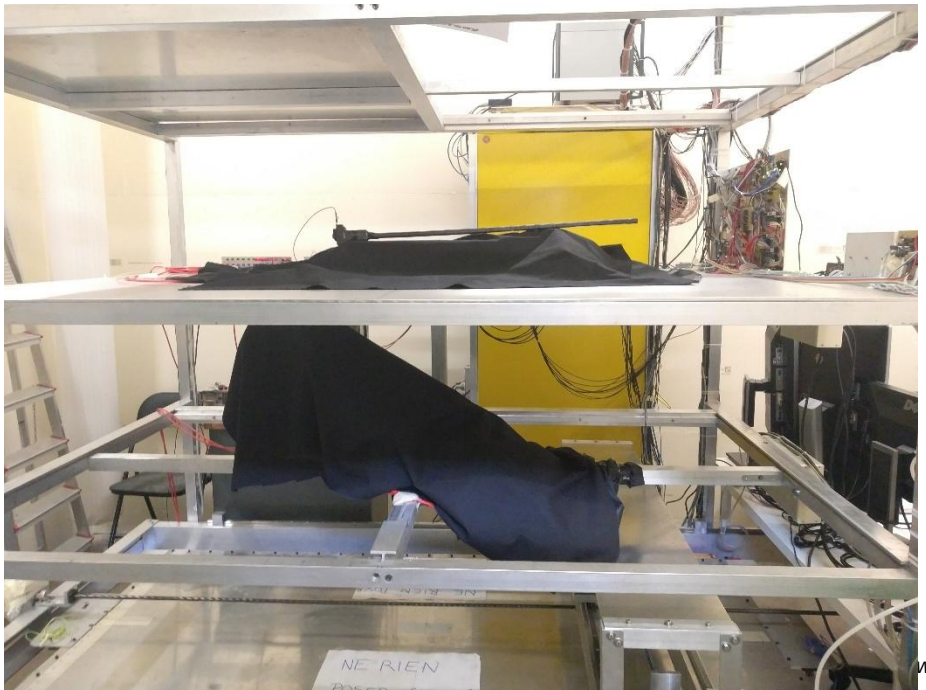
- Example of detector characterization at CERN: prototype of the SHIP timing detector => scintillator bar equipped with SiPMs and MUSIC ASICs (Barcelona Univ). The WaveCatcher module permits a fine and precise measurement of all signal parameters

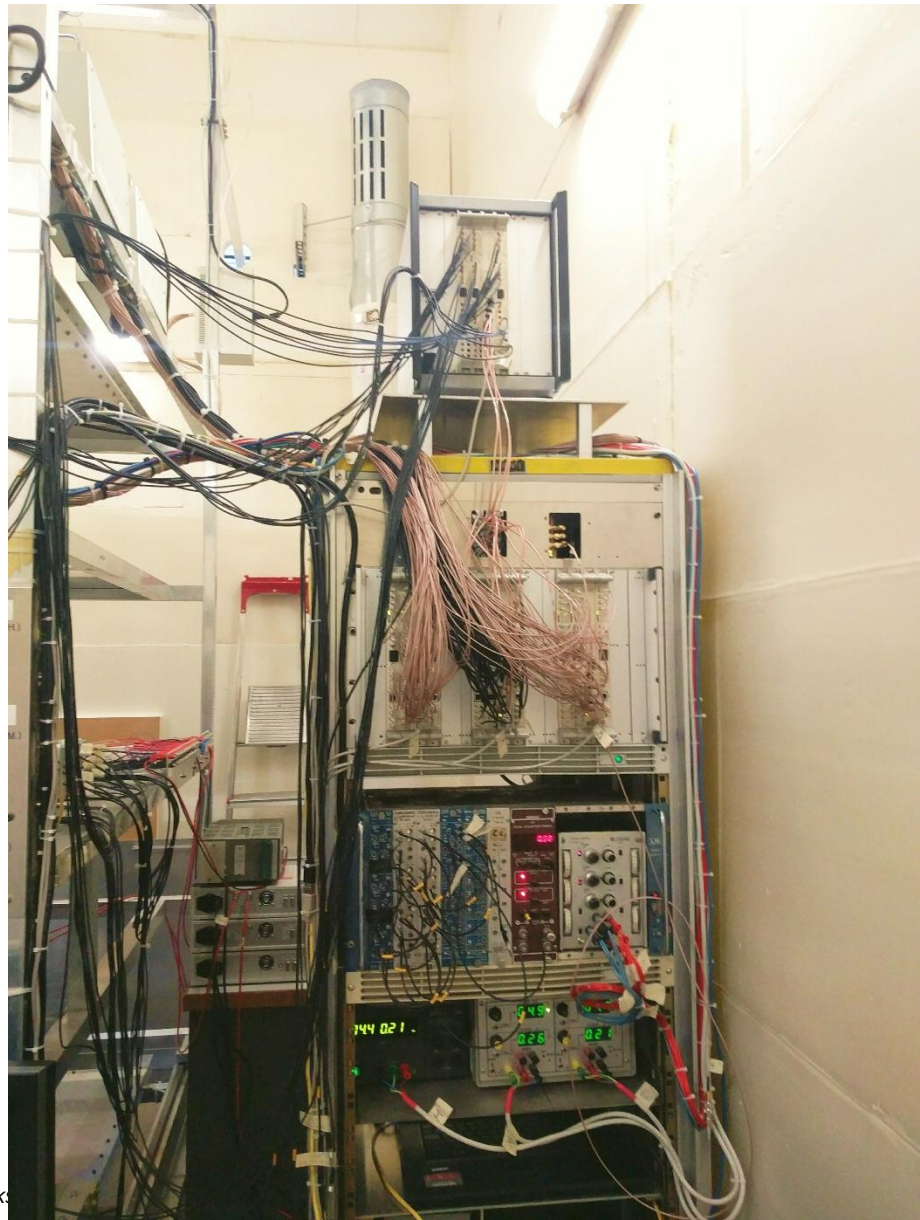


C.Betancourt et al, JINST 12(2017) P11023 [1709.08972]

Medium size system: CORTO electronics

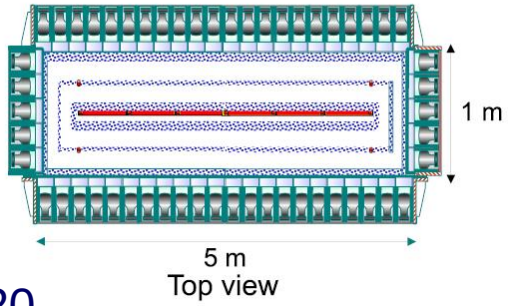
- CORTO is a cosmic ray telescope facility located at LAL in Orsay
- It is based on 3 MRPC chambers of 2 m² => 3 x 48 strip channels for muon tracking
- A 64-channel crate is dedicated to user's detector in test
- All 208 channels work synchronously thanks to a central trigger board

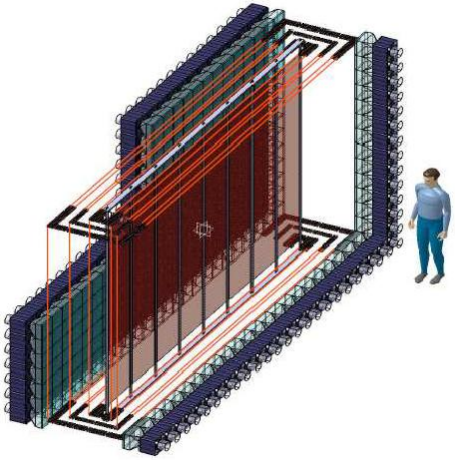




Larger system: SuperNemo electronics

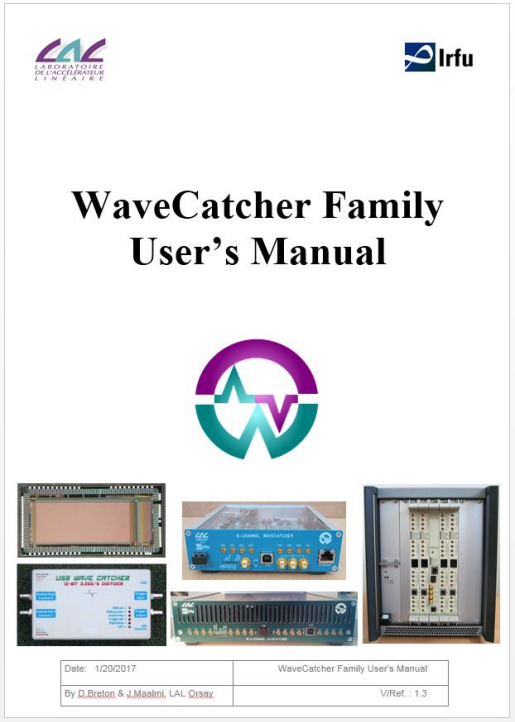
- SuperNemo is a detector dedicated to direct observation of rare double beta decays in LSM (Modane)
- It is based on a drift chamber and a calorimeter surrounding source foils
- 6U crates with custom backplane
- WaveCatcher boards are used for calorimeter readout => 3 crates with 320 channels each



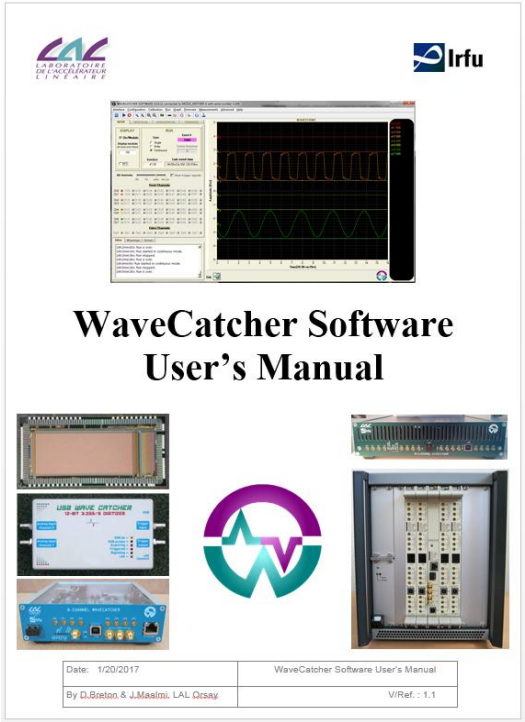


WaveCatcher documentation.

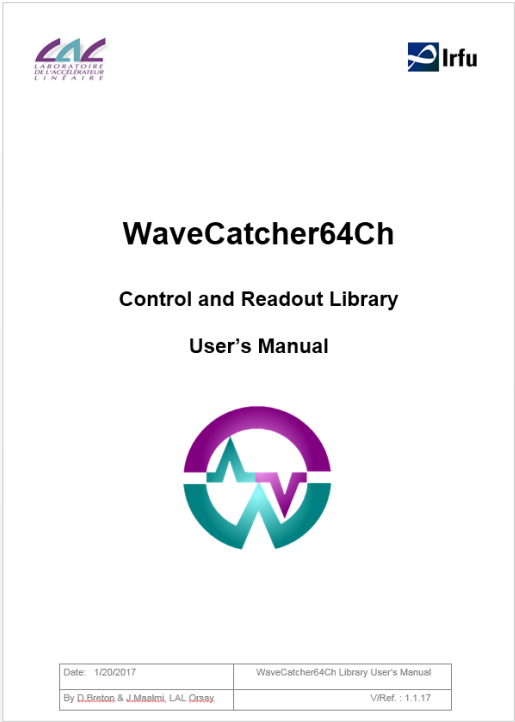
Hardware



Control & Readout software



C Library (Windows & Linux)



https://owncloud.lal.in2p3.fr/public.php?service=files&t=56e4a2c53a991cb08f73d03f1ce58ba2

CAEN products based on SAMLONG

- The WaveCatcher mezzanines are mounted on the CAEN motherboards
- Hardware was adapted, and a specific firmware has been developed to permit the interconnection between the motherboards and the mezzanines
- We participated to the integration of the modules in CAEN's high level software library
- Based on this library, a dedicated software has been written by Jihane: "CaenWaveCatcher", very close in spirit and aspect to our own software.

X743 family (based on SAMLONG)

Conclusion

- ✓ WaveCatchers are **powerful waveform digitizers**
  - ➢ Currently 12 bits => should rise to **14 bits** with the new version of SAMLONG

- ✓ With respect to ADCs**,** waveform sampling with **fast analog memories** permits **high precision measurements** at **lower cost**
  - ➢ Possible bothering drawbacks are sampling depth & readout dead-time

- ✓Chip developments depend on technology and drive system developments
  - ➢ **CMOS 0.35 µm** offers a good dynamic range (~ 2V => 12 to 14 bits) and permits a sampling rate up to 3.2 GS/s and a reduced dead time (125 µs) with a few ps rms resolution => **multipurpose systems: WaveCatchers**
  - ➢ **CMOS 0.18 µm** permits reaching very high rates (~ 10 GS/s) but dynamic range goes down to 1V => 10 bits with a very fast embedded ADC with a latency shorter than 1.5 µs, a few ps rms resolution and a very low power consumption => **SAMPIC**, optimized for **high rate & large scale time measurement** (like PET scanners)

WaveCatcher: Performance Summary

		Unit
SCA Technology	AMS CMOS 0.35µm	
SCA Number of channels	2	
SCA power consumption (max)	400 (3.3V supply)	mW
SCA noise	< 700	µV rms
SCA depth	1024	Cells
Sampling speed	0.4 to 3.2	GSPS
Bandwidth	500	MHz
Range (unipolar)	± 1.25	V
ADC resolution	12	bits
Total noise	< 700	µV rms
Dynamic range	~ 11.7	bits rms
Conversion time for full waveform (1024 samples)	125 (66 in fast mode)	µs
Readout capacity	30 (USB), > 100 (UDP)	Mbytes/s
Single Pulse Time precision before correction	~ 15	ps rms
Single Pulse Time precision after time INL correction	~ 3.5	ps rms