ID de Contribution: **14** Type: **Non spécifié**

FEANICS : A High Dynamic Range, High Energy resolution multi-detector integrated Circuit and its generic test bench

jeudi 11 octobre 2018 15:00 (30 minutes)

The GES project stands for "Generic Electronics System". It is aimed at developing a chain of generic electronics, comprising hardware, firmware and software modules to be assembled for the purpose of data acquisition on particle detectors. The modules include ASIC chips, electronics boards, and firmware or software components. The range of applications of the GES modules typically covers nuclear physics experiments, but can naturally extend beyond these to reach other domains such as particle physics, medical imaging and treatments, astrophysics, etc. Many aspects of the GES project can be considered as a follow-up or a spin-off of the GET project (General Electronics for Time Projection Chambers) as they might partly rely on GET hardware, firmware and software designs.
In order to fulfill the demanding requirements in terms of dynamic range and at the same time to ensure a high genericity, we have designed a new multi-channel ASIC called FEANICS (Front-End Adapative gaiN Integrated CircuitS) based on a floating-point Charge Sensitive Amplifier FPCSA architecture. This architecture is based on automatic gain switching during the rise time of the pulse. By default, the CSA is configured in a high gain mode. If the charge exceeds a specific value, the CSA automatically switches to a low gain value. Thanks to this basic principle, one can reach high dynamic range and high energy resolution.

The key parameters of the FEANICS chip are listed below:

• 16-channel ASIC in standard CMOS AMS 0.35µm technology.
• High input dynamic range (40pC max) with anti-saturation option for both polarities of input signal
• High resolution
• Optional shaper with tunable peaking time (60ns-10µs)
• Fully programmable ASIC thanks to embedded SPI protocol.
• Self trigger option
• 50 ohms output buffer with baseline adjustment for versatility (AGET-compliant)
• Auto-calibration, temperature probe, offset compensation circuit⋯

The FEANICS chip is tested and validated using a generic multi-asic board. The purpose of this board is to be able to test different kinds of ASICs with little or no modifications of the firmware and software used to readout the chip.
The multi-asic board and the ASIC card are connected to a digital subsystem based on a COTS "Picozed Zynq"module and its evaluation motherboard. The Zynq FPGA will implement all the firmware needed to control, configure and readout the multi-asic board and the Zynq double core processor will run the acquisition software over a an embedded Linux operating system. Firmware module are developed with generic features allowing them to be reused within different contexts such as different kinds of ASICs.

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