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ilC



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Protections

Simulations

Proposed test board

Conclusion

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Introduction

Sparks have many differents origins:

- Corona effect spark (detector imperfection or dirt) ;
- Raether limit (detector geometry and set-up condition) ;
- High ionisation may cause divergent avalanche by photon feedback effect.

During this breakdown, the gaz is so highly ionising that an arc is created between mesh and anode. As frond-end electronics are connected to the anodes, the readout chip may be destroyed !

Orders of magnitude

 C_{mesh} =8 fF/cm² If S_{mesh} =1536 cm² (32×48), then C_{mesh} =12 nF HV=450 V $Q = C_{mesh} \times HV$ =5.5 µC $E = \frac{1}{2} \times C_{mesh} \times HV^2$ =1.2 mJ (standard HBM ESD protection: 200 µJ)

Energy is similar, but the current in spark discharges is much higher due to lack of serial resistance:





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Protections

A lot of schematics to protect form sparks! Two examples:



We must keep in mind: $C_{prot} \gg C_{det}$ (keep signal), but $C_{prot} \ll C_{mesh}$ (to protect).

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We must integrate spark protections !

- ILC DHCAL will have from 30 to 50 000 000 channels: no external components allowed!
- Easier fabrication of PCB mask: cost \;
- Easier PCB (?) cost ∖;
- Increased reliability

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We have still to wonder and propose solutions !

- Resistive oxyde on PCB pads ?
- Resistor and capacaitor burried inside PCB, diodes inside ASIC ?
- Only a serial resistor and diodes inside ASIC ?

BUT:

Difficult to simulate (which capacitor value, which inductance in net, does the mesh dischage entirely...);

We have to perform bench tests to compare protection circuits !



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Simulations

Example (1)

COMPASS (gassiplex) protection detailed schematic (C_{prot} =470 pF):



COMPASS (gassiplex) protection simulation:



No arc cut-out in simulation: better model needed !

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Simulations



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Proposed test board

Concept

Idea adapted from E. Noschis *et al.* in *Protection circuit for the T2 readout electronics of the TOTEM experiment*:



Must list different protections to test !

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Proposed test board



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- *Rendez-vous* with Rui thursday 26/02 to have feedback on embedded capacitors/resistors ;
- We must decide which protections do we want to test ;
- Need agreement to start board design (S. Cap).

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