环形正负电子对撞机
Circular Electron Positron Collider

中国科学院高能物理研究所
Institute of High Energy Physics
Chinese Academy of Sciences

華中師範大學

山东大学
SHANDONG UNIVERSITY

IPHC
Institut Pluridisciplinaire Hubert CURIEN STRASBOURG

Electron Collider Oriented PIxelated Cmos Sensor development

WANG Meng

On behalf of the CEPC VTX study group

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Outline:

- *Requirements*

- *R&D activities*

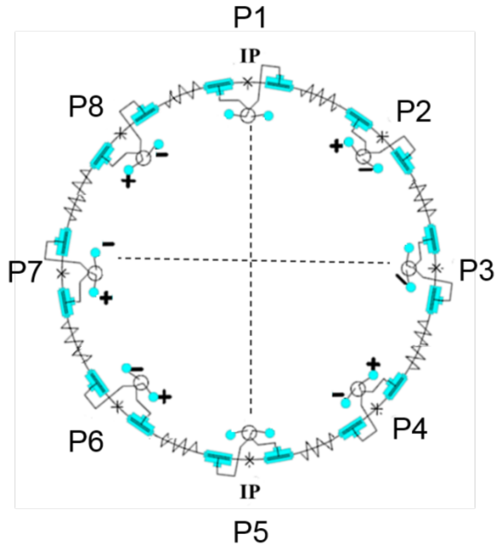
- *Future plan and outlook*

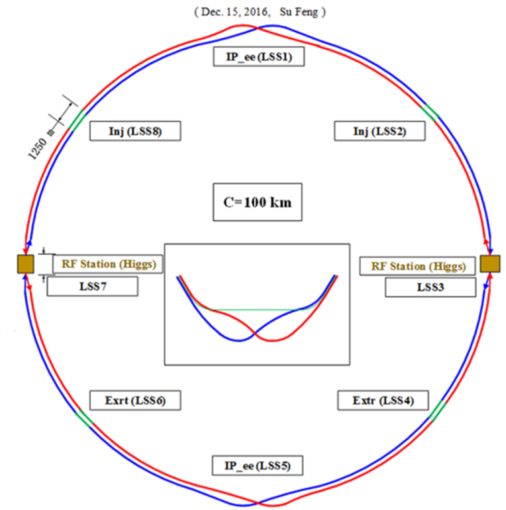
- *Summary*

CEPC and Its Beam Timing

Circular e^+e^- Higgs (Z) factory **two detectors, 1M ZH events in 10yrs**

$E_{cm} \approx 240$GeV, luminosity ~2×10^{34} $cm^{-2}s^{-1}$, (1×10^{34} $cm^{-2}s^{-1}$ at the Z-pole)





Single Ring - 54Km

- **Baseline design in pre-CDR**
- Bunch number 50
- Colliding every 3.6μs, continuously

→Power pulsing not applicable

Fully Partial Double Ring - 100Km

- **Baseline design in CDR**
- Bunch number 286 (half ring)
- Bunch spacing 0.537μs

Detector Requirements

- Efficient tagging of heavy quarks (b/c) and τ leptons

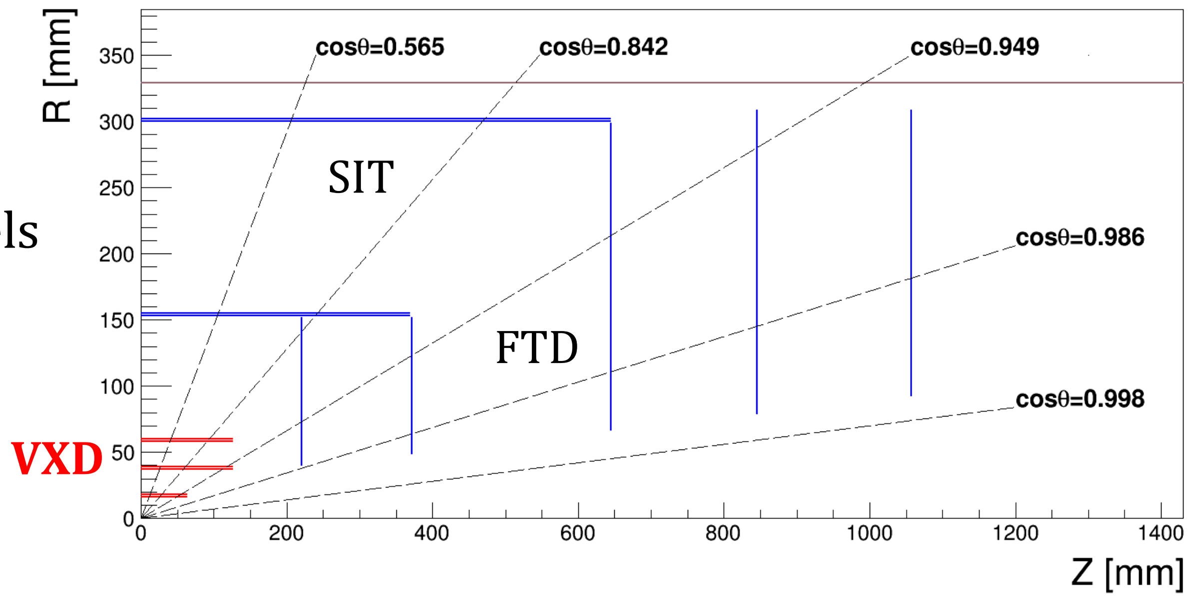
⟶ impact parameter resolution

$$\sigma_{r\phi} = 5 \oplus \frac{10}{p(GeV)\sin^{3/2}\theta} (\mu m)$$

- Detector system requirements:
  - σ_{SP} near the IP: *<3 μm* ⟶ ~16μm pixel pitch
  - material budget: *≤ 0.15%X_0/layer* ⟶ power consumption < 50mW/cm^2, if air cooling used
  - first layer located at a radius: *~1.6 cm*
  - pixel occupancy: *≤ 1 %* ⟶ ~ μs level readout

Target: fine pitch, low power, fast pixel sensor + light structure

Baseline Detector Layout



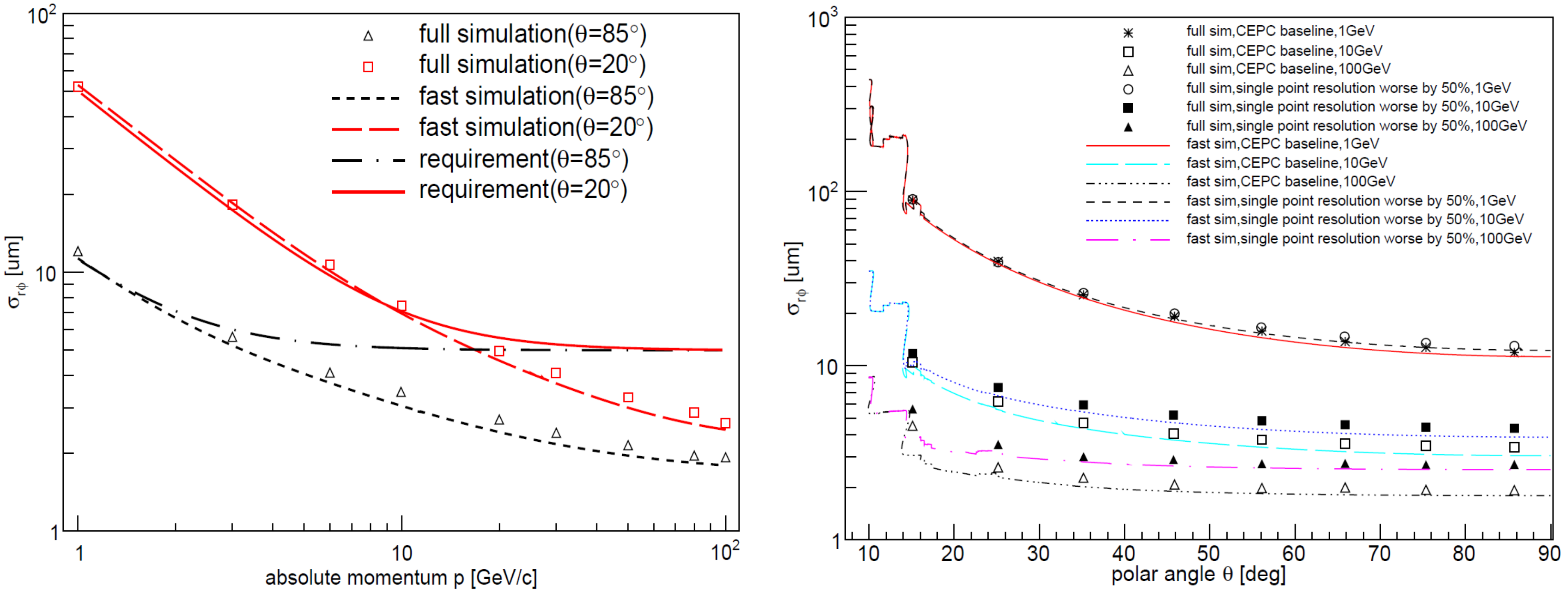
VXD:

- ILD like layout
- 3 layers of double-sided pixels
- σ_{SP}=2.8μm, inner most layer
- Polar angle θ~15 degrees

VXD parameters

	R (mm)	|z| (mm)	|cos θ|	σ_{sp} (μm)	Readout time (μs)
Layer 1	16	62.5	0.97	2.8	20
Layer 2	18	62.5	0.96	6	1-10
Layer 3	37	125.0	0.96	4	20
Layer 4	39	125.0	0.95	4	20
Layer 5	58	125.0	0.91	4	20
Layer 6	60	125.0	0.90	4	20

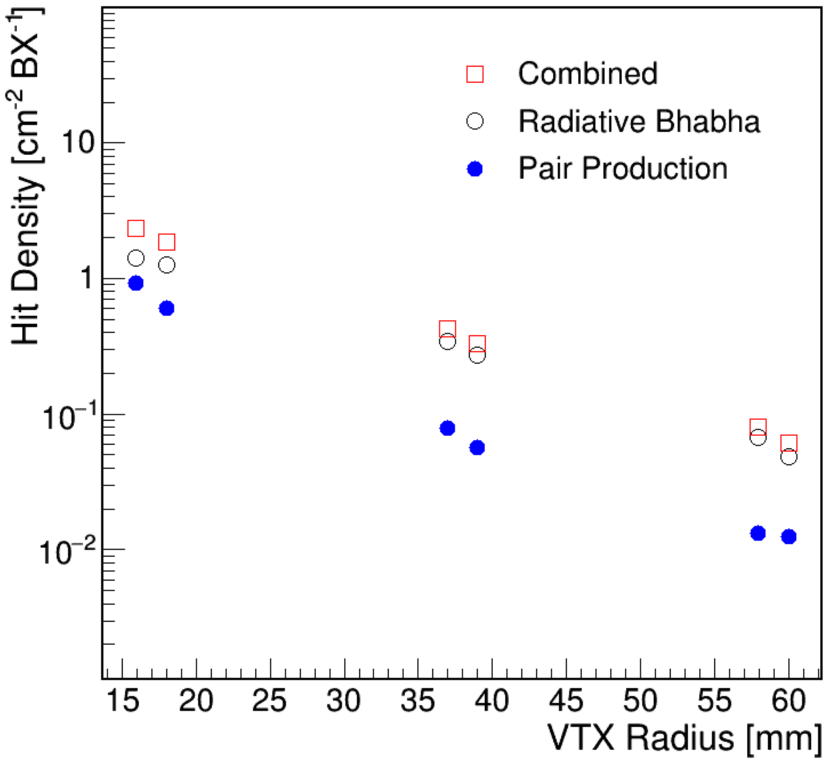
Performance Studies



Result: could meet the physics requirement with the baseline design

Beam-Induced Backgrounds

- Various sources of backgrounds studied with Monte Carlo simulation :
  - Beamstrahlung
  - Lost Particles
  - Synchrotron Radiation



- **Hit density** ~2.5 hit cm^{-2} BX^{-1}
  → detector occupancy: <1%
  by estimating tolerable hit density, with a safety factor of 10 included

- **Radiation level**
  - TID ~2.5 MRad / year
  - NIEL ~10^{12} 1MeV n_{eq} / (cm^2 year)

  (safety factor: 10)

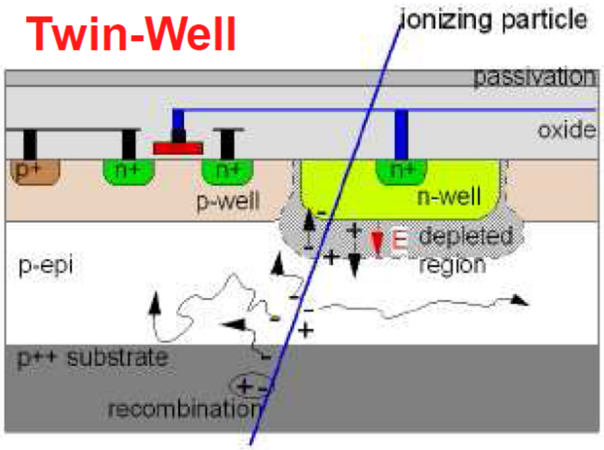
R&D activities

Initial sensor R&D targeting on

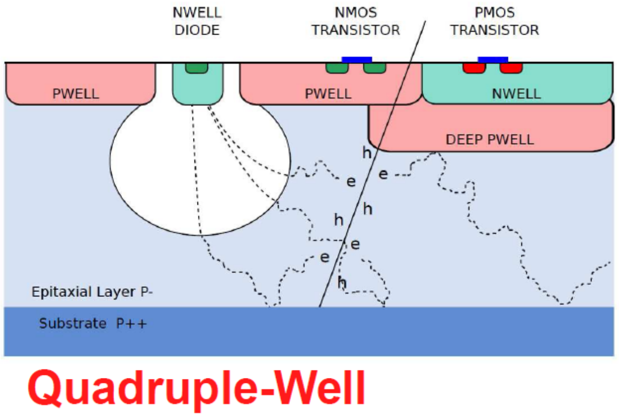
- *Pixel single point resolution <3- 5μm*
- *Power consumption at the current level <100mW/cm^2*
- *Integration time 10-100μs*

- CMOS pixel sensor (CPS)-funded by NSFC, MOST and IHEP
  TowerJazz CIS 0.18 μm process

CMOS Pixel Sensors: Main Features



- Prominent features of CMOS pixel sensors:
  - High granularity ➔ excellent (micronic) spatial resolution
  - Signal generated in (very) thin (15 - 40 µm) epitaxial layer
    - ➔ Resistivity may be >> 1 k Ω • cm
  - Signal processing µ-circuits integrated on sensor substrate
    - ➔ Impact on downstream electronics and syst. integration (➔ cost)



- CMOS pixel sensor technology has the highest potential:
  - R&D largely consists in trying to exploit potential at best with accessible industrial processes
    - Manufacturing param. not optimised for particle detection: wafer/EPI characteristics, feature size, N(ML), ...

- Read-out architectures :
  - 1st generation : rolling shutter with analog read-out (twin-well)
  - 2nd generation : rolling shutter with // read-out & end-of-column discrimination (twin-well)
  - 3rd generation : data driven read-out with in-pixel discrimination (synchronous/asynchronous)

Motivation for Using CMOS Pixel Sensors

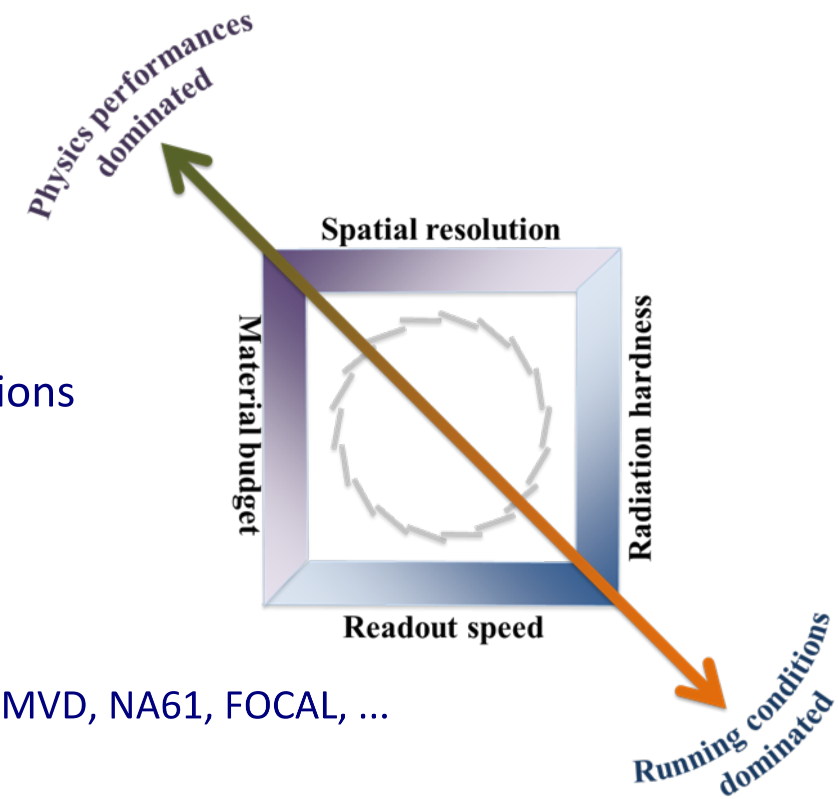
- CPS development triggered by need of very high granularity & low material budget

- Applications exhibit(ed) much milder running conditions than pp/LHC

➔ Relaxed speed & radiation tolerance specifications

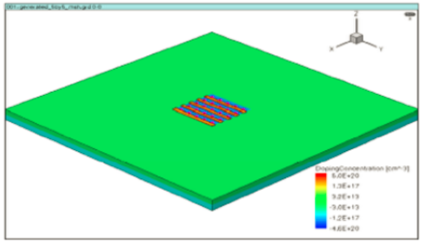
- Increasing panel of existing, foreseen or potential application domains :
  - Heavy Ion Collisions : STAR-PXL, ALICE-ITS, CBM-MVD, NA61, FOCAL, ...
  - $e^+ e^-$ collisions : ILC, BES-3, CEPC ...
  - Non-collider experiments : FIRST, NA63, Mu3e, PANDA, ...
  - High precision beam telescopes adapted to medium/low energy electron beams:
    - few µm resolution achievable on DUT with EUDET-BT (DESY), BTF-BT (Frascati), ...
  - **RECENTLY: high rate pp collisions ➔ addressing the pb of speed and radiation hardness**

Quadrature of the Vertex Detector

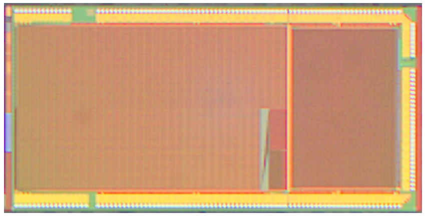


CMOS Pixel Sensor R&D Activities

- **Sensor design & TCAD simulation**
  - Different sensor diode geometries, epitaxial-layer properties and radiation damage



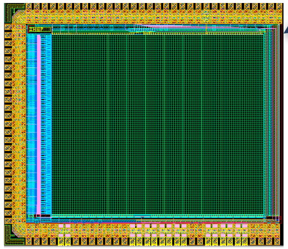
- **First submission in Nov. 2015**
  - Exploratory prototype, analog pixel, rolling shutter readout mode
  - Sensor optimization and radiation tolerance study
  - sensing node AC-coupled to increase biased voltage

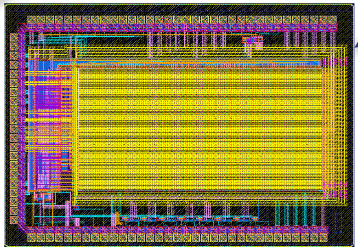


- **Second submission in May 2017**
  - Tow prototypes with digital pixels (in-pixel discriminator)
  - Tow different readout schemes: rolling shutter & asynchronous

Design goals

Spatial resolution	$5\ \mu m$
Integration time	$< 10\ \mu s$
Power consumption	$< 80 mW/cm^2$

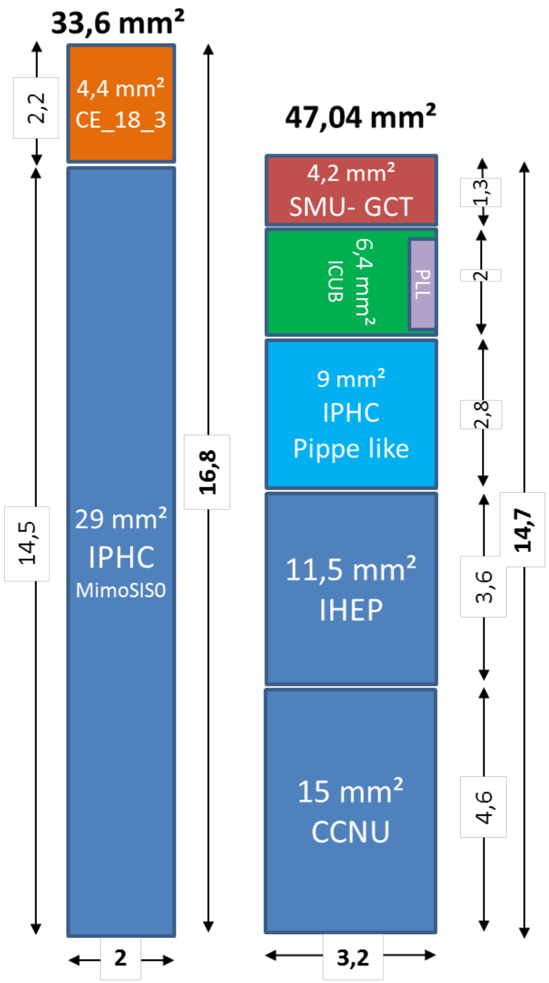




chip returned from the foundry

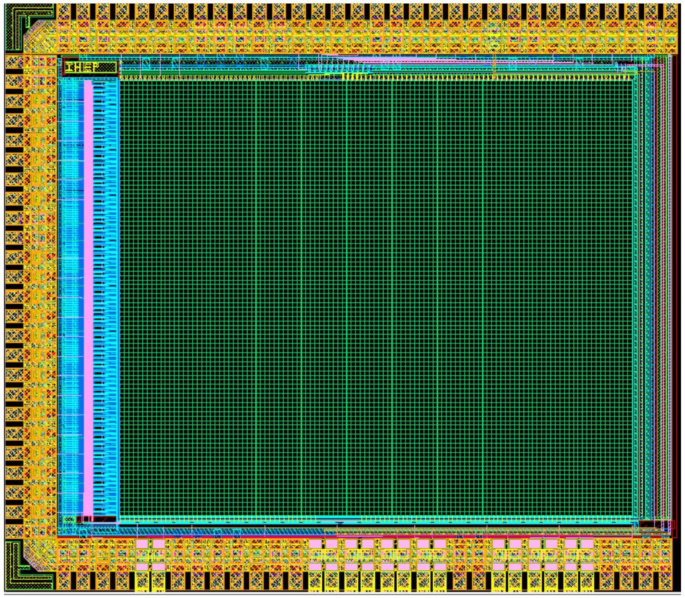
Common Submission

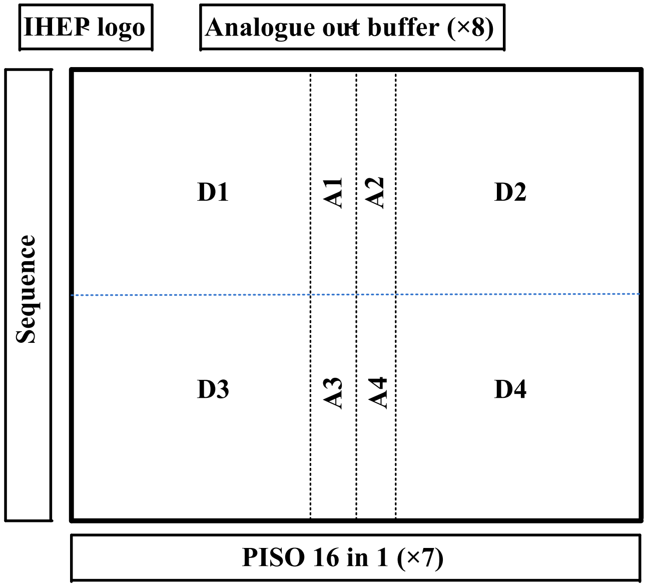
- Bring together efforts and funding resources
- 2 GDS submitted to TowerJazz with total 80 mm² surface
- 8 circuits from 5 institutions



- CE-18-3 (IPHC): Pixel matrix with short peaking time and for studies of tolerance to high ionising radiation
- Mimosis0 (IPHC): Pixel matrix with sensor real height to study data driven readout mechanism and radiation tolerance (CMB)
- GCT (SMU, US): 3 Gbps serial link transmission for CPS
- PLL (IPHC): clock reference for CPS
- ICUB (Unistra): SPAD – external contribution
- PIPPE (IPHC): Pixel matrix for low energy X rays detection
- IHEP: rolling-shutter mode
- CCNU: asynchronous mode

2nd CPS Submission: Rolling-shutter Mode





Two different pixel versions:

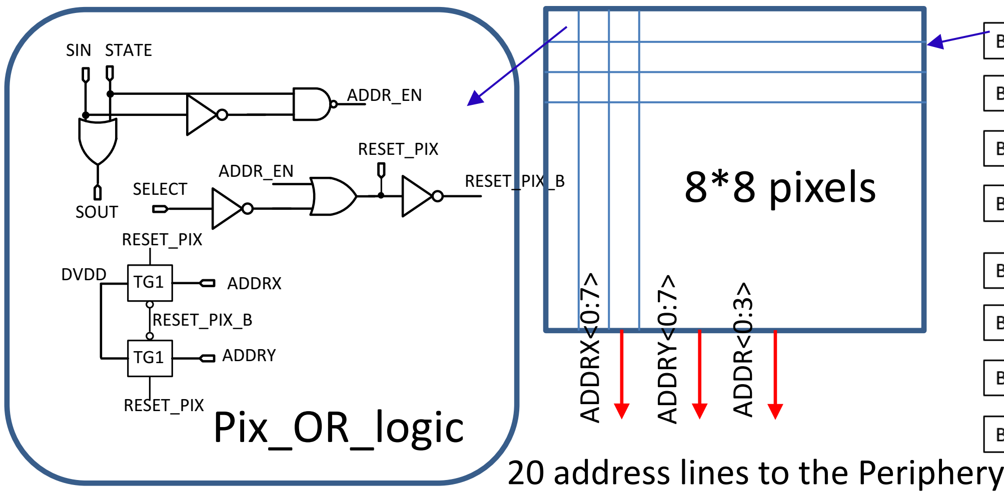
- Pixel size: 22μm×22μm
  → 65% of ASTRAL chip
- Same amount of transistors;
- Offset cancellation technique;
- Version 2 has higher signal gain, but suffers "more" from "Latch" input voltage distortion.

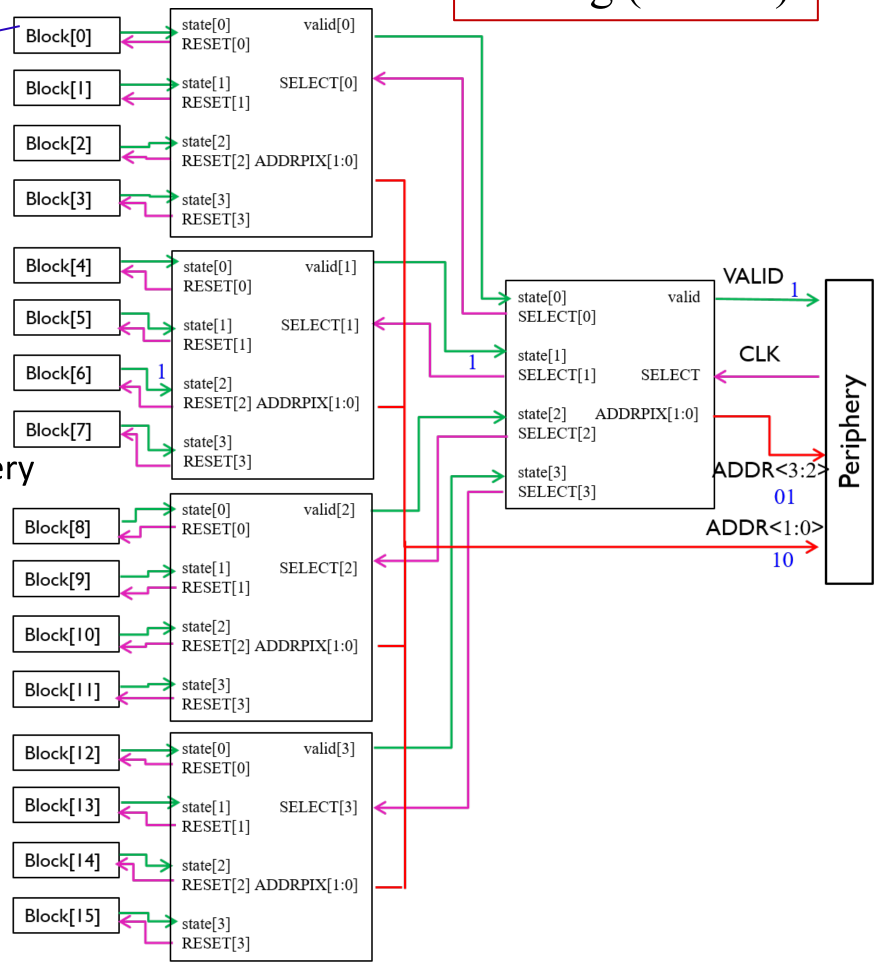
Chip features:

- 3×3.3 mm²
- 96×112 pixels with 8 sub-matrix
- Processing speed: 11.2μs/frame with 100 ns/row
- Output data speed: 160 MHz
- Power: 3.7μA/pixel (14.4 mW/cm² @pixel matrix)

2nd CPS Submission: Asynchronous Mode

P.Yang (CCNU)





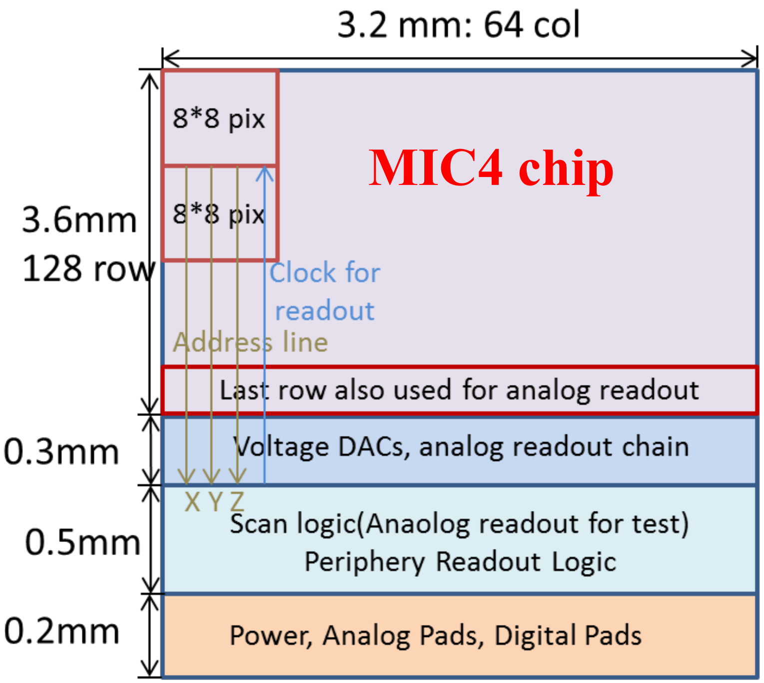
Matrix readout architecture:

- **AERD (Address-Encoder and Reset-Decoder)** many connection lines occupy larger area than the logic circuit itself
- **OR gate chain:** speed is limited with the number of the chain pixels
- **Combine these two solutions:** 64 pixels as a group using OR gate chain, groups using AERD structure to readout

2nd CPS Submission: Asynchronous Mode

front-end I: Same structure as ALPIDE chip

- ENC: 8 e^-
- Power cons.: 61 nA/pixel
- Threshold: 140 e^-
- Peaking time < 1 us
- Pulse duration < 3 µs



front-end II: CSA based front-end circuit

- Pixel size: 25 × 25 μm^2
- ENC: 24 e^-
- Power cons.: 50 nW/pixel (8 mW/cm^2 @pixel matrix)
- Threshold: 170 e^-
- Peaking time < 500 ns @ Qin < 1.5 ke^-
- Pulse duration < 9.4 µs @ Qin < 1.5 ke^-

- 3.2 × 3.7 mm^2
- 128 × 64 pixels
- Integration time: < 5 µs/10 µs
- Power consumption: < 80 mW/cm^2
- Chip periphery
  - Band gap
  - Voltage DAC
  - Current DAC
  - Matrix configuration
  - LVDS
  - Custom designed PADs

Future Plan on R&D

- laboratory and test-beam characterizations
- Coordination on sensor design team
- Novel readout scheme
- Radiation hardness
- Large area pixel array design
- Time stamp
- Small (16μm×16μm) pixel, targeting on 3μm single point resolution
  - To explore SOI 3D connection technology by designing the in-pixel digital logic in a separated tier
  - Or to look for any new process

Summary

- R&D started along the baseline design specifications
- 2nd CPS prototype design submitted
  - *More in-pixel electronics*
  - *New asynchronous readout architecture*
- CPS test system being developed and improved
- 2nd SOI prototype test in progress
  - *Sensor thinning*
  - Good performance shown by preliminary results
- Overall sensor architecture in consideration
- More expertise needed and collaboration welcomed

Thank you for your attention!

CEPC CDR Parameters

beta_y=2mm

D. Wang

	Higgs	*W*	*Z*
Number of IPs	2		
Energy (GeV)	120	80	45.5
Circumference (km)	100		
SR loss/turn (GeV)	1.68	0.33	0.035
Half crossing angle (mrad)	16.5		
Piwinski angle	2.75	4.39	10.8
N_e/bunch (10^{10})	12.9	3.6	1.6
Bunch number	286	5220	10900
Beam current (mA)	17.7	90.3	83.8
SR power /beam (MW)	30	30	2.9
Bending radius (km)	10.9		
Momentum compaction (10^{-5})	1.14		
β_{IP} x/y (m)	0.36/0.002		
Emittance x/y (nm)	1.21/0.0036	0.54/0.0018	0.17/0.0029
Transverse σ_{IP} (um)	20.9/0.086	13.9/0.060	7.91/0.076
ξ_x/ξ_y/IP	0.024/0.094	0.009/0.055	0.005/0.0165
RF Phase (degree)	128	134.4	138.6
V_{RF} (GV)	2.14	0.465	0.053
f_{RF} (MHz) (harmonic)	650		
Nature bunch length σ_z (mm)	2.72	2.98	3.67
Bunch length σ_z (mm)	3.48	3.7	5.18
HOM power/cavity (kw)	0.46 (2cell)	0.32(2cell)	0.11(2cell)
Energy spread (%)	0.098	0.066	0.037
Energy acceptance requirement (%)	1.21		
Energy acceptance by RF (%)	2.06	1.48	0.75
Photon number due to beamstrahlung	0.25	0.11	0.08
Lifetime due to beamstrahlung (hour)	1.0		
F (hour glass)	0.93	0.96	0.986
L_{max}/IP ($10^{34}cm^{-2}s^{-1}$)	2.0	4.1	1.0