ATLAS Upgrade

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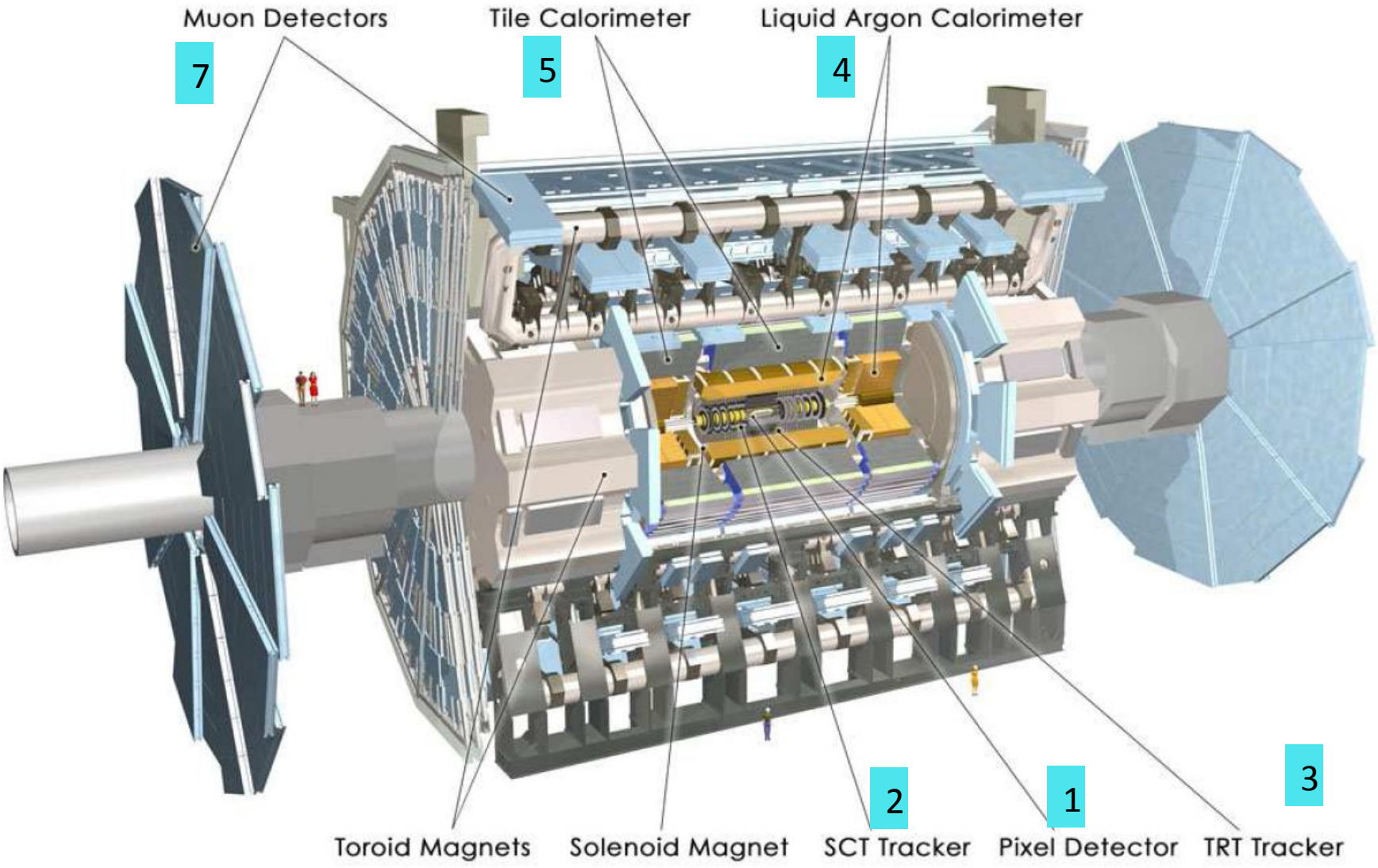
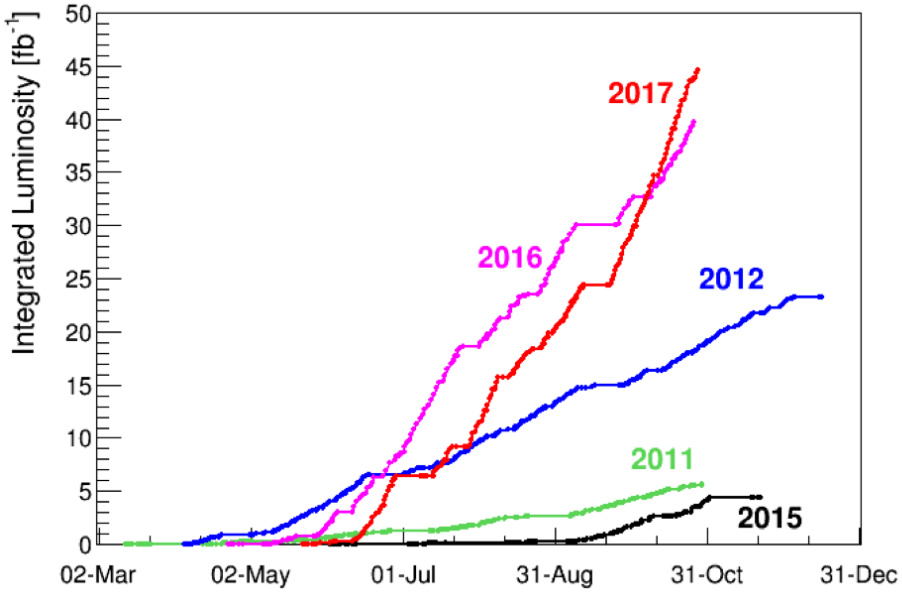
Outline

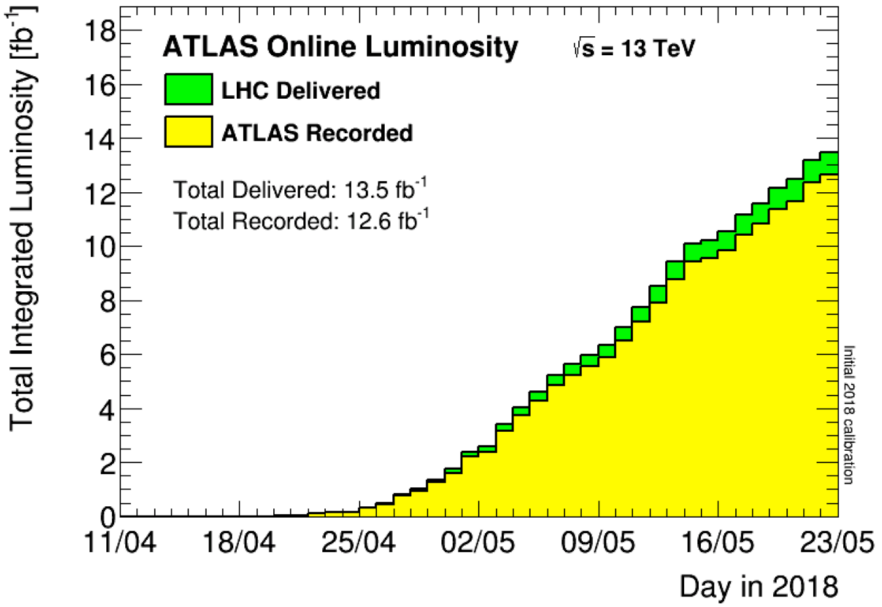
- Introduction to ATLAS experiment
- ATLAS upgrade
  - Phase-I upgrade
  - Phase-II upgrade
- Summary

ATLAS Detector

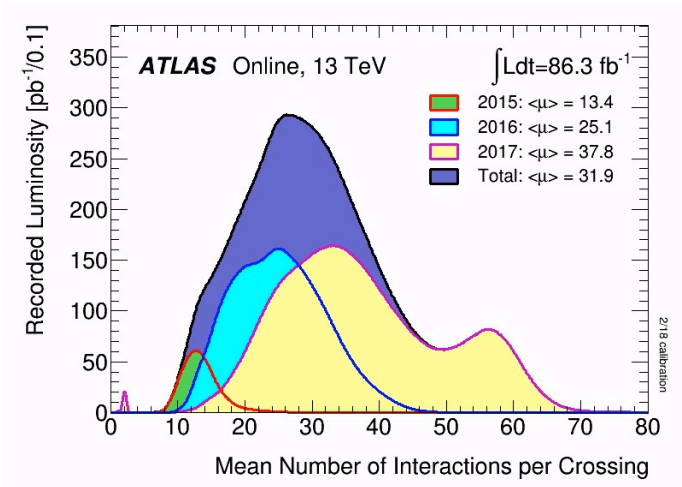


Data Collected by ATLAS

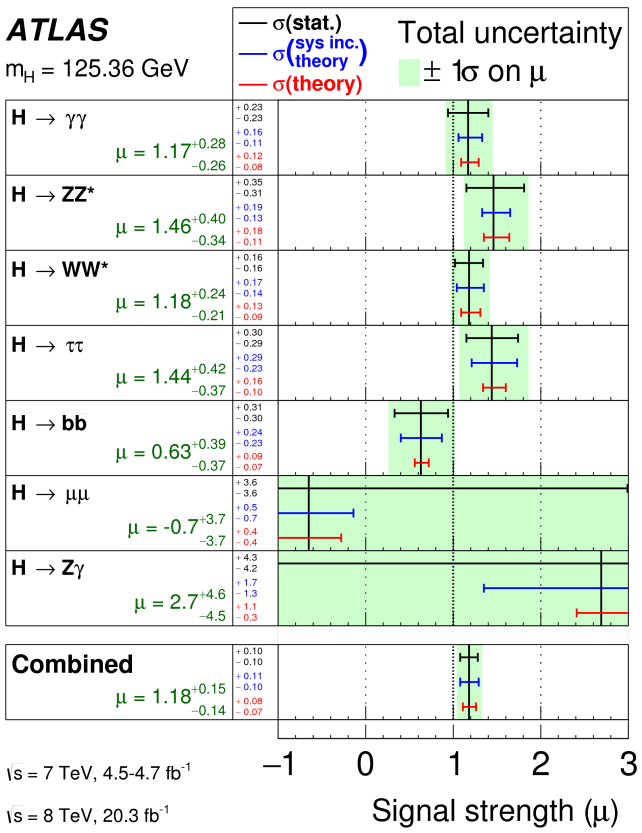


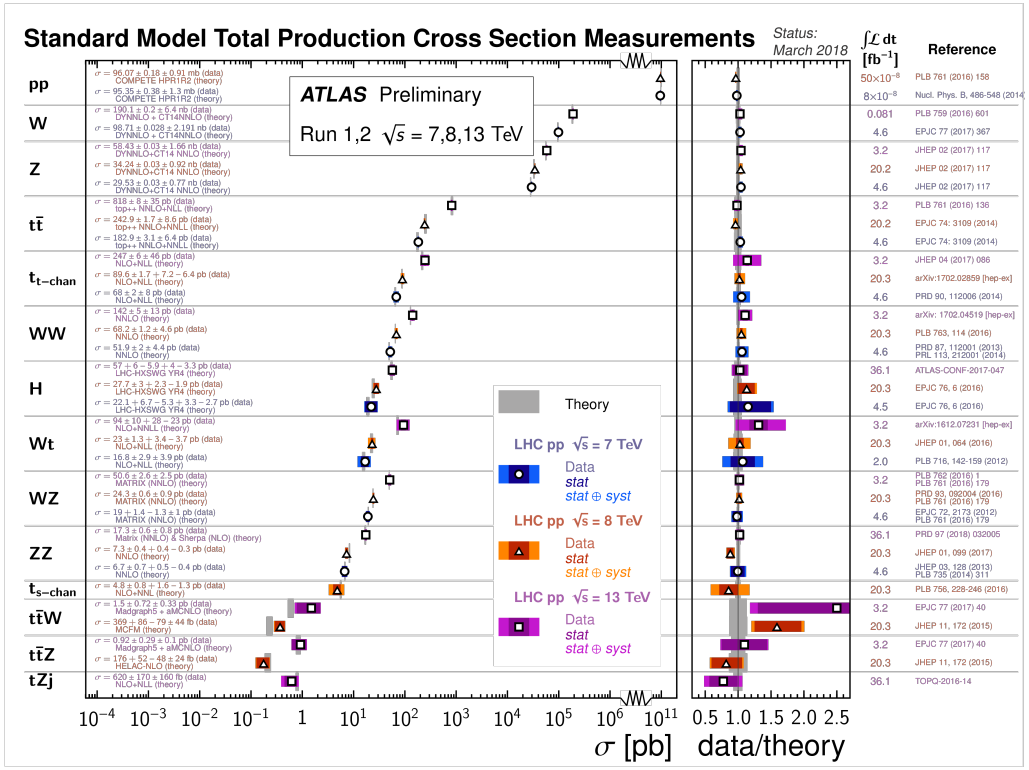


- ATLAS detector operated very successfully
- Pile-up increased significantly with higher peak luminosity.



ATLAS Physics Results



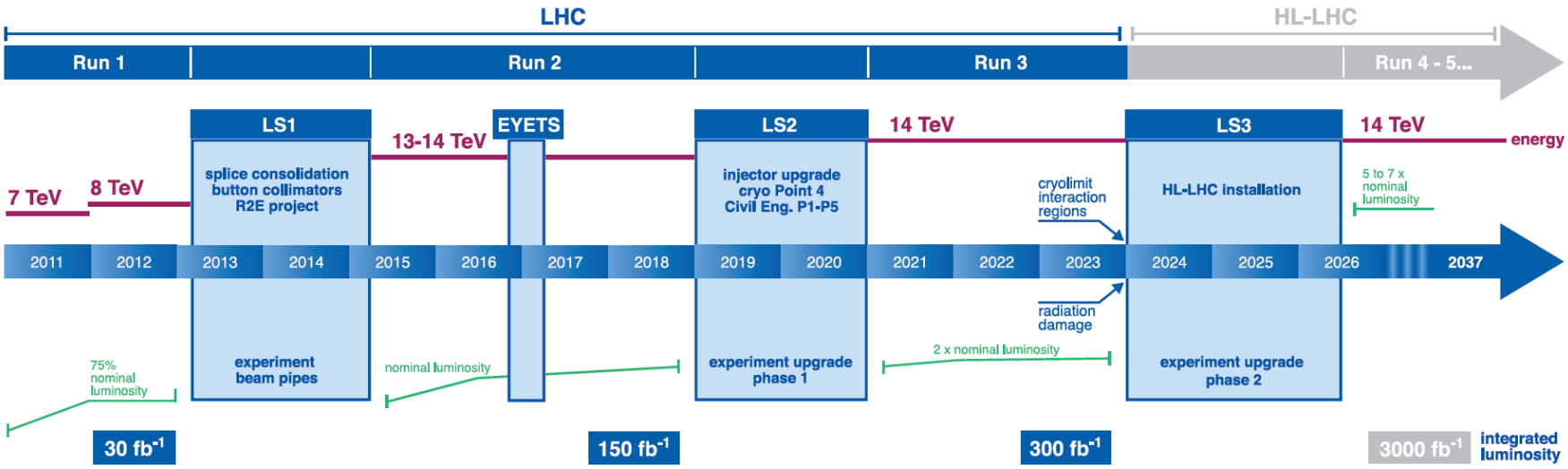


More data needed to improve the precision of Higgs measurements, other SM measurements, and new physics searches.

The High-Luminosity LHC (HL-LHC)

- Upgrade LHC luminosity to permit accumulation of 3 ab^{-1} data sample over a ~ 10 year run period following LS3 for machine and detector upgrades
- Plan for $\mathcal{L} = 5\times10^{34}\ cm^{-2}s^{-1}$ with ultimate luminosity of $\mathcal{L} = 7.5\times10^{34}\ cm^{-2}s^{-1}$

μ=140 μ=200



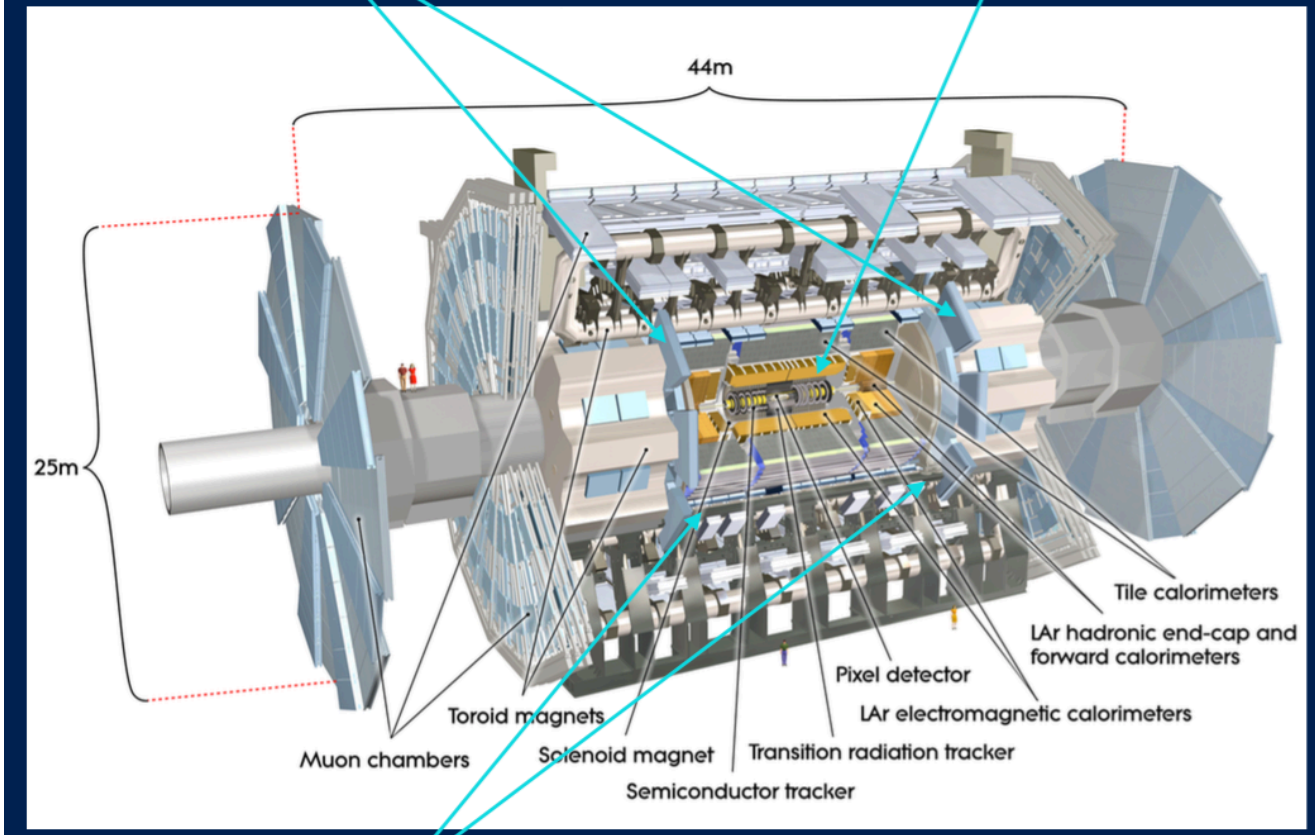
- ATLAS upgrades:

Long Shutdown 1 (LS1): RPC in barrel feet regions, MDT at |eta| in [1.1, 1.3], pixel IBL, HLT
Long Shutdown 2 (LS2): New Small Wheel, muon, LAr electronics, L1 calo, FTK, TDAQ
Long Shutdown 3 (LS3): many new systems, R&D activities and TDR preparation ongoing

ATLAS Phase-1 Upgrade

New Small Wheel detector

LAr front-end electronics



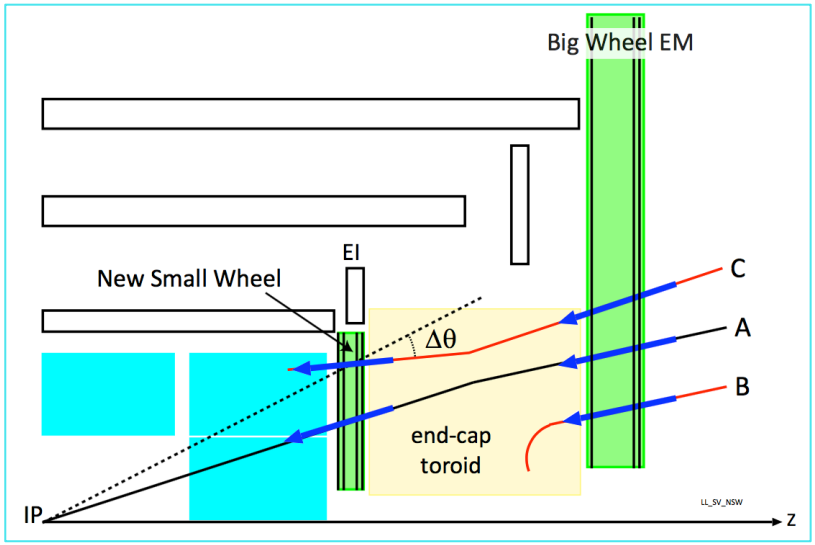
New muon RPC detector (BIS78)

TDAQ off-detector electronics:

- L1 hardware trigger:
  - L1 calorimeter
  - L1 topological
  - L1 NSW trigger
  - L1 endcap trigger
  - L1 MuCTPi
- L1.5 hardware trigger:
  - Fast Track Trigger
- readout system
- HLT

New Small Wheel

- Two 5 meter radius wheels in the inner end-cap region (1.3<|η|<2.7)
- Each wheel is formed by
  - 2 external sTGC quadruplets (mainly trigger, bunch ID identification + vector tracking with <1 mrad angular resolution
  - 2 internal MicroMegas quadruplets (mainly tracking spatial resolution <100 μm)
- Needed to reduce fake muon triggers in the end-cap region.



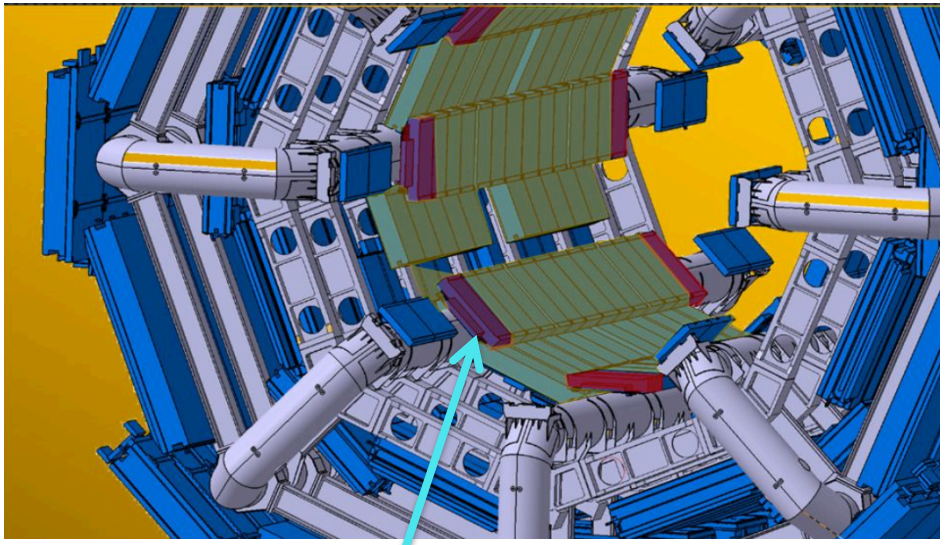
ATLAS-TDR-020-2013

Expected L1 muon rate for L = 3×10^{34} cm^{-2}s^{-1}

L1MU threshold (GeV)	Level-1 rate (kHz)
$p_T > 20$	60 ± 11
$p_T > 40$	29 ± 5
$p_T > 20$ barrel only	7 ± 1
$p_T > 20$ with NSW	22 ± 3
$p_T > 20$ with NSW and EIL4	17 ± 2

Barrel Inner Small Region (BIS78)

- NSW covers the region 1.3<|η|<2.7, while the big wheel covers 1.0<|η|<2.7
- Half of the region 1.0<|η|<1.3 covered by the existing EIL4 TGC end-cap trigger detectors
- New detectors in the BIS region cover the other half
- 16 RPC trigger chambers (8 each side)+ replacement of 16 existing MDT with sMDT
- The additional RPC chambers can significantly reduce the foreseen fake rate



Barrel Inner Smaller Region
BIS78 RPC+sMDT

- Phase II pilot project:

Same MDT and RPC detector technology that will be used for Phase II, when the full BI layer will be equipped

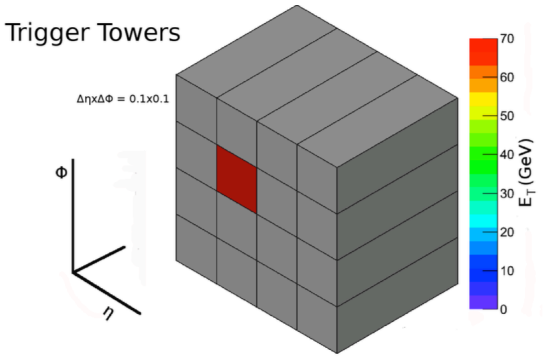
LAr Calorimeter and L1Calo New Electronics

LAr calorimeter:

- New Front-End (Trigger Digitizer Board) and Back-End (Digital Processing System Boards)
- Increased trigger tower granularity ($\Delta\eta \times \Delta\phi = 0.025 \times 0.1$)
- Good trigger performances with the increasing luminosity and pile-up:
  1. Low trigger rate, thanks to the background rejection
  2. Low thresholds and better turn-on curves, due to the higher geometrical resolution

L1Calo:

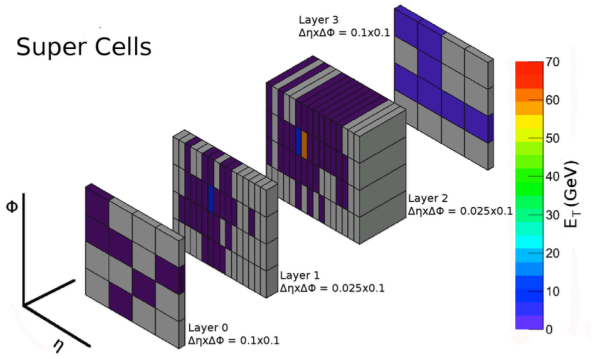
- New feature extractor boards: eFEX, gFEX, jFEX
- More refined processing of electromagnetic calorimeter information at higher granularity
- Better discrimination between photons, electrons, taus and jets
- Efficient signal object triggers for EW-scale physics



An electron with pT=70 GeV seen by existing L1-Calo trigger electronics

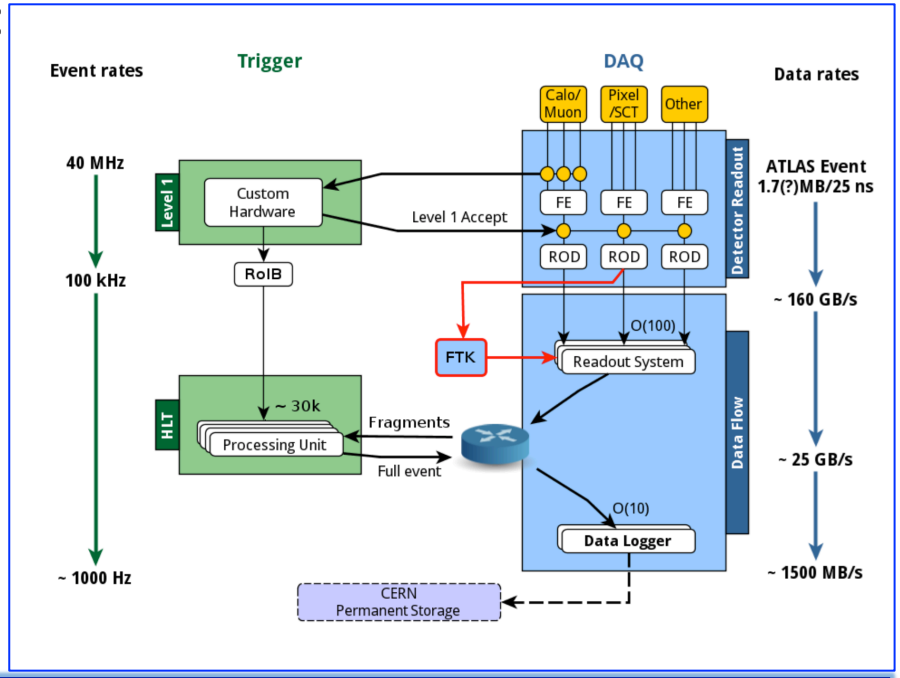
LEFT → Right

Seen by the proposed upgraded trigger electronics



Fast TracKer (FTK)

- A system of electronics, using data from pixel, SCT, and IBL
- Performs real-time tracking for all events accepted by the Level-1 trigger (no RoI), supporting HLT decision
- Efficiency > 90% for p_T >1 GeV, $|\eta|$<2.5, rate up to 100 kHz, latency <100 μs
- Provides tracking information to Level-2 in ~ 25 μs
- Based on pipelined custom hardware:
  - Frist stage (pattern recognition) + second stage (track fitting)
  - 8192 associative memory custom chips > 1000 FPGAs
- Expected to be done 100% for Phase-I.



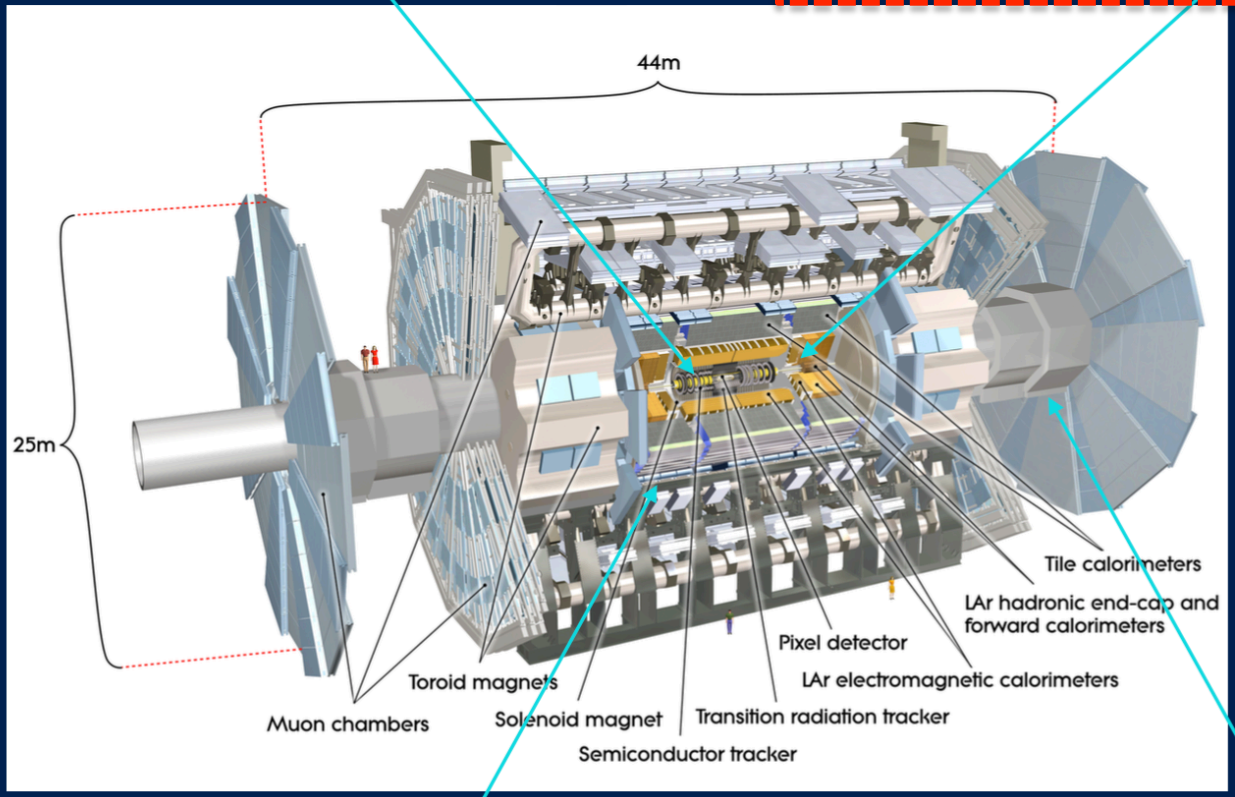
TDAQ Phase-I

- L1 calo:
  - new trigger and readout electronics, new fibre optics system
  - finer granularity data, more efficient algorithms
- L1 topo:
  - new board: topological algorithms, calorimeters and muons
- L1 end-cap:
  - New muon end-cap sector logic board with new inputs
  - New Small Wheel muon system (trigger processor boards)
  - RPC new BIS78 trigger boards
  - Outer layer of the extended barrel of the Tile Calorimeter
  - Reduce the fake trigger rate
- L1 MuCTPi: new Muon to Central Trigger Processor interface board
- FTK: new hardware track system
- HLT: output rate up to 1 kHz
- Felix readout system:
  - Function as a router between the FE links and commercial multi-gigabit network technology
  - Previous hardware RODs are replaced with software processes
  - Phase-I: NSW, BIS78, L1calo. It will be the standard system for phase-II

ATLAS Upgrade for Phase-II

NEW ALL-SILICON INNER TRACKER (ITK) WITH ETA COVERAGE UP TO 4

HIGH GRANULARITY TIMING DETECTOR (HGTD) IN FORWARD REGION (OPTION)



TDAQ OFF-DETECTOR ELECTRONICS:

- L0 HARDWARE TRIGGER:
  - L0 CALORIMETER
  - L0 TOPOLOGICAL
  - L0 MUON
  - L0 GLOBAL
- L1 HARDWARE TRIGGER (OPTION):
  - L1 GLOBAL
  - L1 TRACK TRIGGER
- READOUT SYSTEM
- HLT

NEW MUON CHAMBERS IN THE INNER BARREL REGION

FORWARD MUON TAGGER (OPTION)

Inner Tracker

- The first ATLAS Phase-II TDR (ATLAS-TDR-025-2017), covering the outer part of the tracker based on silicon strip detector, submitted to the LHCC
- New all-silicon tracking system
  - pixel detector at small radius close to the beam line + large area strip tracker surrounding it
  - Central region: five pixel layers followed by two short-strip layers of paired stereo modules, then two long-strip layers of paired stereo modules
  - Forward regions: six strip disks and a number of pixel rings leading to one or more hits depending on the ring layer and η position
- Extension up to $|\eta| = 4$
- Nearly ten times more electronics channels (60 million)

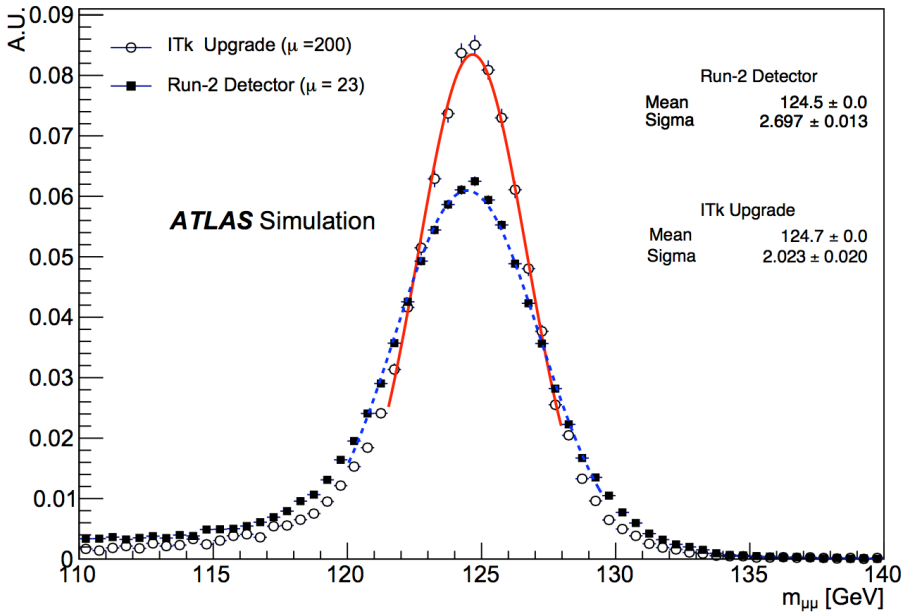
Performance with ITk

- Equal or better performances than the existing detector in a much more difficult tracking environment

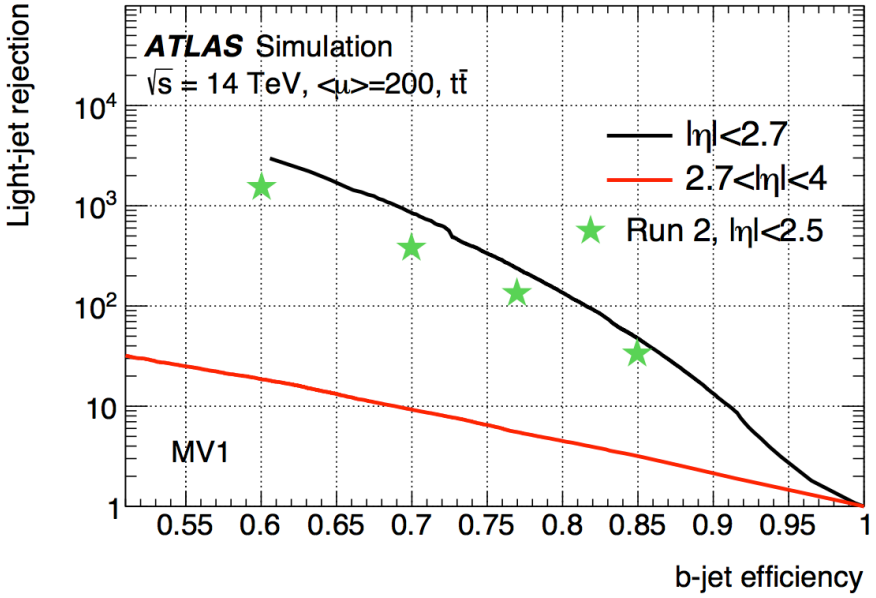
  - high track reconstruction efficiency and low rate of fake tracks

  > 99% efficiency for muons with p_T > 3 GeV: 85% efficiency for pions and electrons above 1 GeV, keeping fake rates below 1%

Mass resolution for H→μμ events



Performance of MV1 Btagging Algorithm



LAr Calorimeter + HGTD

Liquid Argon Calorimeter

- Current electronics is not compatible with phase-II requests (latency and trigger rate)
- Radiation hardness requirements are above original design (1 kGy and 2.7 × 1013 neq/cm2)
- Phase-I upgraded boards will continue to be used
- New front-end and back-end electronics
- Full granularity FE digital data sent at 40 MHz to back-end

High Granularity Timing Detector (HGTD)

- Motivation: pile-up mitigation, improve e/γ and Jet/E_t^{miss} performance
- Lower trigger thresholds and increased physics acceptance; validate isolation for e/ɣ
- Sort charged tracks by time to reduce confusion in tracking and particle flow

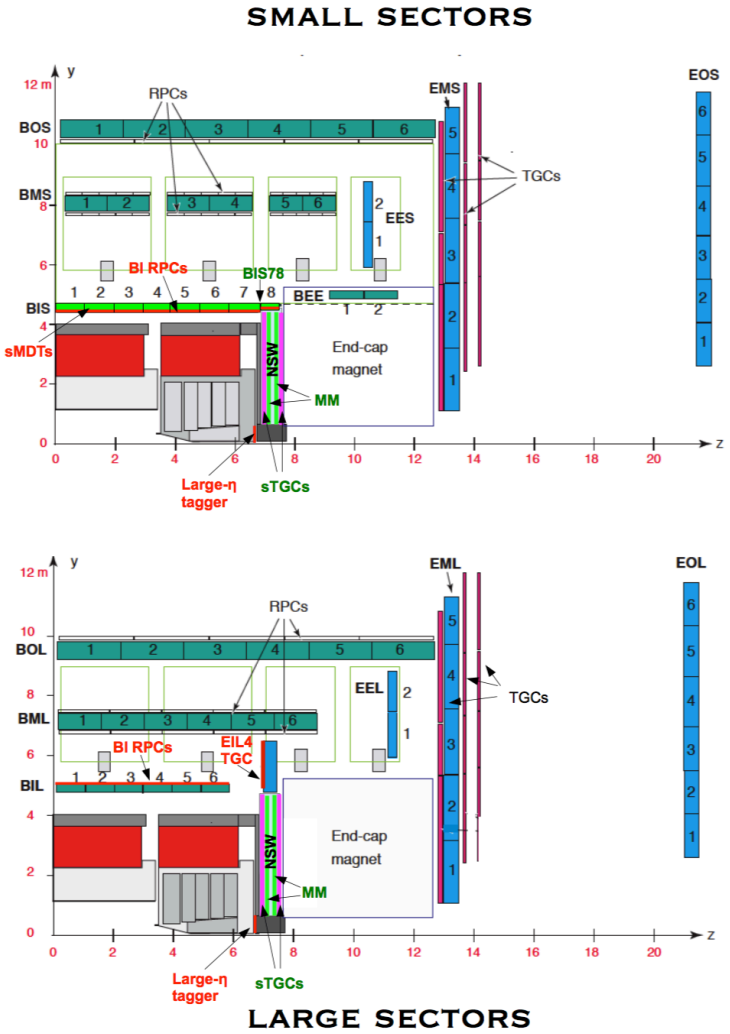
Pseudorapidity coverage	$2.4 < \|\eta\| < 4.0$
Thickness in z	75 mm (+50 mm moderator)
Position of active layers in z	3435 mm $< z <$ 3485 mm
Radial extension:	
Total	110 mm $< R <$ 1000 mm
Active area	120 mm $< R <$ 640 mm
Time resolution per track	30 ps
Number of hits per track:	
$2.4 < \|\eta\| < 3.1$	2
$3.1 < \|\eta\| < 4.0$	3
Pixel size	1.3×1.3 mm^2
Number of channels	3.54M
Active area	6.3 m^2

Tile Calorimeter

- Motivations for the upgrade:
  - Better radiation tolerance, better precision and finer trigger granularity
  - Increased rate and latency
  - Ageing of components exceeding the design lifetime
- New electronics:
  - High speed optical communication for full data transmission at 40 MHz to off-detector electronics
  - Reduced modularity
  - Digital information for the L0/L1 Trigger systems
  - Full redundant data path and powering

Muon Detectors

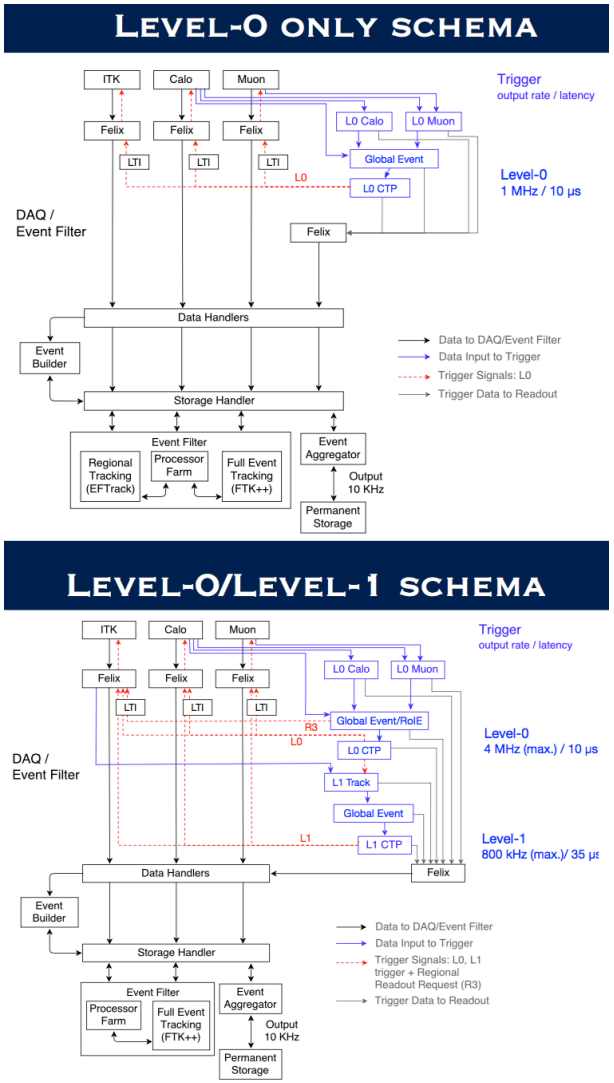
- Motivation:
  - Reduce the trigger fake rate in barrel and end-cap regions
  - Increase trigger performances
  - Increase geometrical coverage in the barrel
- New detectors:
  - Barrel inner RPC + sMDT:
  - old BIS MDT replaced by new (sMDT + RPC)
  - new RPC mounted on top of existing BIL MDT
  - TGC EIL4
  - Large-eta-tagger: up to $|\eta| = 4$; several physics channels identified and under study (Micro-Pattern Gas Detectors)



Level-0 and Level-0/Level-1 TDAQ

- L0 trigger rate = 1 MHz; L0 latency = 10 μs
- The Global Event processor replaces the existing L1Topo and integrates topological functions with additional selection algorithms using additional information from the calorimeters

- L0/L1 schema introduces a second level of hardware track trigger (pattern recognition with AM chips + track fitting with FPGA)
- L0 trigger rate = 4 MHz; L0 latency = 10 μs
- L1 trigger rate = 800 kHz; L1 latency = 35 μs
- The L0 Global Event processor generates the commands request for the read out of the data from the ITk detector
- The L1Track receives ROI from ITk and performs track finding
- The L1 Global Event processor refines e/γ, τ, jets and ETmiss signatures and improves rejection by combining
  The refined calorimeter signature information with
  The tracking information from L1Track



Summary

- The large datasets to be collected with the High-Luminosity LHC will allow to:
  - Precision measurements in the 125 GeV Higgs boson sector
  - Search for rare Higgs boson decay modes
  - Study the low production cross section Standard Model processes
  - Search for new phenomena beyond Standard Model
- Phase-I upgrades:
  - Advanced state, production starting soon for most of the systems
  - Provides improved rate capabilities and background rejection for L=2-3x10^{34} $cm^{-2}s^{-1}$
- Phase-II upgrades:
  - Designed for L=5-7.5 x 10^{34} $cm^{-2}s^{-1}$ and 3000 fb^{-1}
  - Up to factor 10 increase in radiation hardness
  - Improved pile-up handling with new tracker and possible timing detector
  - Trigger and readout capabilities
  - Different options for the upgrades under evaluation

Collaboration among FCPPL Institutions

- Many French and Chinese institutions are involved in many aspects of the Phase I and II upgrade.
- The Phase II program is now acted and agreed by LHCC and ATLAS collaboration, TDR published and the final funding agency validation is ongoing.
- It is the time to think possible collaborations:

For Phase II

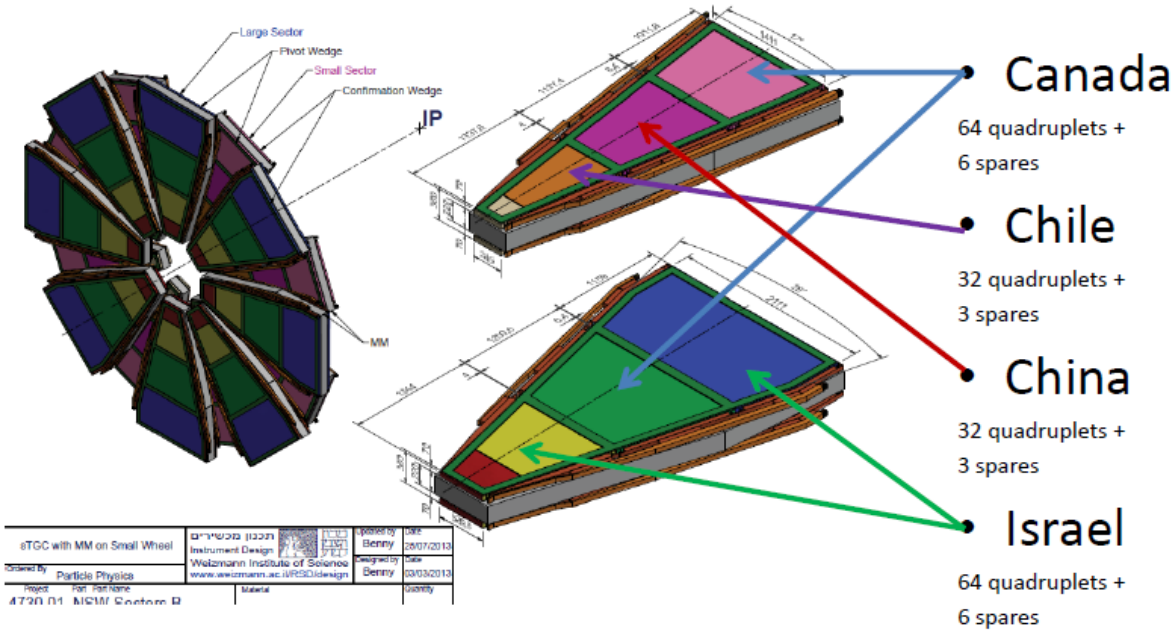
- ✓ CPPM, LAL, LAPP, LPC, LPNHE, LPSC (LAr (Calo +HGTD), ITK, TILE)
- ✓ IHEP, Tsinghua, Nanjing: ITk silicon
- ✓ USTC, SDU, STJU: NSW, RPC-electronics
- ✓ Chinese clusters may also join the effort on HGTD

Large rooms for strong collaboration on many aspects, already on pixel R&D, intense data treatment (optical links and FPGA, O(Tb/s)), trigger for the various subsystems, as well as new detectors (HGTD,...)

Thanks!

Thanks to Riccardo Vari for a couple of his slides.

sTGC at Shandong University



China: 144 sTGC chambers 365 strip channel, 30 wire channel, 45 pad channel

完成sTGC Module-0样品，并进行了宇宙线扫描测试

High Luminosity Projections

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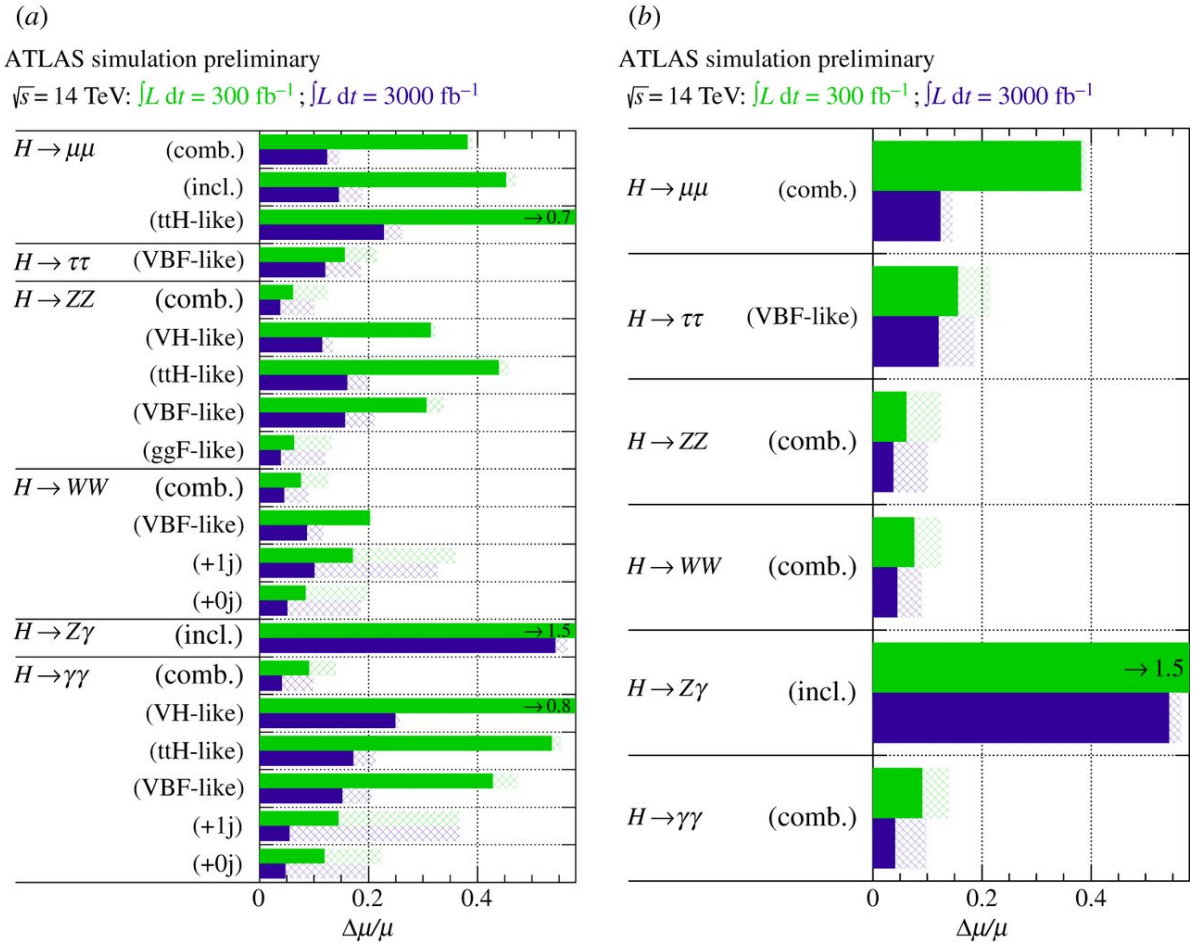
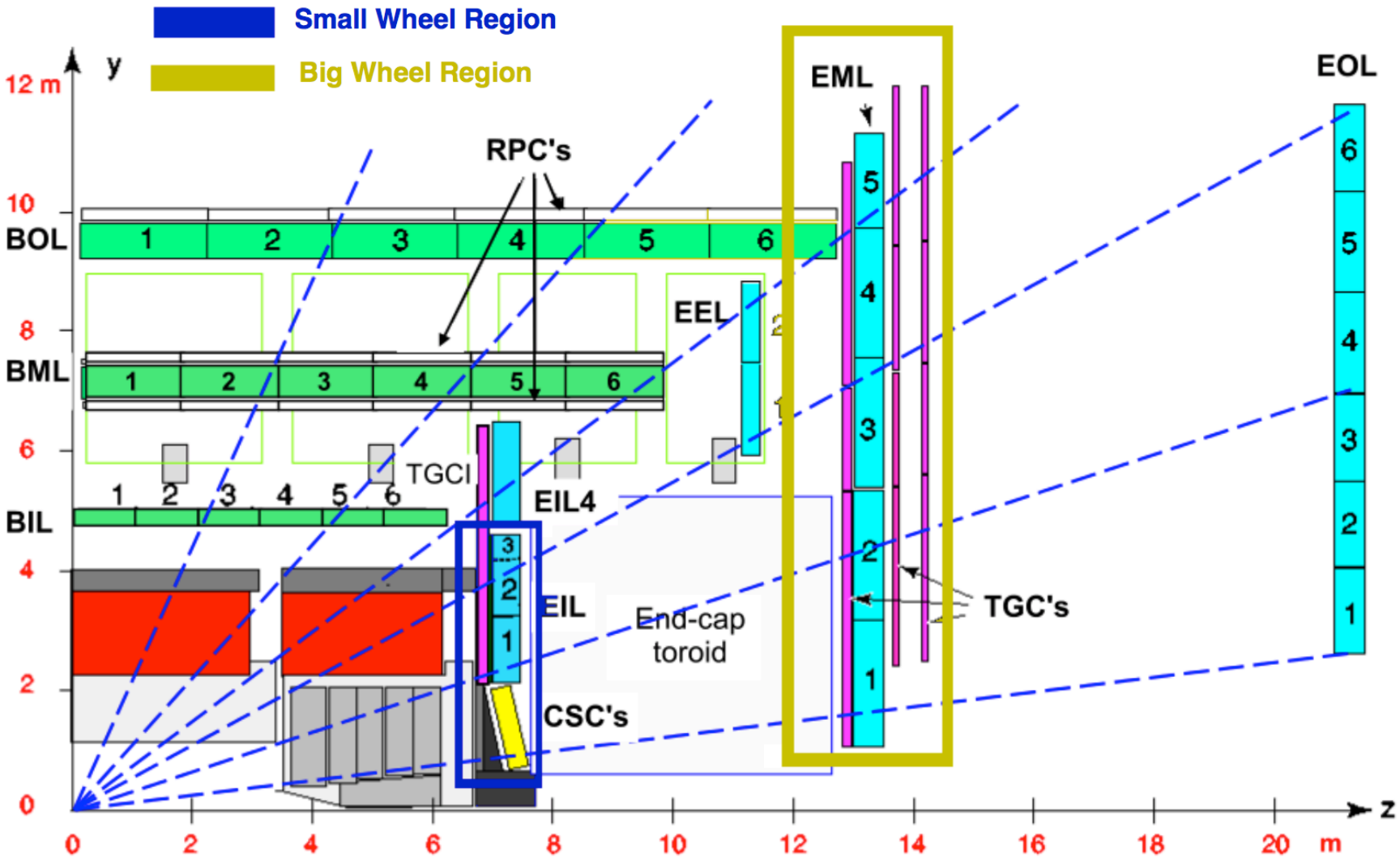
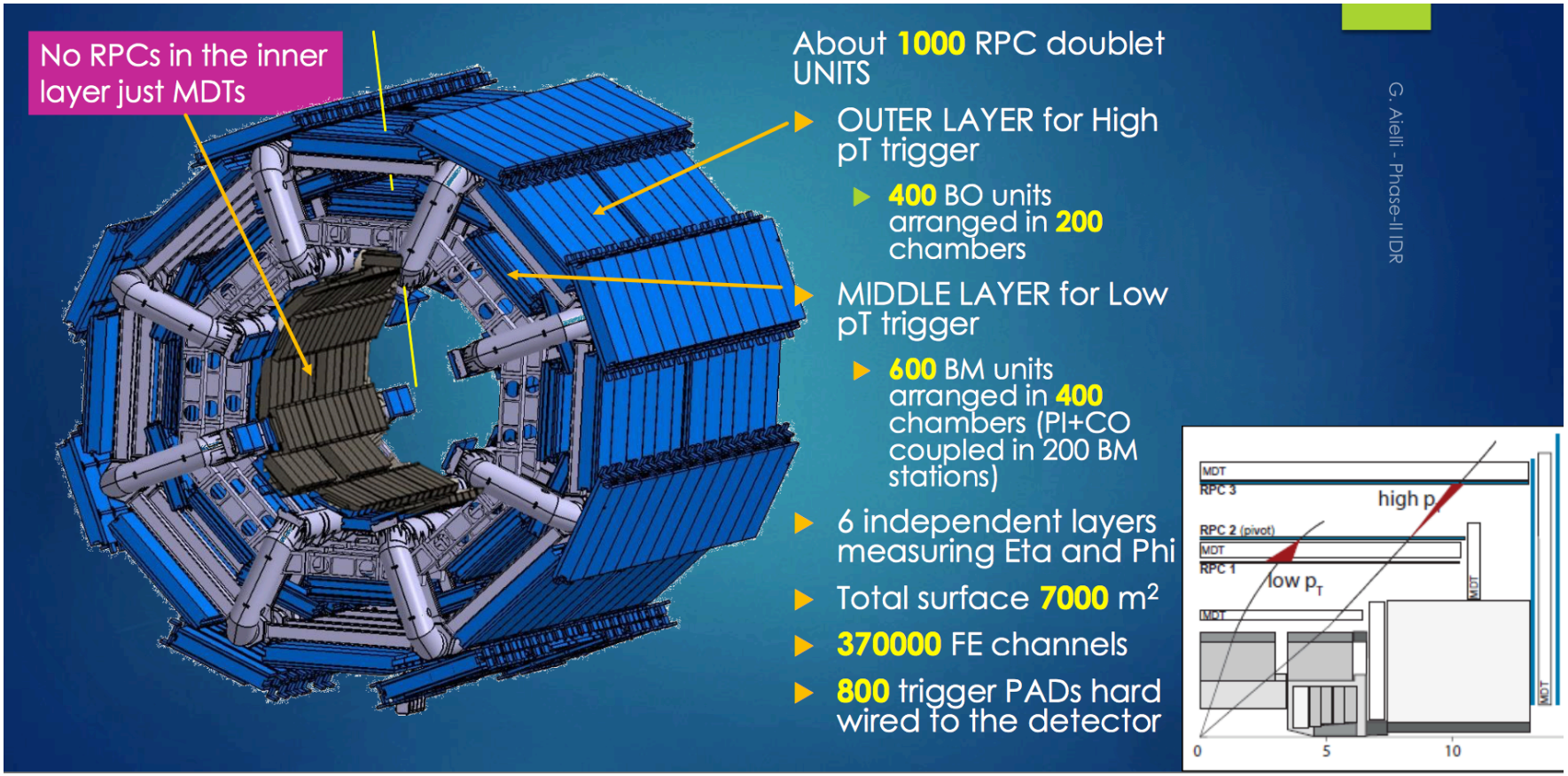


- HL-LHC can improve by a factor of 2–3, without the inclusion of theoretical systematic uncertainties
- The hashed areas indicate the increase in error due to current theory systematic uncertainties.

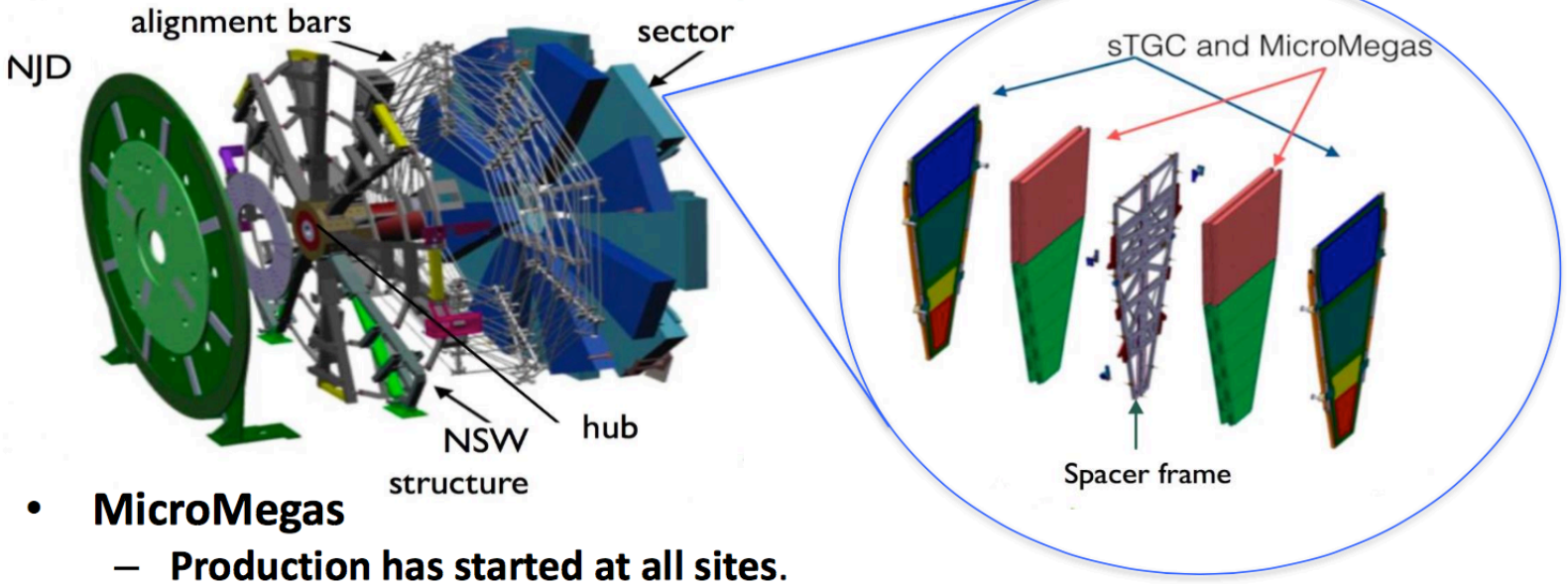
Z-Y View of ¼ of the ATLAS Detector



RPC System


No RPCs in the inner layer just MDTs
About 1000 RPC doublet UNITS
OUTER LAYER for High pT trigger
400 BO units arranged in 200 chambers
MIDDLE LAYER for Low pT trigger
600 BM units arranged in 400 chambers (PI+CO coupled in 200 BM stations)
6 independent layers measuring Eta and Phi
Total surface 7000 m2
370000 FE channels
800 trigger PADs hard wired to the detector
G. Aielli - Phase-II IDR
MDT
RPC 3
high pT
RPC 2 (pivot)
MDT
RPC 1
low pT
MDT
MDT
MDT
0
5
10

Upgrade Phase-I : New Small Wheel



- **MicroMegas**
  - **Production has started at all sites.**
  - Some batches of PCB for strip electrodes had cut strips (getting back on track again).
  - **New cleaning protocol (due to HV problems) to be deployed at production sites.**
  - Resume chamber assembly in 1-2 months, panel production continues uninterrupted.

- **sTGC**
  - Moved forward towards **series production**.
  - **Production schedule very tight.**
  - **First module** fully closed and completed.

In parallel, getting ready for wedge integration @ CERN

Pixel Layout

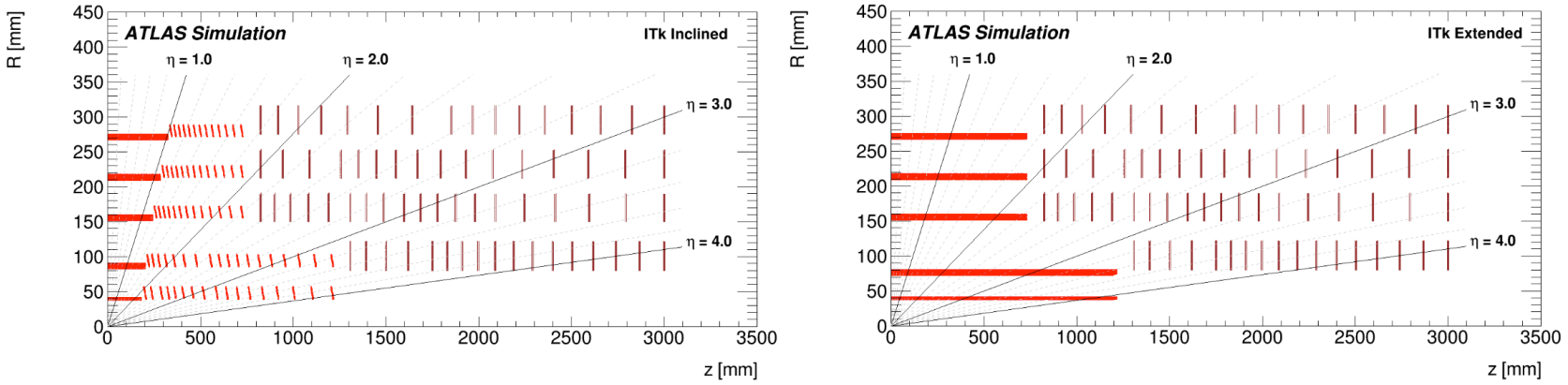
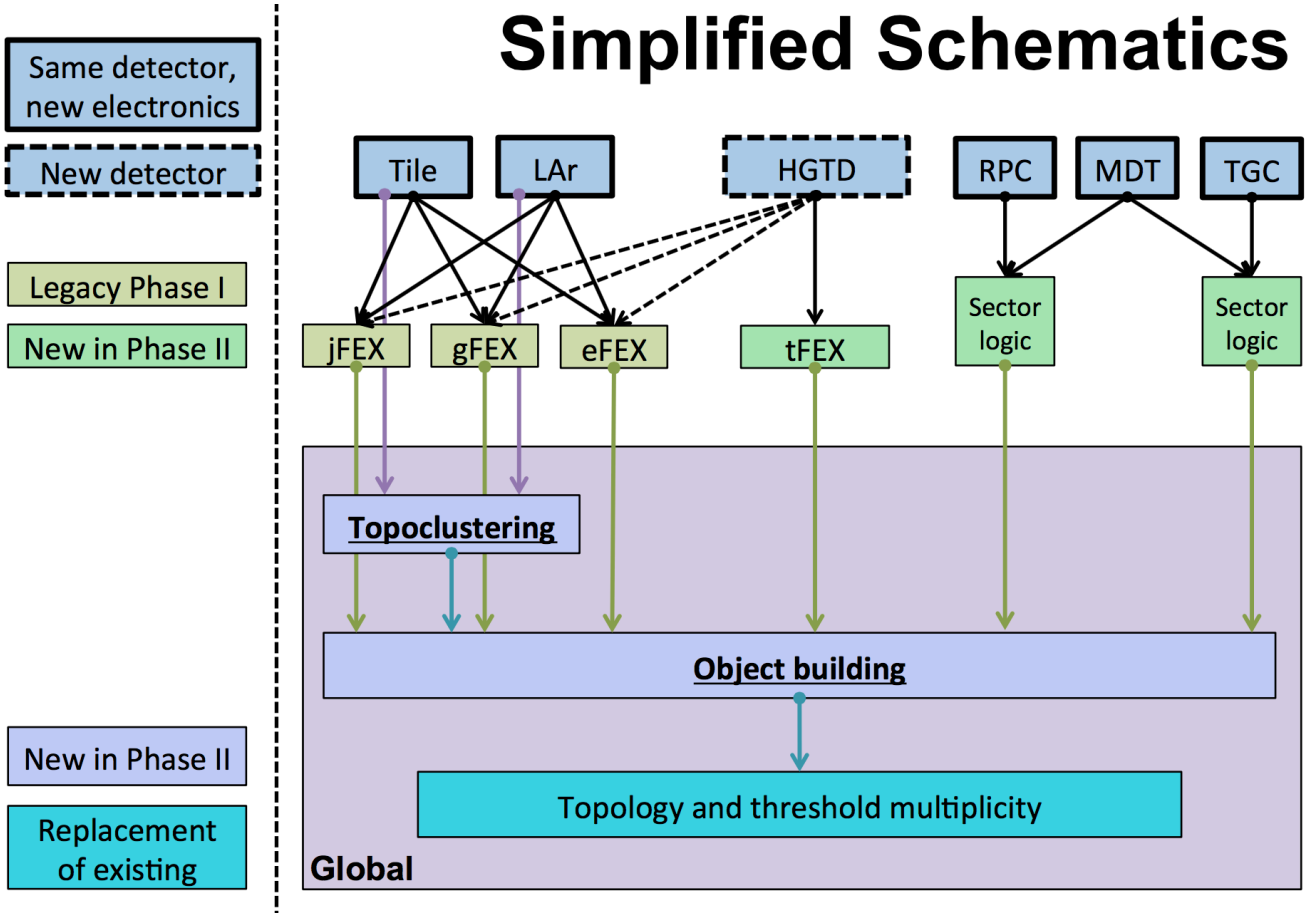


Figure 3.4: Diagrams showing simulated energy deposits in active layers for the two candidate layouts zoomed in on the Pixel barrel. **Left:** The Inclined layout. **Right:** The Extended layout.

- In the Inclined stave concept the material transversed by particles close to the interaction region in the very forward region is minimised. This provides better impact parameter resolution for particles within the p_T-range relevant for jet vertex tagging.
- Multiple hits on a track in the first layer close to the interaction region facilitates robust track finding and thus improves the tracking efficiency for primaries and fake rates.
- With an Inclined inner pixel barrel system with more hits, it is possible to reduce the complexity of the Pixel Detector end-cap ring system, significantly reducing the amount of needed pixel surface to achieve the necessary hit coverage. At the same time, the inclining sensors on the barrel staves allows to cover the same η range as with Extended barrel staves with less silicon surface.

Level-0 Calorimeter Trigger (L0calo)



High Luminosity Impact on the Experiment

- HIGH LUMINOSITY IS NEEDED TO ACHIEVE PHYSICS GOALS
- ALL PARTS OF THE EXPERIMENT HAVE TO STAND A PEAK LEVELLED LUMINOSITY OF 7.5×10^{34} CM^{-2}S^{-1}
- DETECTOR CHALLENGES:
  - HIGH PILEUP (<μ> UP TO ~200 COLLISIONS/ CROSSING)
  - HIGH RADIATION LEVELS (~10^{16} NEQ/CM^2; 10 MGY)
- REQUIREMENTS:
  - KEEP GOOD PHYSICS PERFORMANCES IN THIS CHALLENGING ENVIRONMENT, AT LEAST AS GOOD AS IN RUN 2 AND 3
  - KEEP ACCEPTABLE TRIGGER RATE WITH LOW P_T THRESHOLD
  - MITIGATE PILE-UP UP TO HIGH η

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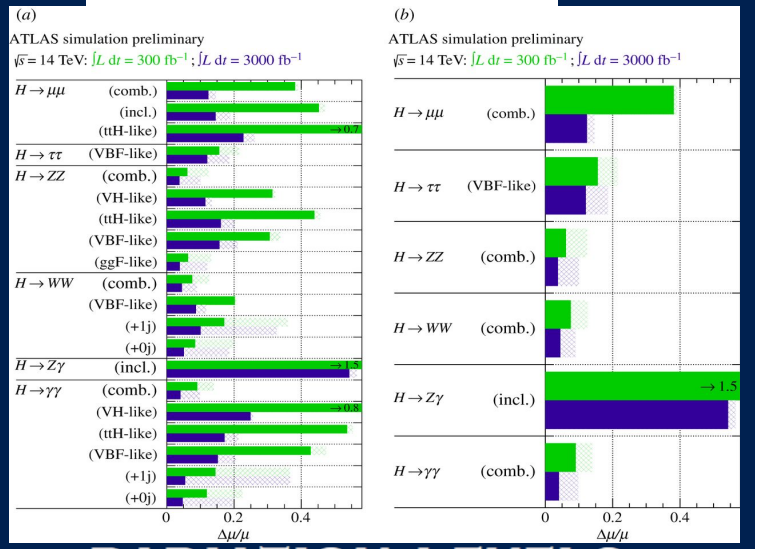

RADIATION LEVELS