ATLAS Silicon Pixel R&D

-CPPM /ACC perspective-

11th FCPPL workshop

May 22nd, 2018

Marlon Barbero

CPPM / ATLAS Chinese Cluster Collaboration

- CPPM / ACC collaboration for design and test of Front-End pixel electronics for ATLAS phase II upgrade.

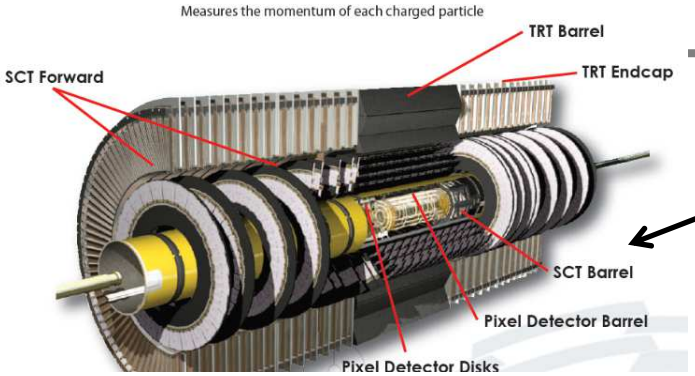
- Scientific cooperation supervised by Pr. Xinchou LOU, Dr. Zheng WANG and Pr. M.B., derived from ACC / ATLAS CPPM project (Pr. Jin SHAN / Dr. Emmanuel MONNIER)

  …involving IHEP, SDU (Pr. Meng WANG) and CPPM

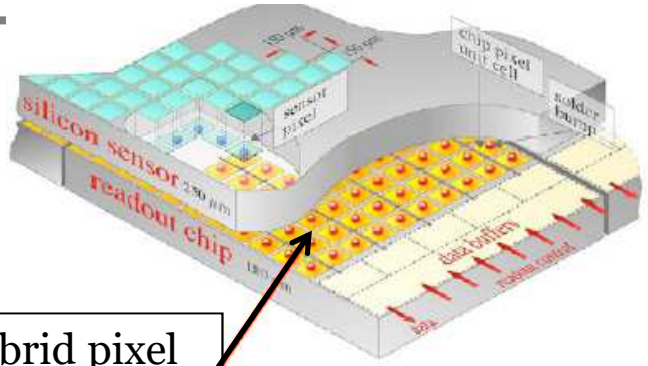
Plan

- Historical aspects:
  - Original ATLAS 3-pixel layers + IBl in 2014.
- ITk and new developments.
  - ATLAS ITk (Inner Tracker) upgrade
  - RD53 and 65nm Front-End electronics
  - Novel CMOS sensors
- Conclusion
  - Chinese-French prospects for collaboration

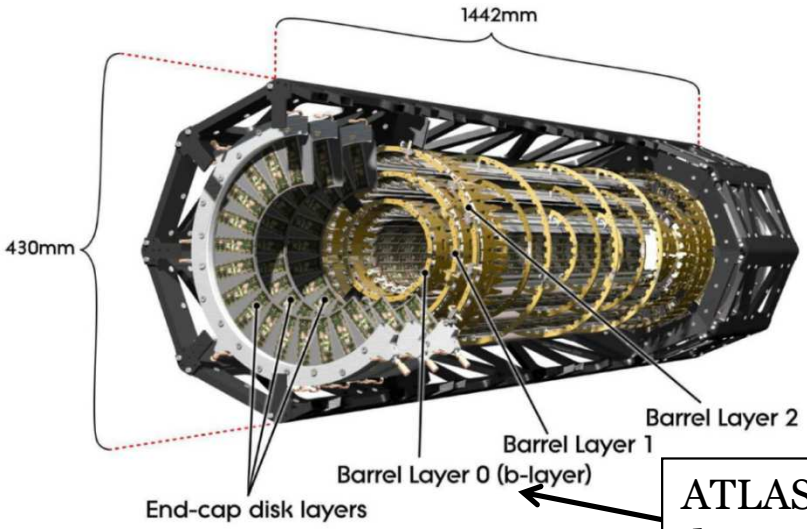
Original pixel detector



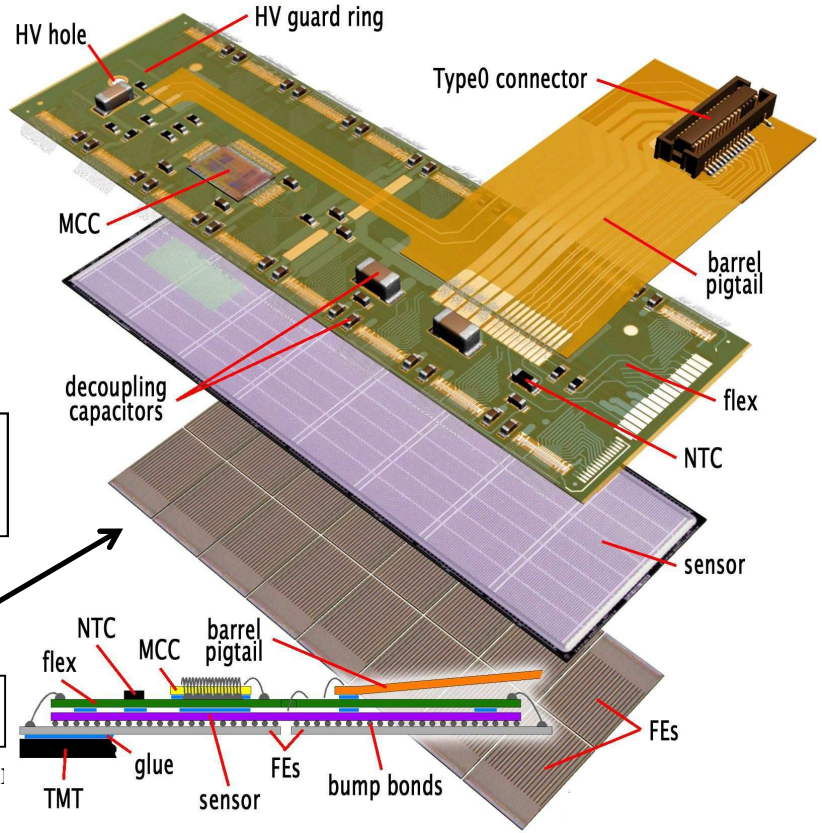
ATLAS Tracker (<2014)



Hybrid pixel



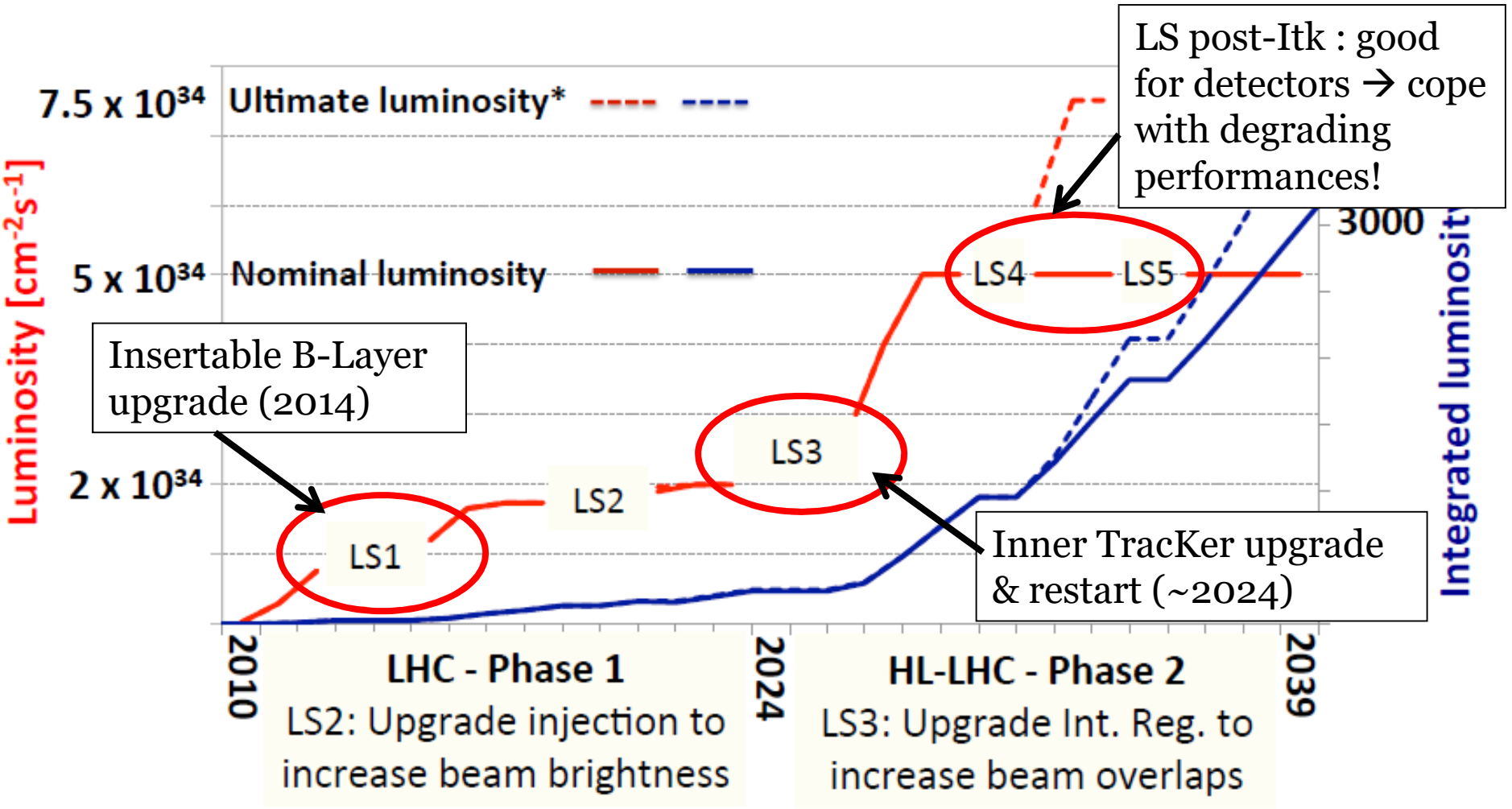
ATLAS Pixel detector (<2014)



Original hybrid module

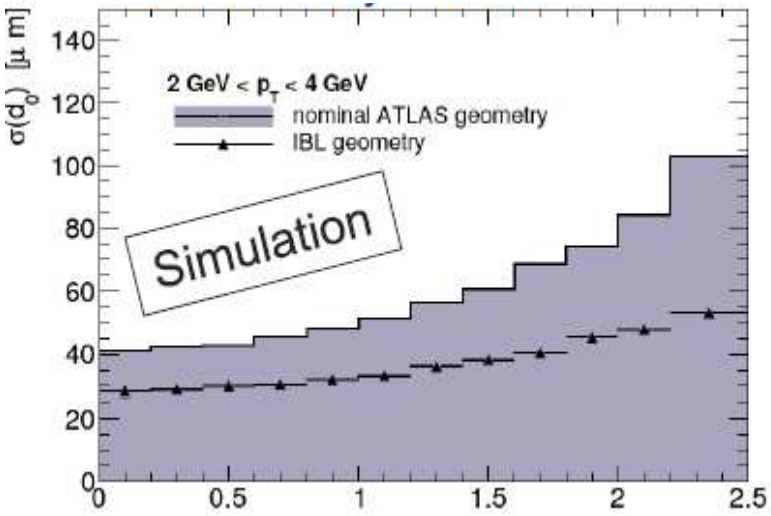
The initial ATLAS pixel detector: 87 millions pixels of size 50×400μm^2, in a 3-layer cylinder, cooled down at -15°C, measuring particle crossing 40 millions times per second!

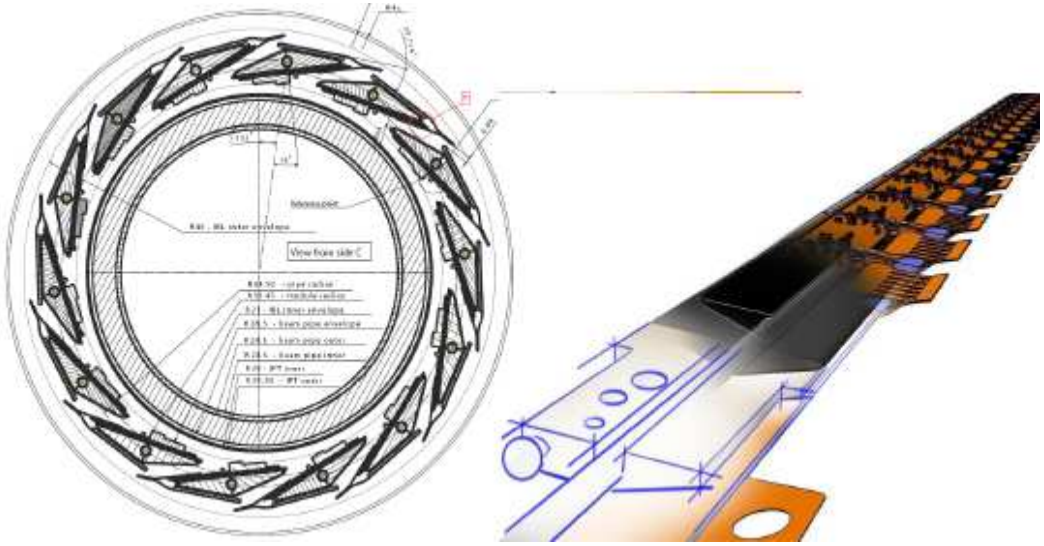
Long Shutdowns & Upgrades



IBL motivation

- Improve b-tagging performances:
  - Impact parameter resolution improves by factor ~2.
  - Light jet rejection at higher pileup >2 better (for fix b-tag efficiency).
- Increase robustness of pattern recognition, in particular in case of B-layer modules failures.
- New innermost layer between beam pipe and initial inner layer.
  - 2 mm mechanical clearance!
- Short distance to interaction point:
  - High particle flux.
  - High occupancy (10^{-4} → 10^{-3} / pix.)
  - Radiation damage 250 MRad.

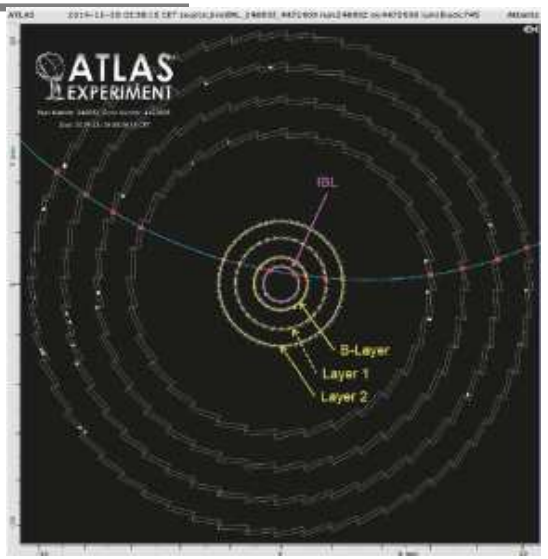


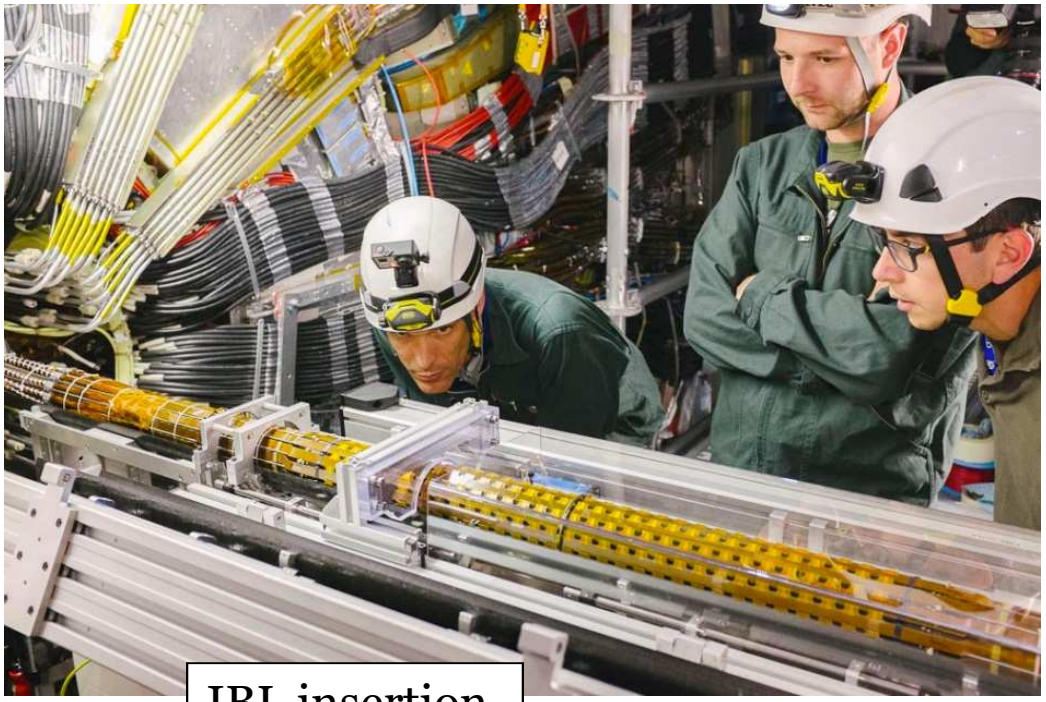


IBL upgrade

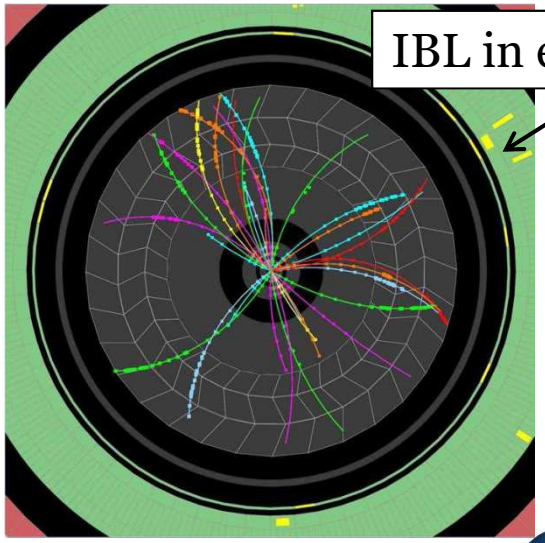
- 2014: The IBL upgrade!

IBL w. cosmic



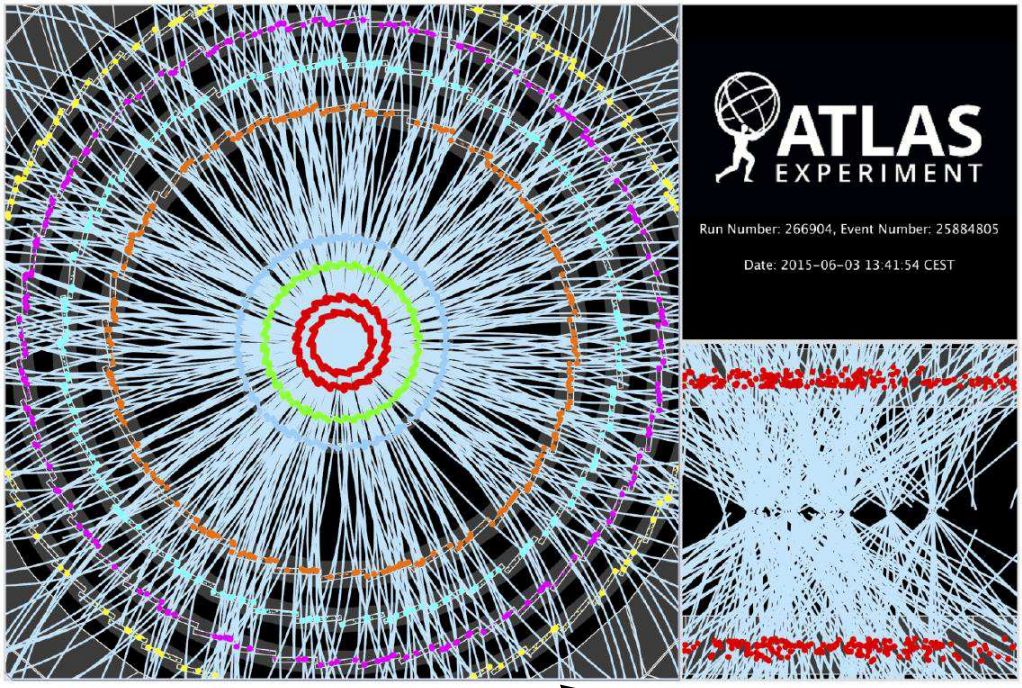


IBL insertion



IBL in event

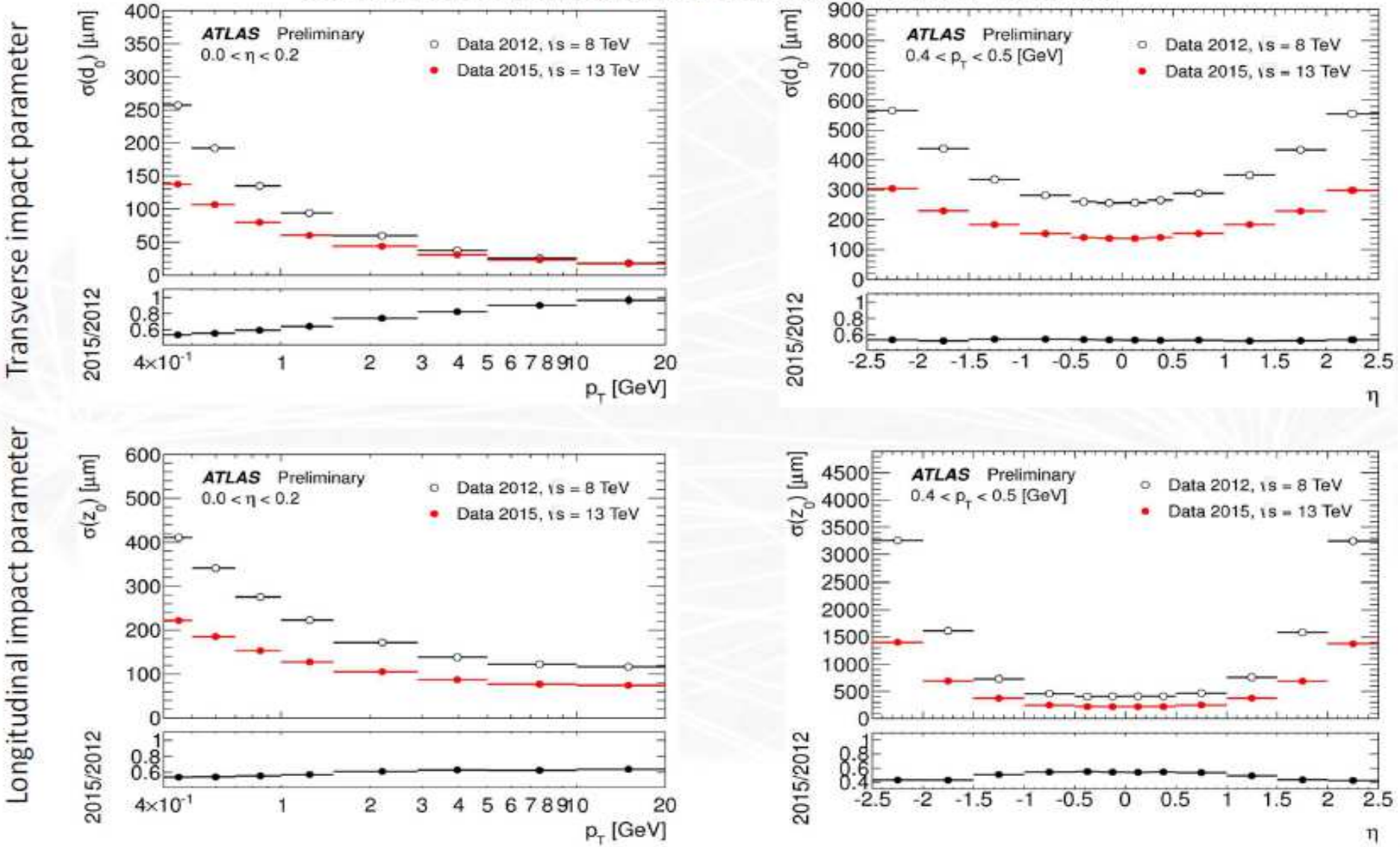
IBL upgrade



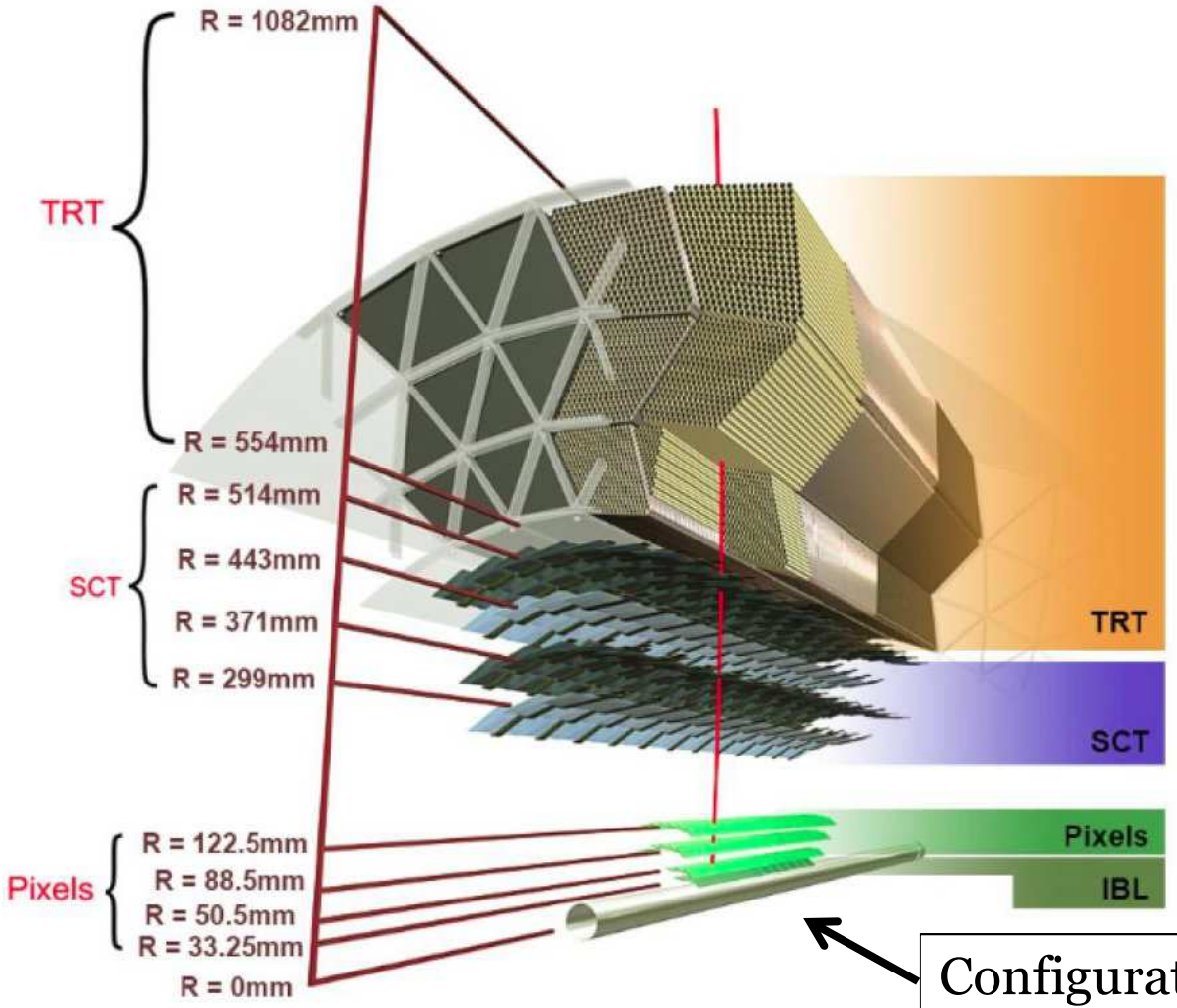
Multiple vertices disentangled with the IBL!

IBL upgrade

Comparison of Run 1 and Run 2 impact parameter resolution

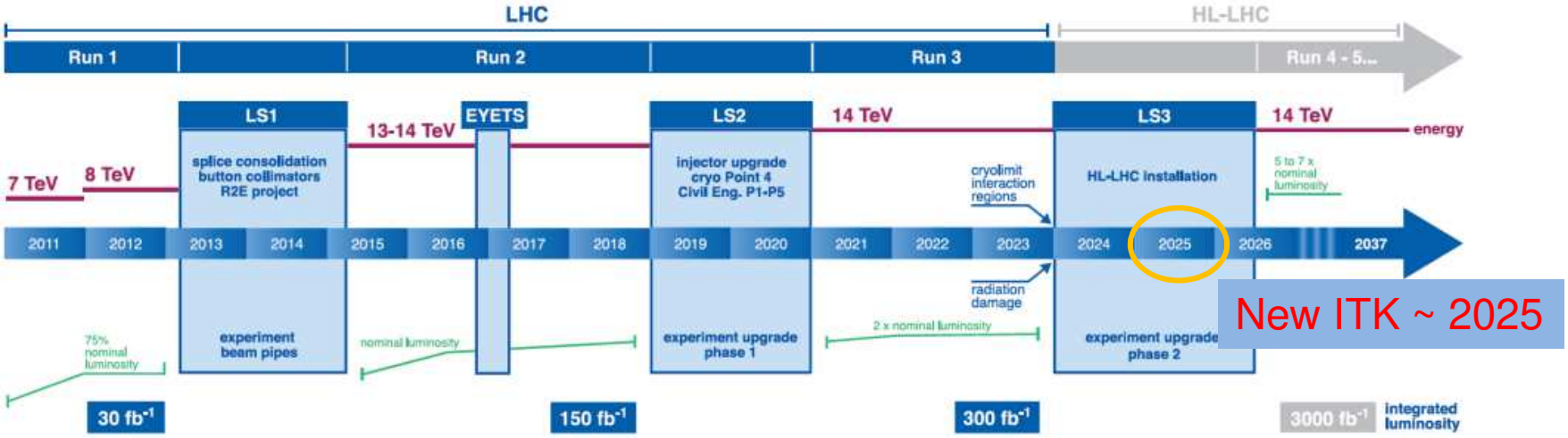


ATLAS tracker (present: 10m² silicon→ ~200m² for ITk!)



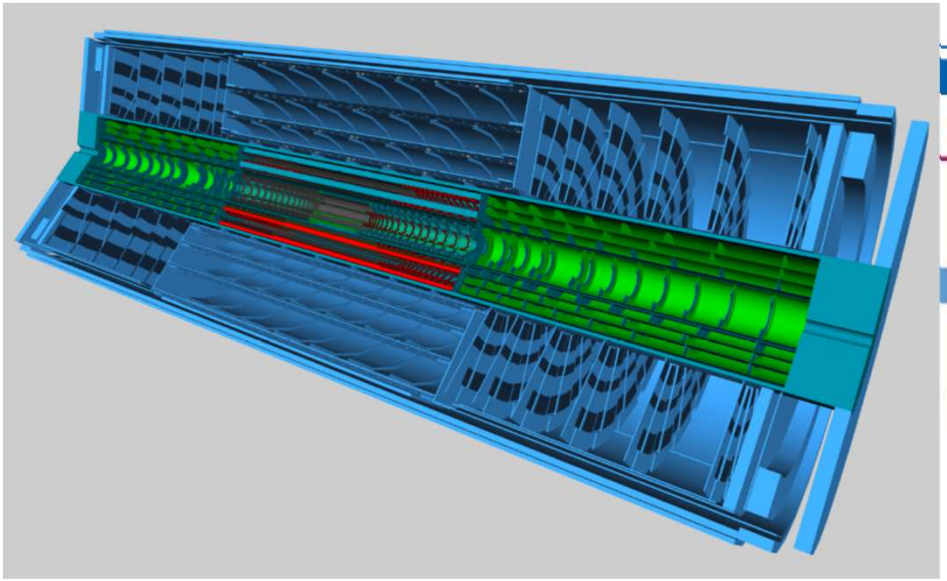
Configuration for Run II and Run III → 2022

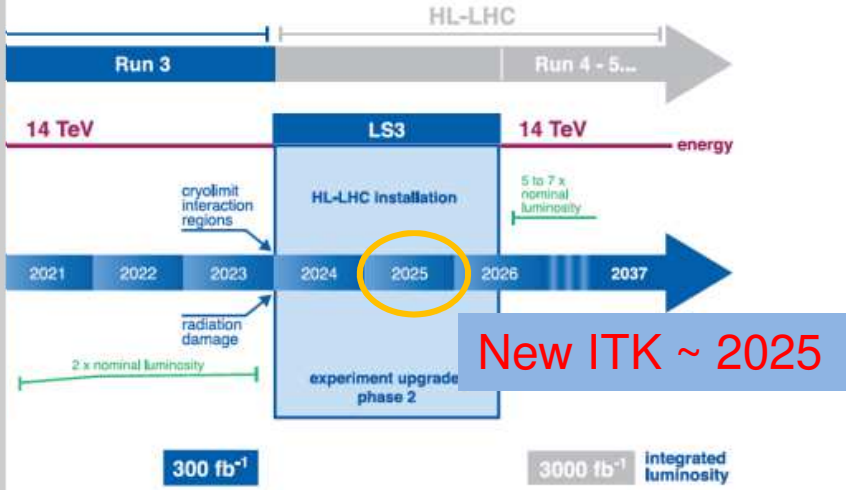
The ITK upgrade

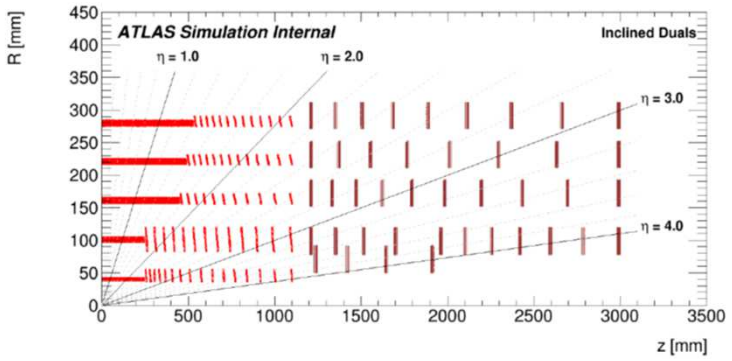


New ITK ~ 2025

The ITK upgrade







- New tracker for HL-LHC based on **silicon only technologies**.
- The new pixel detector will have **5 layers (L0 to L4)**.
- Upgraded hybrid detectors using **RD53 IC** will be used for the first 4 layers.
- Possibility of using **CMOS Depleted Monolithic Active Pixel Sensors** in L4: on-going discussion.
- Finalizing and preparing for **production**.

Pixel volume - Strip volume
Pixel Insertable (L0/1) – Fixed L2/3/4)
Technology different / layer

New IC for hybrid pixel detectors & RD53

RD53: an **ATLAS-CMS** collaboration for the development of **LARGE scale pixel chips for ATLAS/CMS phase-2 upgrades**

Participants: 24 Institutions from Europe and USA:
Annecy-LAPP, Aragon, Bergen, Bonn, CERN, FH-Dortmund, FNAL, INFN (Bari, Milano, Padova, Bergamo-Pavia, Pisa, Perugia, Torino), LBNL, Marseille-CPPM, New Mexico, NIKHEF, Orsay–LAL, Paris-LPNHE, Prague IP-FNSPE-CTU, RAL-STCF, Sevilla, Santa Cruz.
Lead engineer: Flavio Loddo (many slides borrowed below)

Chosen technology: **65 nm**

RD53 goals:

- Detailed understanding of radiation effects in 65nm → guidelines for radiation hardness, and design of a shared rad-hard IP library
- Development of tools and methodology to efficiently design large complex mixed signal chips
- Design and characterization of full sized pixel array chip

Latest news: Design of RD53A

– **RD53A**: to demonstrate, in a large IC, the suitability of the chosen 65nm CMOS technology for the HL-LHC upgrades of ATLAS and CMS.

– Not intended to be a final production chip :

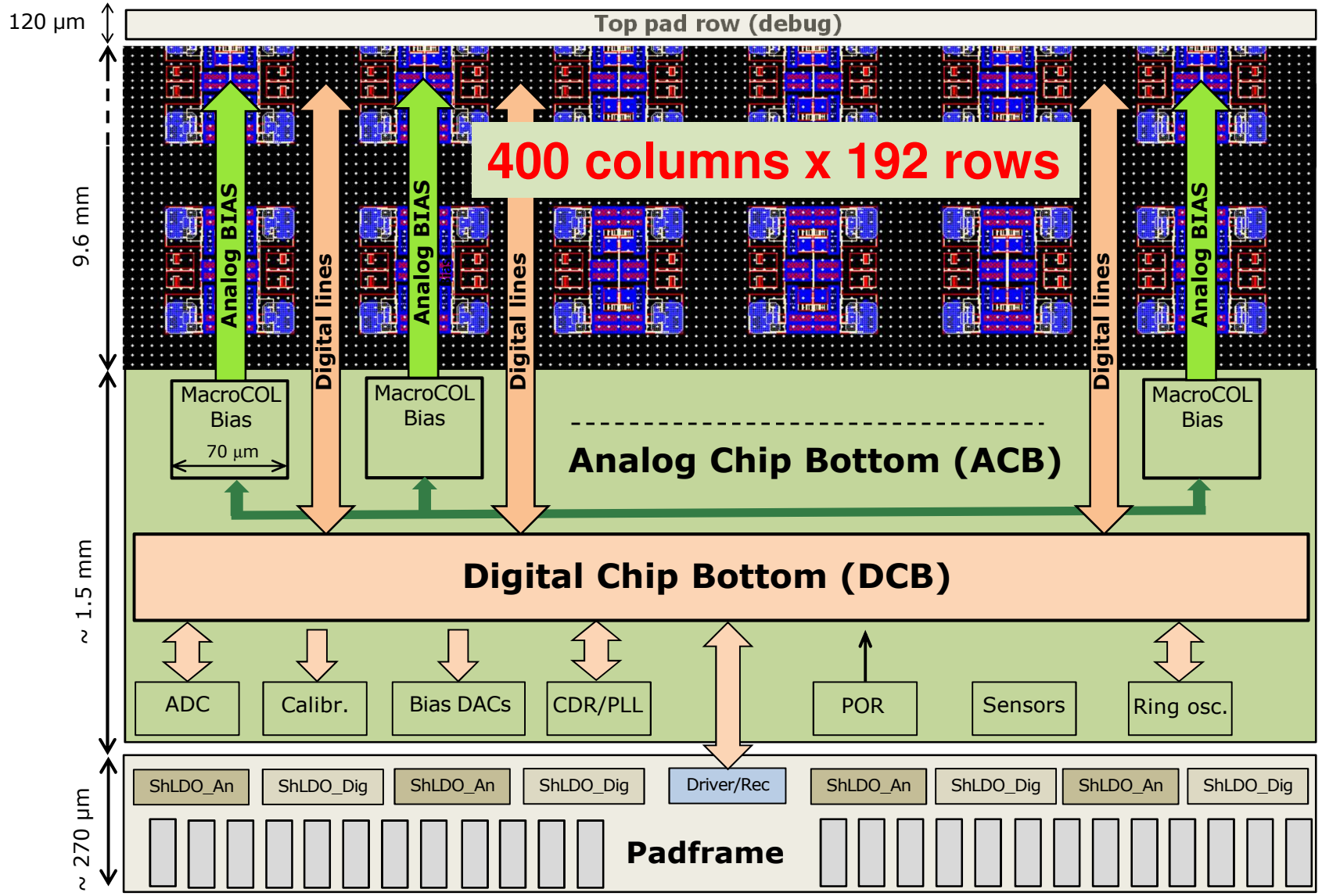
- size: 20 x 11.8 mm^2 (half size of production chip)
- 400 columns x 192 rows (50 x 50 μm^2 pixels)
- contains design variations for testing purposes
- wafer scale production allows prototyping of bump bonding assembly with sensor

  → performance measurement

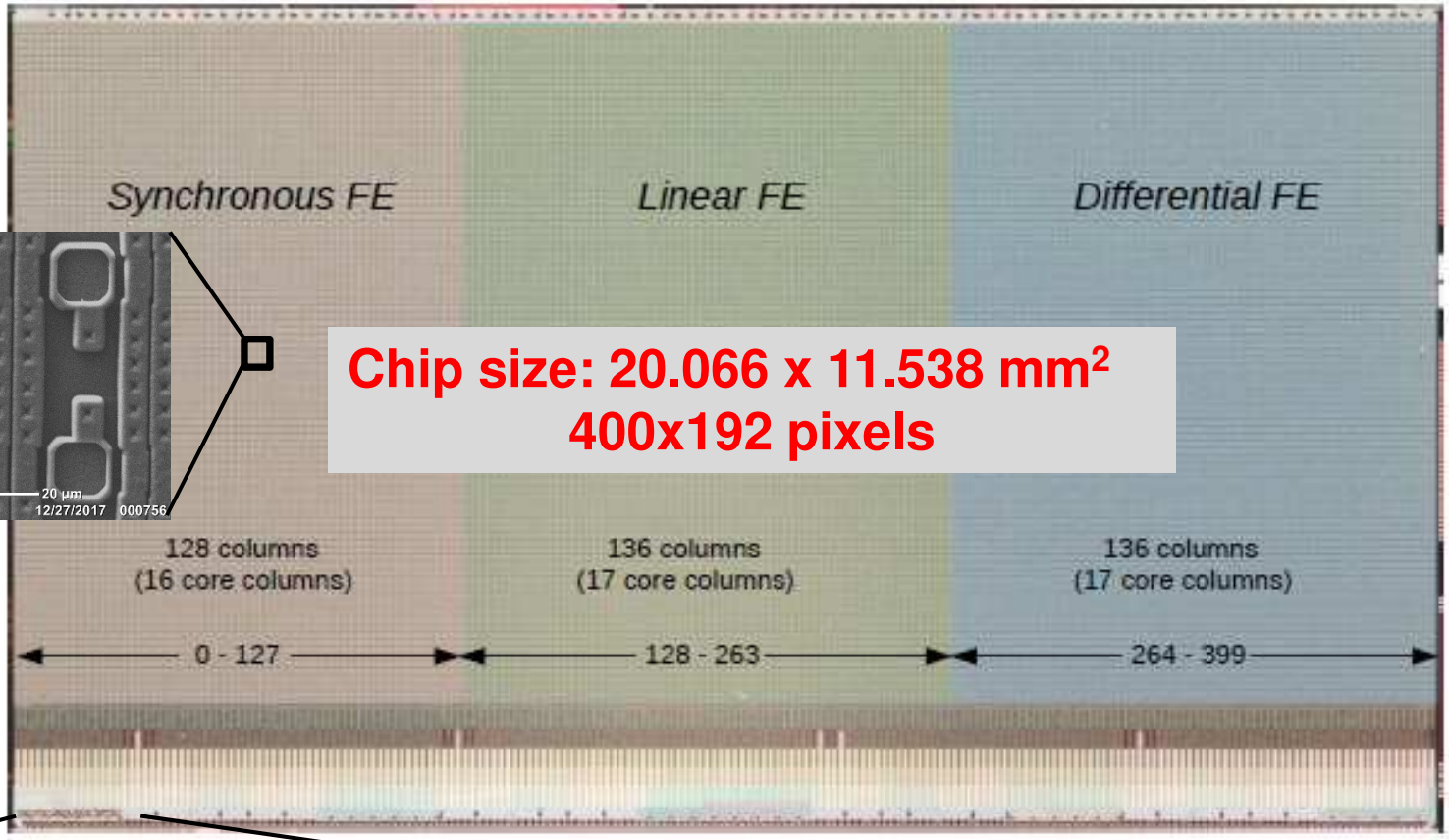
  - will form the basis for production designs of ATLAS and CMS: architecture designed to be easily scalable to a full scale chip

– Submitted at the end of August 2017

RD53A: floorplan

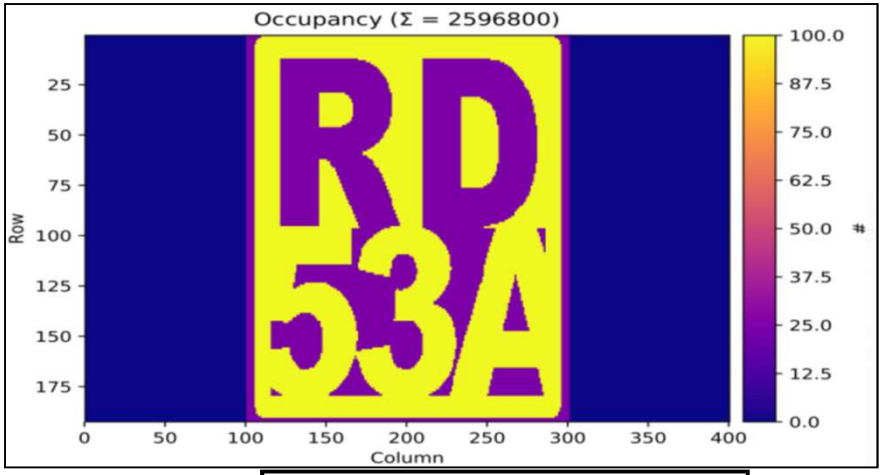


RD53A: 3 analog flavors

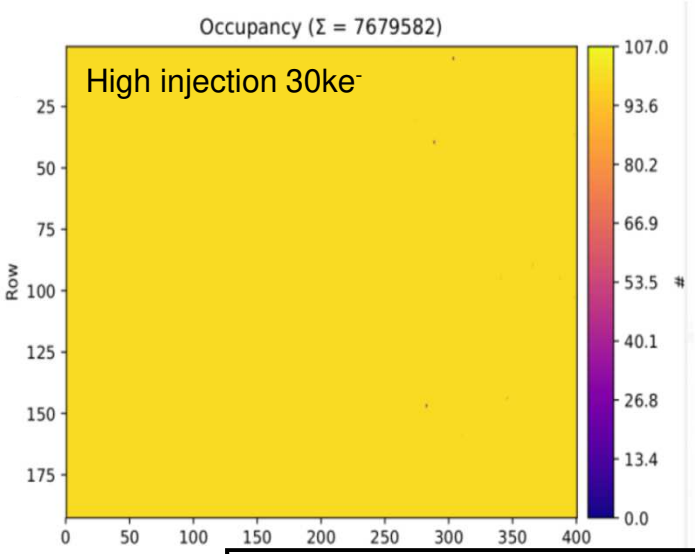


- **Aug. 31, 2017: Submission**
- **Dec. 6, 2017: First chip test**
- **Mar. 15, 2018: 25 wafers ordered**
- **Apr. 13, 2018: First bump-bonded chip test**

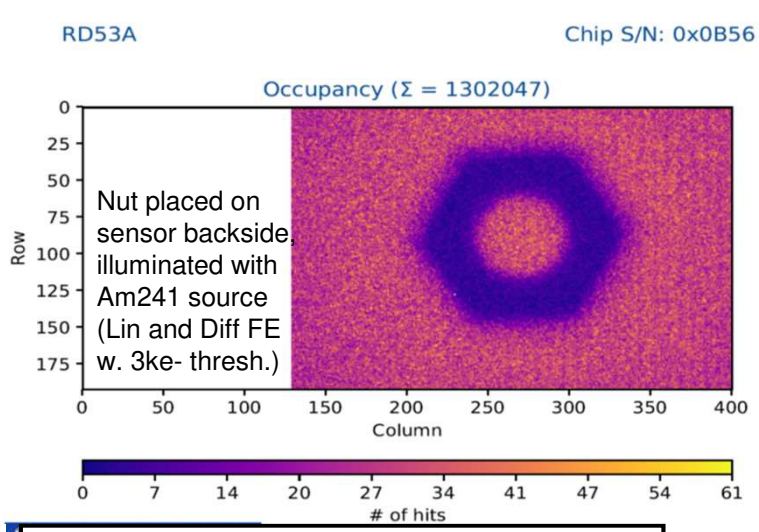
Testing

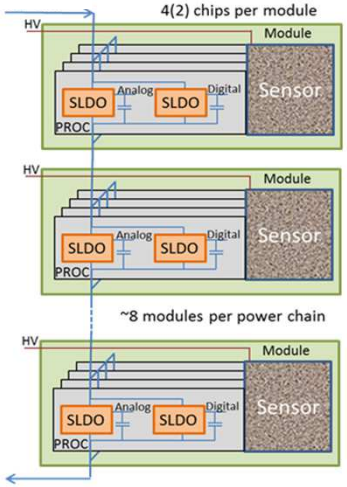


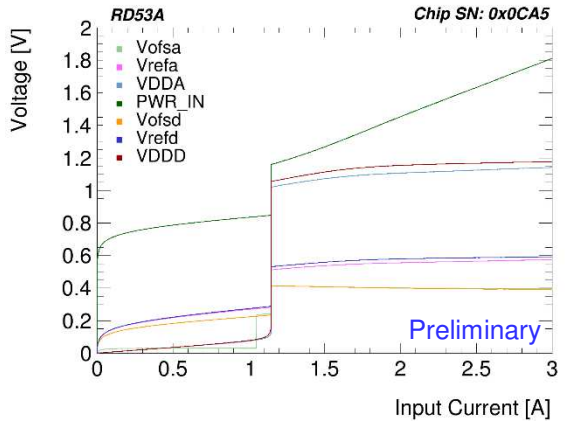
Complex digital scan



All analog flavors responsive







1st assembly in lab mid-April

ShuLDO for Serial Powering

RD53 / 65nm

- The **road to ATLAS Front-End IC** through RD53 collaboration → validated by TDR

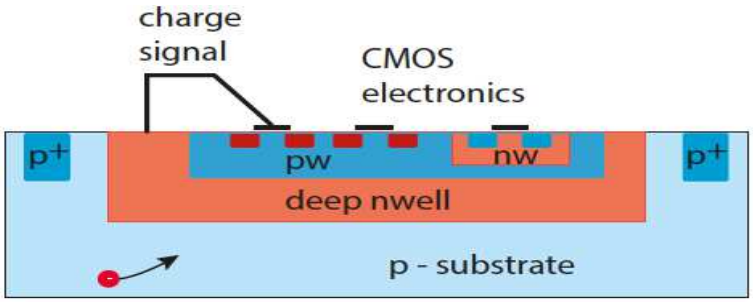
Schedule

- **Until end 2018** : **evaluation** of **RD53A** prototype… many studies needed! Choice of FE among others…
- **RD53B** project **has started**:
  - RD53B library development (fix bugs to few blocks, improve few blocks, etc…). New prototypes (e.g. ShuLDO, band-gap…).
  - Needs for production IC (SEU hardening strategy, 2-level trigger scheme, test scan chain, edge pixels, data formatting/compression…)
- **2019**: Design, fabrication and qualification of **final ATLAS IC**.

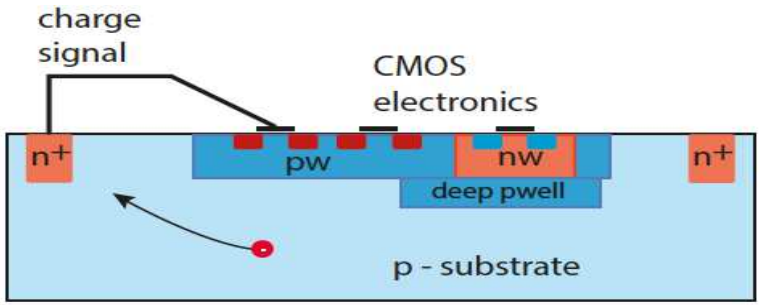
CMOS sensor for L4

Monolithic sensors with electronics all in one!

2 lines of development followed : (a) large electrode design / (b) small electrode design



(a) Large fill-factor



(b) Small fill-factor

- matured over several years
- radiation hardness (TID & NIEL) proven
- rate capability for L4 (and even L3/L2) shown
- timing close to specs

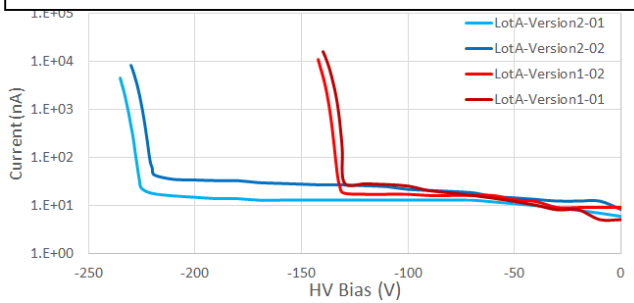
(→ LF / AMS)

- very promising wrt. timing and power
- Vendor already established at CERN
- rate capability for L4 (and even L3/L2) shown
- fast timing due to small C
- radiation hardness -> Sept. 2018

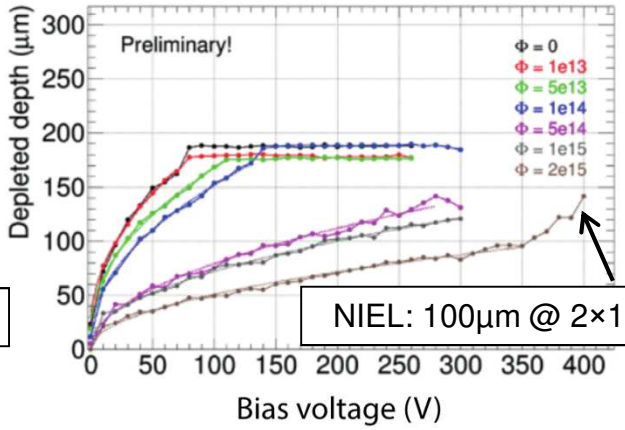
(→ TJ)

Test results -large electrode-

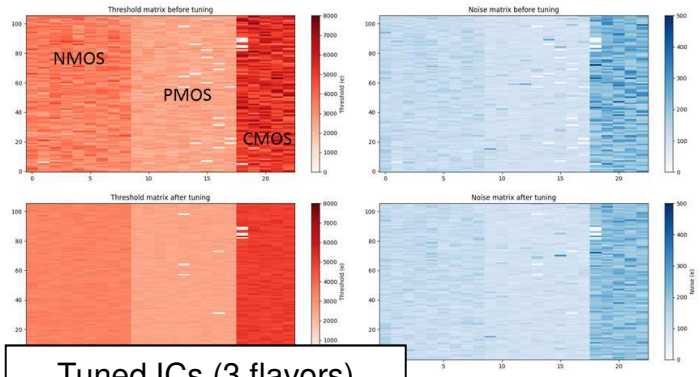
LF new guard-rings w. Shandong Univ



Test board @ PS

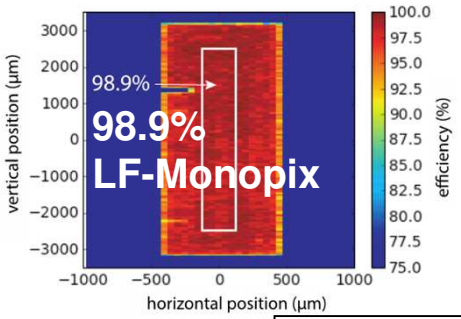


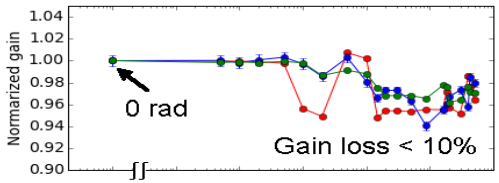
NIEL: 100µm @ 2×10^{15}

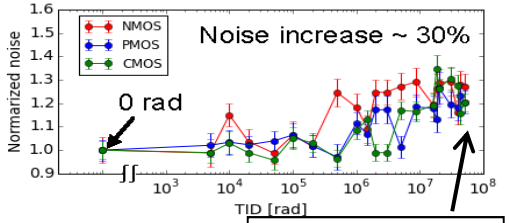


Tuned ICs (3 flavors)

Efficiency @ 10^{15} n_{eq}cm^{-2}

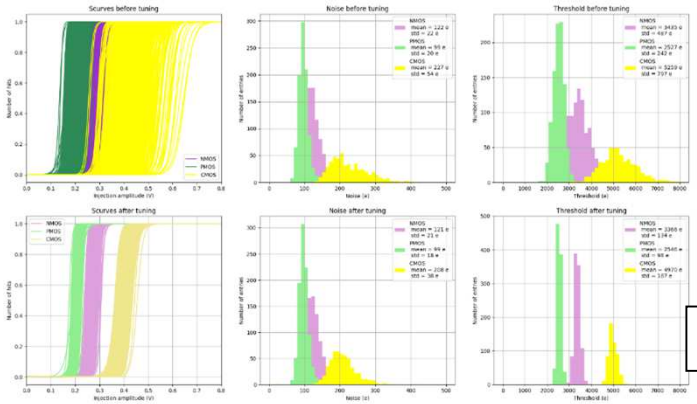




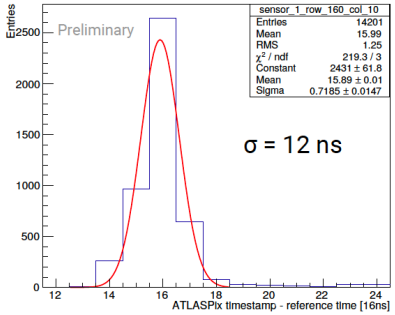


TID 100 MRad

S-curves, thr., noise



Timing (AMS)



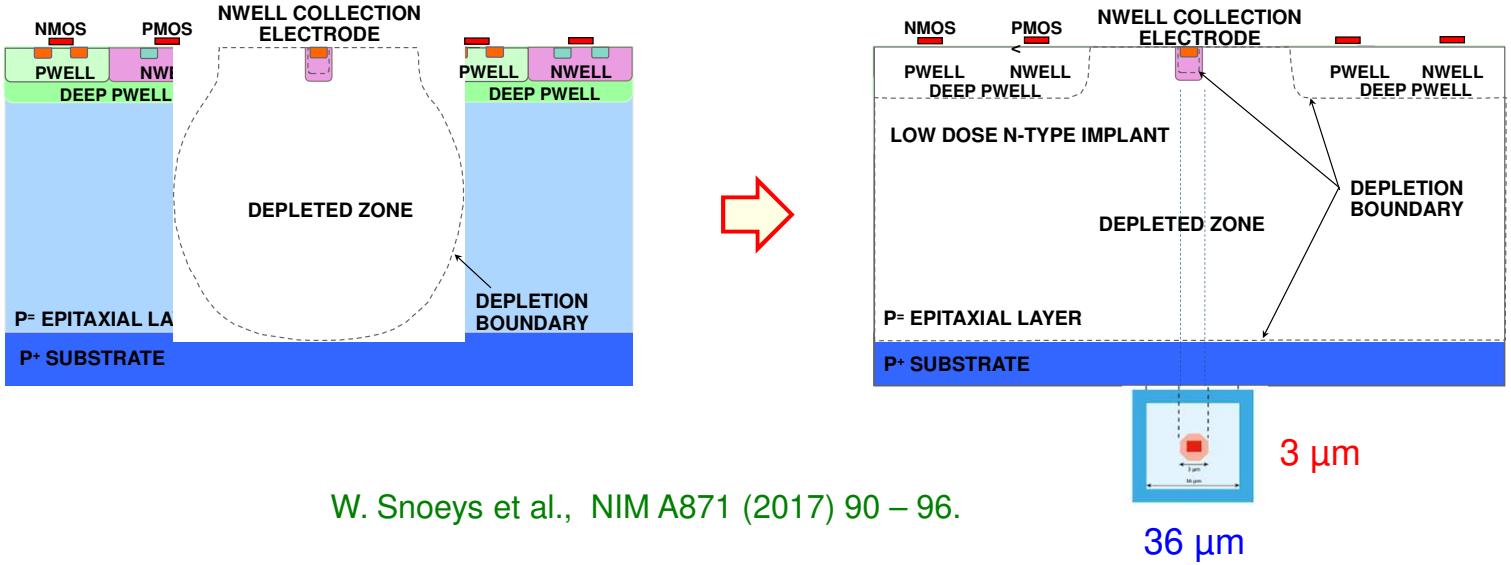
Thesis Jian Liu -Shandong- 2016

TJ process modification

- **TowerJazz** 180 nm CMOS CIS
- deep PW full CMOS in pixel
- epi thickness: 18 – 40 µm
- Design derived from ALICE development
- **Modified process** to improve depletion & lateral E

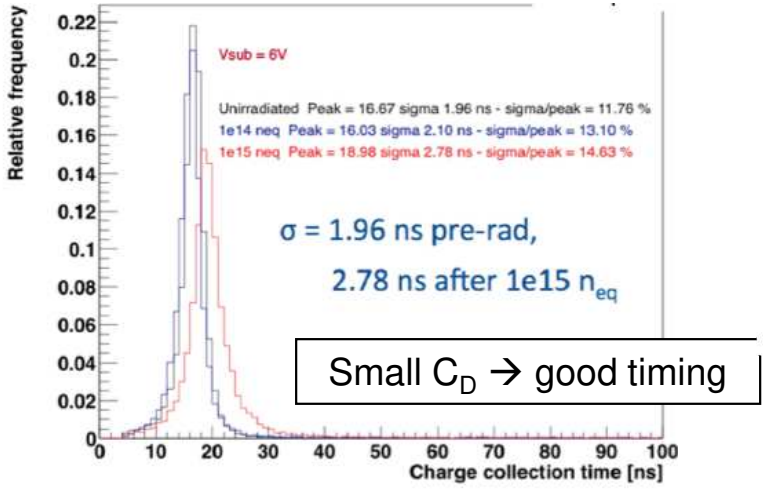
Pixel dimensions:

- 36 x 42 µm^2 pixel size
- **3 µm diameter electrodes**
- Measured capacitance **<5fF**

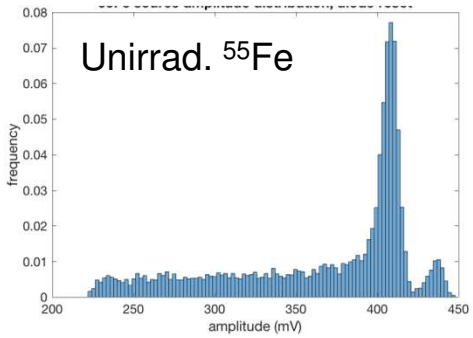


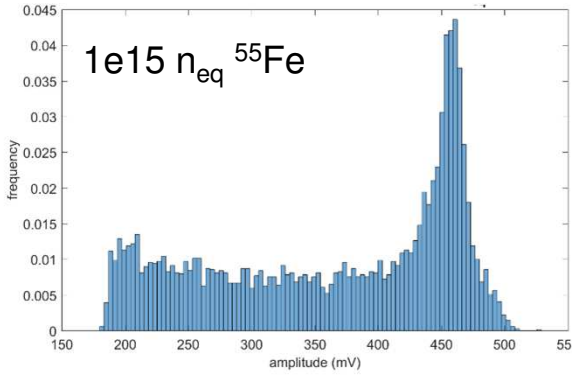
W. Snoeys et al., NIM A871 (2017) 90 – 96.

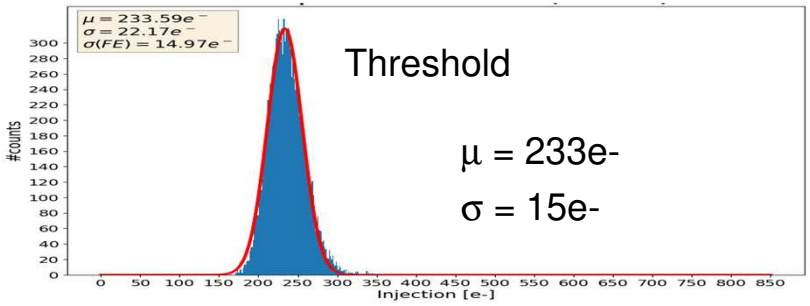
Results -small electrode-

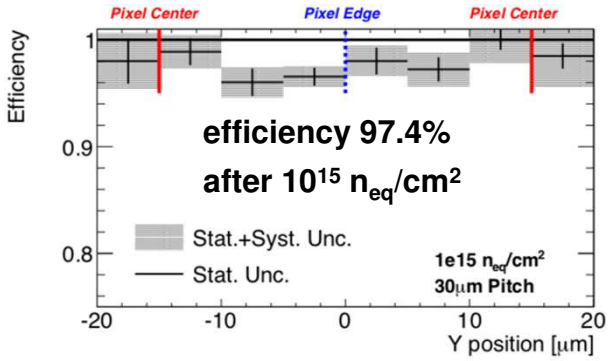


Small C_D → good timing









Efficiency @ 10^{15} $n_{eq}cm^{-2}$

2018 TJ: 2 diff. R/O arch. MALTA & MonoPix

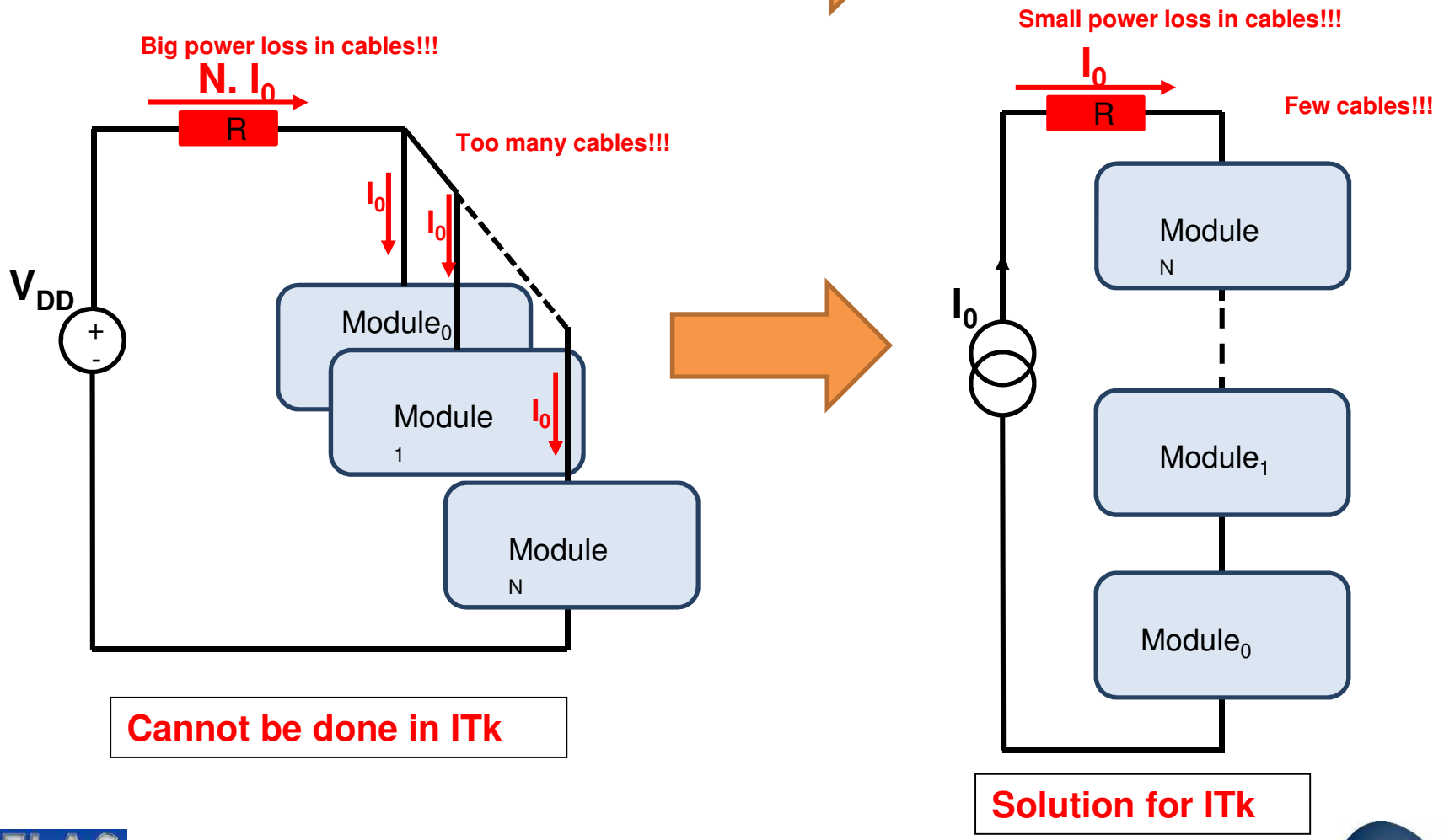
Tests ongoing (lab, beam tests, irradiations):

- small signal 1600 e due to 25 μm epi layer
- but also small ENC ~ 8e- and threshold dispersion ~15 e- due to small C_D

e.g. dvp new blocks: for Serial Powering

Traditional: Parallel Powering

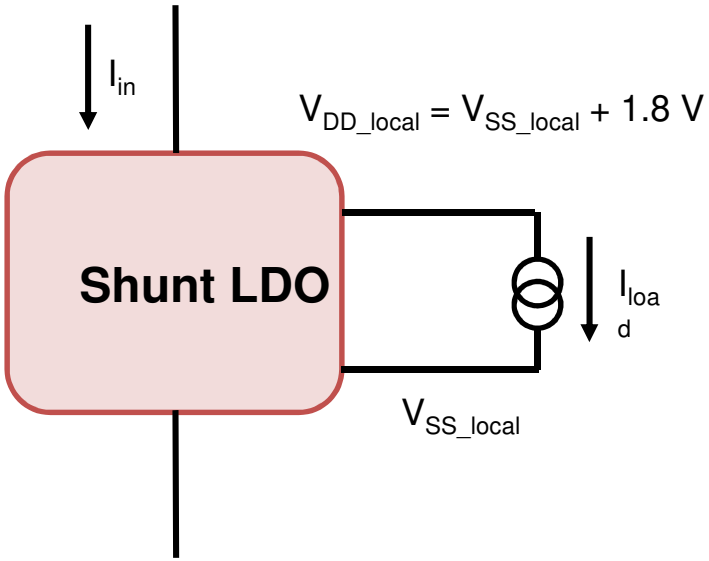
In ITk: Serial Powering



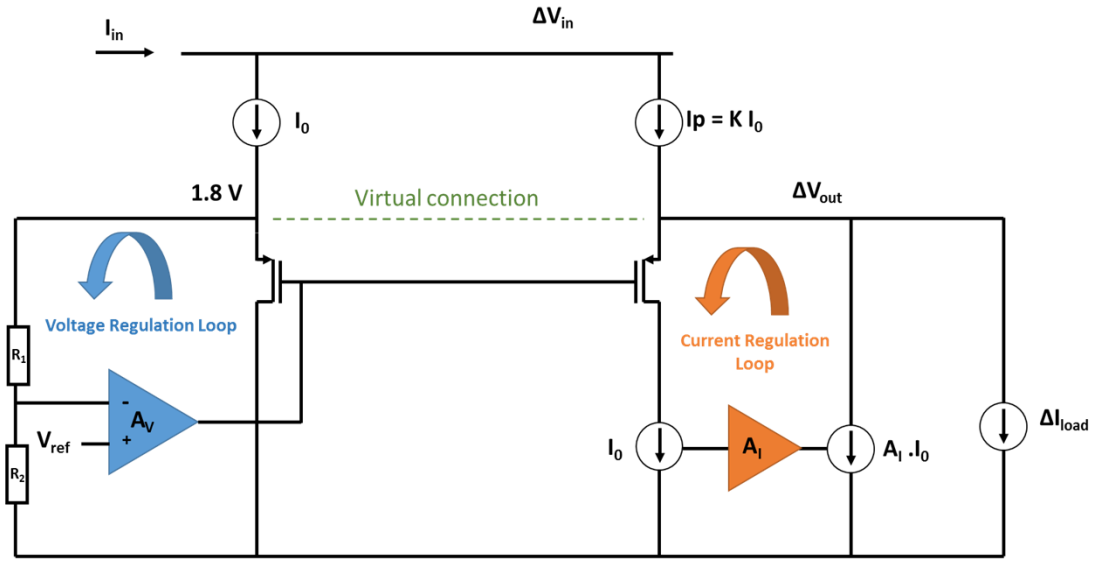
Shunt-LDO en TJ: to power electronics

Shunt Low Drop Out Regulator

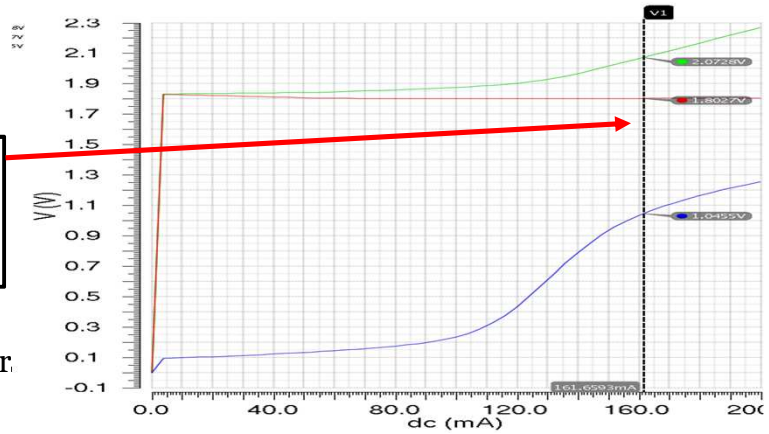
Main idea



Possible solution



For a nominal current (160 lmA), V_{out} is regulated at 1.8V, with a drop out of 200 mV



CMOS pixels project

- **TDR** ATLAS Inner Tracker Pixel Detector now validated
  - Solution **CMOS pixel an option for L4 pixel layer**

Schedule

- **Until fall/end 2018** : Complete **evaluation** of monolithic prototypes
  - ATLASPix, LF-Monopix, TJ-Monopix, TJ-MALTA
  - Feedback for CMOS1 prototype
- **Until end 2018** : **CMOS1 Design critical blocks**
  - Integration of features needed for Module prototype
  - Address Powering and data aggregation and transmission issues
- **Spring 2019** : **Submission of CMOS1**
- **2019: Design of final CMOS IC**

Collaboration with IHEP post-doc in CPPM for 2019
Zhao Mei's application approved
-ATLAS R&D, CEPC R&D-

Conclusion

- **Important developments have occurred this last year for ATLAS pixel ITk detector:**
  - Front-End: **RD53A** submitted and tests very positive so far
  - TDR validated with **CMOS sensor** as a possibility for the pixel L4
  - Many other aspects have seen tremendous progress (mechanics, production model, …)

- We have **benefited from ACC** collaboration support and we look forward the continuation of this fruitful collaboration with our Chinese colleagues → HL-LHC, CEPC, FCC…