SMART

A new electronic design @ GAP/GANIL

Sfp connectivity and Microtca for Advanced Remote Trigger

Smooth Upgrade
of CENTRUM and GTS
towards a new time stamping system
with trigger option
« Made in GANIL »

For all GANIL needs
and other collaborations AGATA, GES(GET+), ...
if interested ...

Slideshow plan

1. Present status / Motivations
2. Items retained / deleted
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4. Global architecture
5. Design strategy
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1 – Present status
Motivations

- ✓ Difficult to propose CENTRUM coupling in 2018
  coupling easy to use but VXI based without any trigger features

- ✓ GTS-V3: custom mezzanine with components under obsolescence (MICTOR connector: 24 weeks for delivery, …)
- ✓ Available quantity limited and dedicated to existing digitizers (numexo2)
- ✓ GTS/TP: complex firmware with many files written or modified by a large number of engineers over the last 10 years and not always documented (→ reverse engineering)
- ✓ Need a powerful solution easy to use/deploy by any GANIL engineer/physicist or any other interested laboratory, all that in the mid term
- ✓ New solution should be used with any kind of FPGA based target board with minimum requirements (1SFP connector or AMC port - 1MGT)

2 – Items retained / deleted

- ✓ Providing same key information:
  - ➔ TS 48 bits/10ns and 32 bit event number
- ✓ Unique 100 MHz clock for synchronization (CDR)
- ✓ Transmission @ 2Gbit/s with 8B/10B encoding towards digitizers and new boards to synchronize …
- ✓ Connectivity and data transmission media saved
  - ➔ SFP connectors, optical transceivers, fiber and/or copper cords
- ✓ Architecture foreseen, « sized » for trigger option
- ✓ TS alignment managed by the new solution, able to handle boards without or with fine delay clock adjustment (like GTS LEAF with delay line & slow control)
- ✓ Internal GTS/Trigger processor protocol abandoned

3 – New elements

- ✓ Use of µTCA standard fully mastered by GANIL/GAP (IN2P3 rec.)
  - ➔ Double / Full size AMC form factor (carrier)
- ✓ Integration of «**S**ystem **O**n **M**odule » durable industrial solution as opposed to the kit reducing costs, engineering time and design errors
- ✓ Use of « lightweight » but robust protocol adapted to small packets of data that have to be transmitted efficiently
- ✓ Transmission @ 4Gbit/s - 8B/10B encoding between new boards (HUB/ROUTER), main alignment done in the FPGA
- ✓ Use of QSFP connectivity to increase copper/fiber links density
- ✓ Build with Xilinx Zynq FPGA (ARM processing/16 Multi Gigabit Transceivers) and the latest Xilinx Zynq UltraSCALE+ (if AMC13)

4 – Global Architecture (terminology)

Only one board ➔ but 2 functions:
- HUB
- ROUTER

16 ports

15 ports

Up to 240 digitizers synchronized by 17 AMC's housed in 2 µTCA shelves (120 equivalent GTS V3)

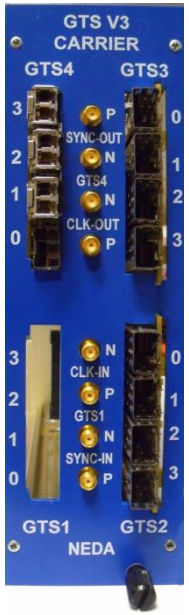
Possibility to have different sizes of FPGA for the same SOM (hub or router)

5 – Design strategy

Phase 1 - Phase 2 …

- ✓ AMC (hub/router)
  - ➔ Triggerless solution validation (CLOCK - TS/EVTNUM)
- ✓ AMC (hub)
  - ➔ Trigger option « de base » (functions/performances vs resources)
- ✓ If more important needs, AMC 13 development with «System On Module » based on UltraScale+ MPSOC for higher trigger level (GTS TP+ type, trigger on hit pattern with GPU, …etc.)
- ✓ In this case, porting of the initial solution at up to 420 synchronization/trigger links (≈ 2xPhase1)
- ✓ Other possibility with on the shelf MPSOC AMC (Vadatech AMC580 – **10000$**)
- ✓ Specifications / Presentations / Documentation
- ✓ Mass production / Valorization

6 – Project summary



- ✓ System design fully mastered by GANIL/GAP (HW/FW/eSW/GUI)
- ✓ 15 links/5000€ vs 9 links/9000 € (4 GTS/1NIM carrier)
- ✓ 2 years for this first coupling solution HUB/ROUTER prototype
- ✓ Keeping all existing connection elements
- ✓ Use of latest or ultra latest SOC FPGA in order to guarantee a 15/20 years durability
- ✓ Open system also addressed to future developments/external labs
- ✓ GAP project (a minimum of 4 people involved…)
- ✓ Internal protocol GTS/TP no longer supported

7 – Phase 1

From few links

4 ports (TX/RX) - QSFP↔ 4SFP
Copper (TurboTwin): 3m (~100€)
Fiber (OM3): 300m (~300/400€)

Up to 240 links of coupling/trigger …

First examples of use in terms of « Physics » channels number:

-3200 ch. Based on a 16 ch. DIGITIZER (NUMEXO2 type)

- 12800 ch. if coupling 64 ch. ASIC FE board (SAM type - 1 AGET)

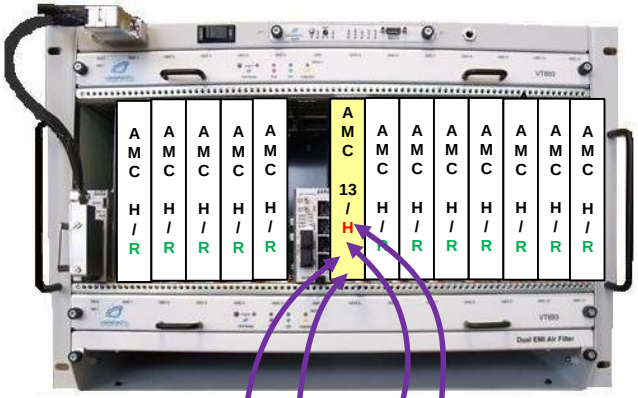
- 51200 ch. if coupling 256 ch. FE ASIC board (GET/ASAD type - 4 AGET's)

Is the system scalable ?

Yes, it is scalable !

8 – Phase 2
Topology A

"AMC13" - MPSOC (Zynq UltraSCALE+)
12 backplane ports +
16 front panel ports (with 4 QSFP)
➔ 28 ports to feed "ROUTER" modules



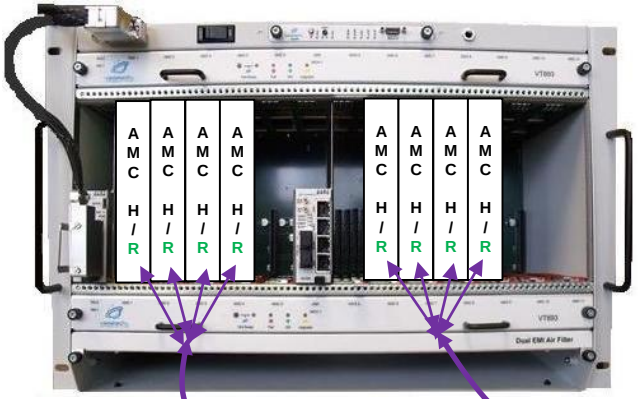
Other examples of use in terms of « Physics » channels number:

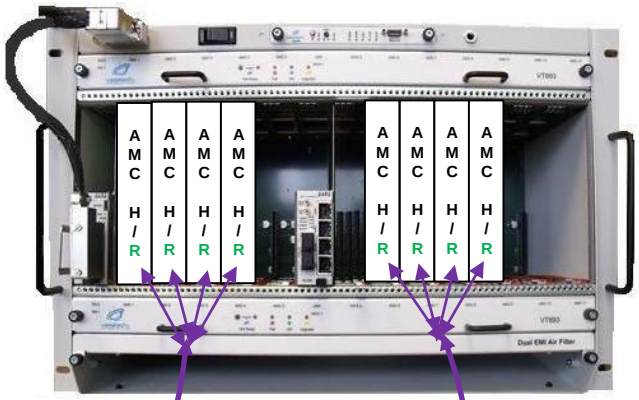
-6400 ch. based on a 16 ch. DIGITIZER (NUMEXO2 type)

- 25600 ch. if coupling 64 ch. ASIC FE board (SAM type - 1 AGET)

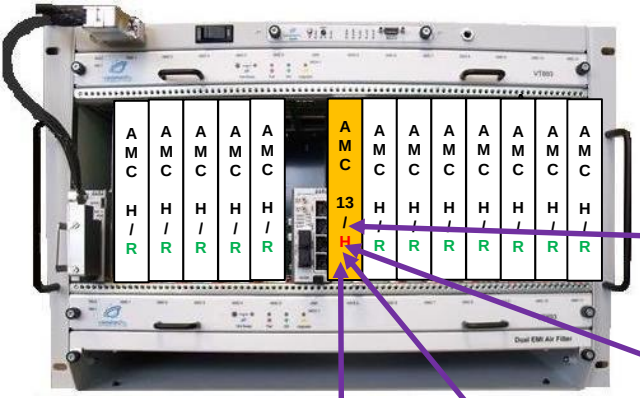
- 102400 ch. if coupling 256 ch. FE ASIC board (GET/ASAD type - 4 AGET's)

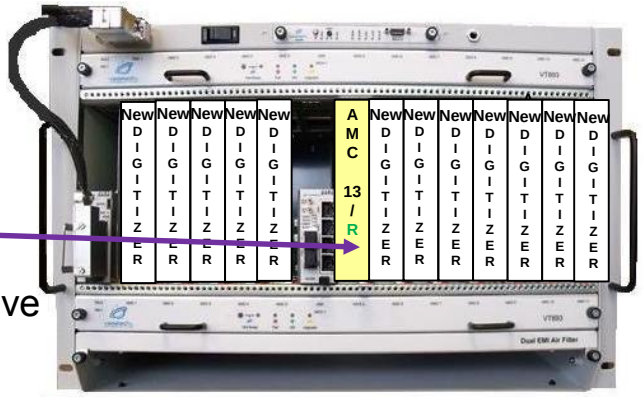
≈ up to 420 coupling/trigger links …



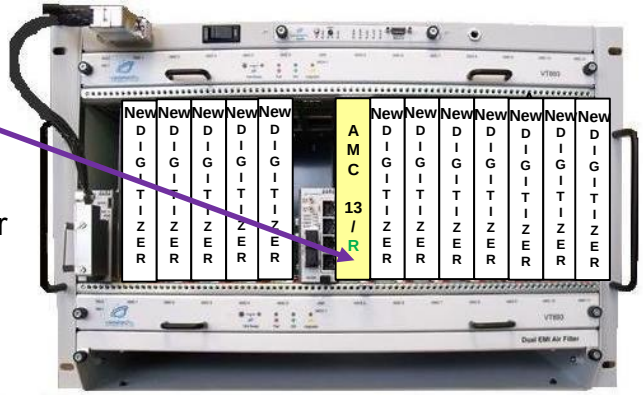


9 – Phase 2
Topology B

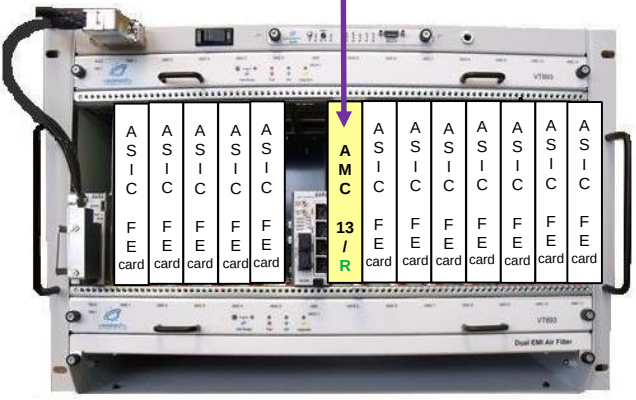


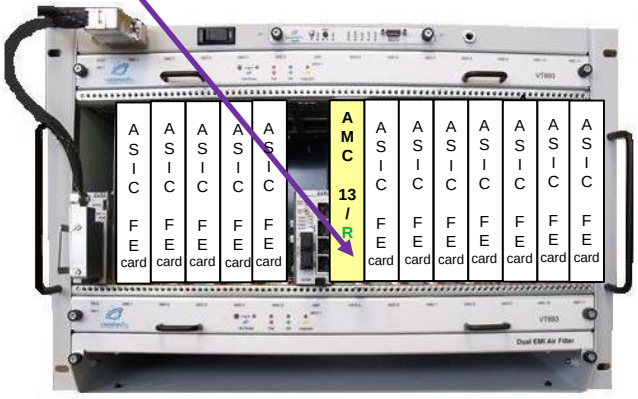


Synchronization/Trigger
of µTCA.0 (.4) boards that don't have
or can't have front panel SFP
connection



QSFP↔ QSFP links/copper or fiber
4x4Gb/s by inter-crate cord





AMC 13 is also used here as
a simple "backplane" router
minimizing cabling to µTCA
boards

Thank you for your attention