

AGATA – EDAQ_PH2 Firmware

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Introduction



- Status since last year
- Ongoing development
- Plan

Status since last year

■ Firmware development

- PreProc: work in standby, nothing done this year
- TriggerProcessor in VC707 kit (Ganil): slow-control-by-IPBUS plug-in + lots of diagnostics for debug purpose

■ Participated in some meetings w/ others contributors

- Town meeting in Valencia in June 2018
 - ✓ Defined a common demonstrator (DEMO_EDAQ_PH2) based on evaluation kits from Xilinx + a timeline
 - Eg. A KC105 board was purchased & received in June at IPHC

■ Was mainly involved in CMS activities (Upgrade Phase 1 & 2)

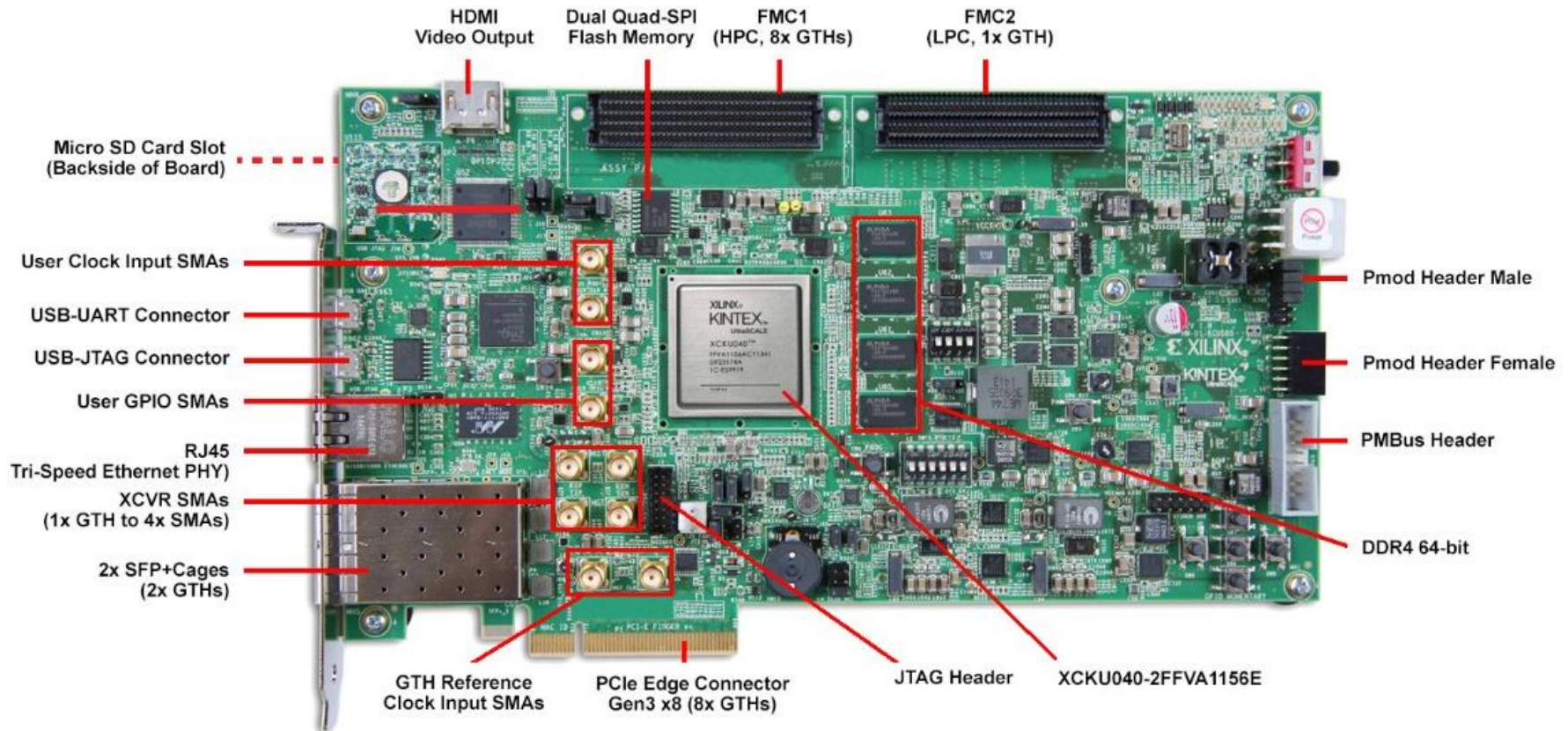
- CMS upgrade Phase1 (production phase)
 - ✓ Still minor dev for heavy ions run, before a long shutdown of LHC for 2 years
- CMS upgrade Phase2 (system tests phase)
 - ✓ This week, it was agreed with my lab (Technical Director, CMS group from IPHC) to leave this activity for a while; at least for one year
 - Except for CMS local needs (laser setup, irradiation setup via Cyclotron)

■ I will be quasi full time for AGATA dev in the coming months

Ongoing development

■ Migrate/Replicate STELLA project (24chan/125MHz/FMC112 from Abaco)

➤ From Kintex-7 uTCA board to Kintex-Ultrascale dev board (KCU105)



Ongoing development

- This work started 2 weeks ago
- Good mean to exercise & play with Ultrascale-series from Xilinx
 - Technology different from 7-series (and 6-series)
 - ✓ Clocking architecture
 - ✓ Primitives & IP Cores : some changes
- Status of the migration
 - Integration of blocks step by step
 - GbE + IPBUS for SlowCtrl & Data transfer to PC: done and fully functional
 - SERDES block (compliant w/ FMC112 ADC Data): done but to be tested
 - DSP blocks for algos (Trigger, MWD): done but to be tested
 - FIFO primitives & BRAMs for Data buffering: some issues!!!
 - ✓ Size seems limited for a Clock Region of the FPGA matrix (not the case in Kintex-7)
 - READOUT block and I/F with GUI via GbE/IPBUS
 - ✓ Need a DDR4 controller I/F instead of DDR3
 - ✓ Maybe replaced by simple FIFO readable by IPBUS

Ongoing development

Migration is not so trivial

- Example of error got from Vivado after PAR concerning a FIFO instantiated for buffering data

The screenshot displays the Vivado IDE interface. On the left, the Hierarchy and Source File Properties panels are visible. The Hierarchy panel shows a component named 'ipcore_big_buffer_INST : ipcore_big_buffer_38'. The Source File Properties panel shows the file 'ipcore_big_buffer_384b.xci' is enabled.

The main workspace is divided into two panels: Synthesis and Implementation. The Synthesis panel shows a status of 'Complete' with 2 errors and 2327 warnings. The Implementation panel shows a status of 'Failed' with 101 errors, 1 critical warning, and 200 warnings.

The Messages window at the bottom shows a list of errors. The selected error is:

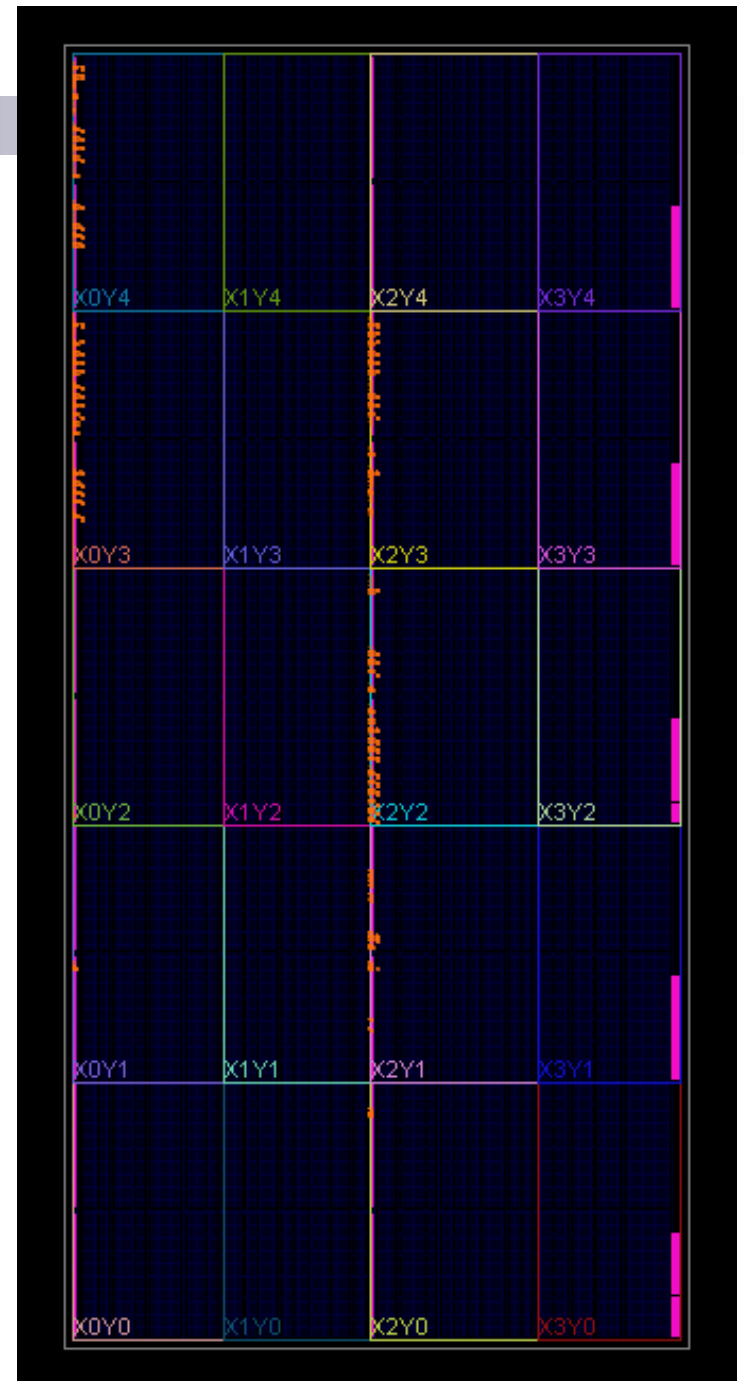
```
[DRC CASC-49] Cascade FIFO36 crosses rbrk: The FIFO36E2 cell dsp_instipcore_big_buffer_INST/U0/inst_fifo_gen/gconvfifo_rf/gbi_biv8_fifo.blk/rst_val_sym.gextw_sym[10].inst_extd/gmult_prim.gbi_chain.gp1[10].gbi_middle.mid_inst_prim/gf36e2_inst.sngffo36e2 is cascaded in series to expand the FIFO depth, however the cascade connection crosses a Clock Region. The use of the CASCADE_ORDER set to MIDDLE or LAST in this location causes a potential hold violation that cannot be corrected and so creates an invalid timing situation. Please take steps to ensure placement of the cascaded FIFO remains inside a single Clock Region or else choose a different implementation style for this FIFO in order to prevent the need for cascading across a Clock Region or the use of this pin. (99 more like this)
```

Below this, another instance of the error is shown:

```
[DRC CASC-49] Cascade FIFO36 crosses rbrk: The FIFO36E2 cell dsp_instipcore_big_buffer_INST/U0/inst_fifo_gen/gconvfifo_rf/gbi_biv8_fifo.blk/rst_val_sym.gextw_sym[10].inst_extd/gmult_prim.gbi_chain.gp1[11].gbi_middle.mid_inst_prim/gf36e2_inst.sngffo36e2 is cascaded in series to expand the FIFO depth, however the cascade connection crosses a Clock Region. The use of the CASCADE_ORDER set to MIDDLE or LAST in this location causes a potential hold violation that cannot be corrected and so creates an invalid timing situation. Please take steps to ensure placement of the
```

Ongoing development

- Like the tool doesn't accept big size FIFO crossing adjacent Clock Regions from the FPGA matrix
 - ✓ Need to understand why

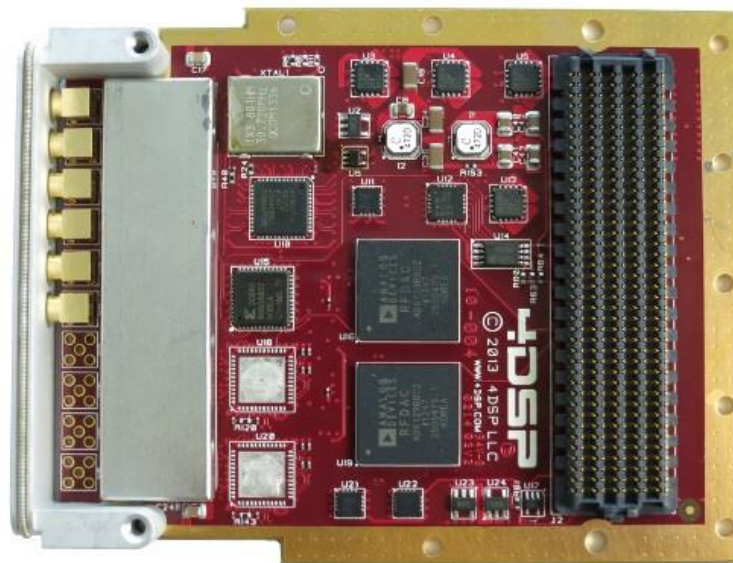


Ongoing development

- The migration is well advanced
 - Need still few weeks to complete it
 - Then check the stability of the algorithms (especially MWD) via the STELLA GUI from Marc Richer
 - ✓ Via simple generator and CAEN Emulator
 - ✓ If not stable, try to fit the IPCores to get stability
- When completed, this local setup will be a good basis
 - For the next steps of the dev
 - ✓ DEMO_EDAQ_PH2
 - ✓ EDAQ_PH2
 - For testing new algorithms without changing the s/w
 - ✓ Keep the features (histogrammer and traces viewer) of the GUI
 - ✓ Control new parameters (if needed) by simple IPBUS python scripts
 - For estimating the FPGA occupancy (by disabling the Readout part)
 - ✓ Case 24 channels
 - ✓ Case 36 channels via some generic parameters (duplication of some channels)
 - ✓ Estimation to be compared view estimation done by Javier

Plan

- Continue the current migration STELLA_KCU105
- For a better dev and monitoring:
 - Purchase the FMC DAC FMC216 from Abaco
 - ✓ 16 D/A 16-bit 312.5Msps
 - Allows direct analog inspection
 - Need to implement a piece of f/w
 - Useful
 - ✓ For testing more rapidly and more easily the algos
 - ✓ Why not, testing production cards (digiOpt12, IDM, etc)



Plan

■ From this basis, start next steps

- Go to DEMO_EDAQ_PH2
- Go to EDAQ_PH2 (production)
 - ✓ Merging of different blocks

■ For that

- Reuse functional blocks from STELLA_KCU105
- Add synchro/timing features based on previous designs
 - ✓ GTS leaf f/w from Numexo (Ganil)
 - G. de France informed A. Boujrad to get it
- Add features of Control Card (need more infos on that)
- Add the block (IDM channels receiver) from Valencia
 - ✓ Possible on KCU105?
- Purchase the FMC cable identified by collab. for connecting the kits of the DEMO_EDAQ_PH2
 - ✓ DEMO_EDAQ_PH2 = {IDM + PP + STARE} on kits
 - ✓ To receive channel data from IDM
 - ✓ To Transfer data to STARE
- Define transfer protocol, registers tables, data formats & acquisition modes (links with s/w by IPBUS), diag, etc...