R&D on electronics: Introduction

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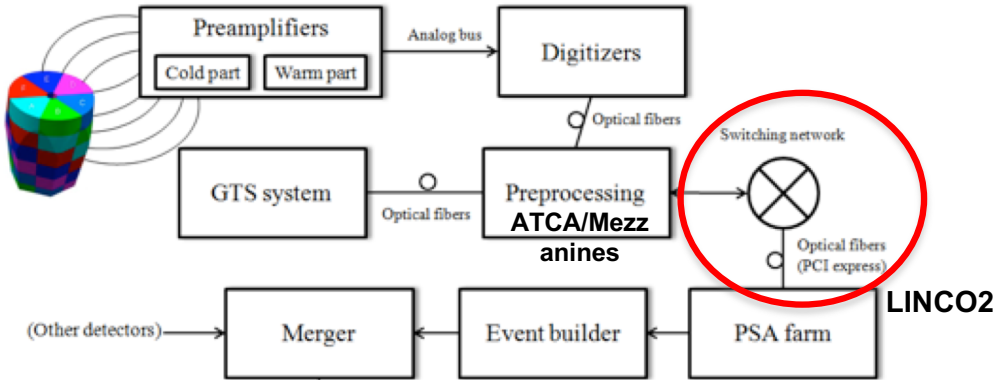
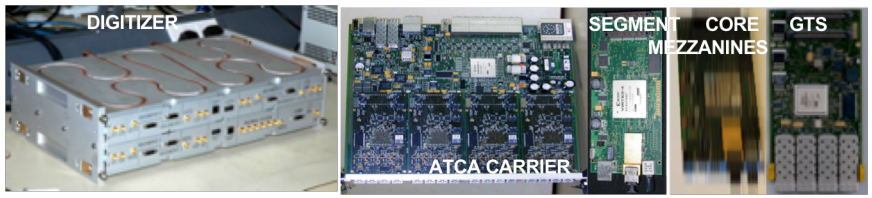
Outline

- AGATA Electronics Evolution
- Found issues
- Guidelines for R&D initiative
- On going Technical Proposal

AGATA Electronics Evolution

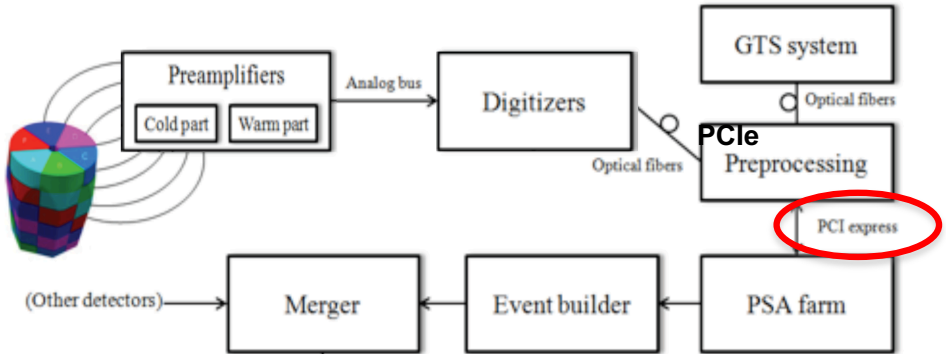
AGATA Electronics Phase 0/Early1 (23-25 ch available)

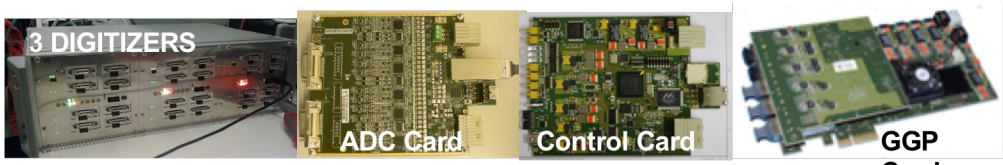




IPHC Strasbourg Uni.Liverpool STFC Daresbury IPNO, CSNSM-Orsay INFN-Padova

AGATA Electronics Advanced Phase 1 (13 ch available)





INFN-Milano INFN-Padova INFN-LNL IFIC-Valencia ETSE-Uni-Valencia

New production batch of Adv. Phase 1 electronics
10 channels + spares

We need to go to 60 channels

Known issues

Issues suffered in AGATA Electronics evolution

At least:

- Component obsolescence (transceivers, IC, …)
- Compatibility issues, i.e. GGP and workstations
- Difficulties in HR for maintenance and repairing
- Costs increasing for old components
- …

So …

Seemed not sensible to produce more AdvPh1 electronics.
Better to start an new R&D in view of AGATA 4π

Guidelines for the R&D

We had guidelines from experts for the AdvPh1 (2012) which could be extended to the new R&D. Basically,

- **Improve integration**
- **Reduce production and maintenance costs**
- **Keep backward compatibility of each generation FEE and with GTS.**

FEE Group discussions identified the following lines of R&D

1. Possibility of **higher integration and power consumption reduction** in the AGATA **core and segment pre-amplifier**. Exploring the **ASIC technology** for the AGATA pre-amplifiers. **(Far future 2025)**
2. Possible **integration of the Digitizer and the ADC** in the spirit of the Digital Pre-amplifier module. **(Not so far future)**

Guidelines for the R&D

FEE Group discussions identified the following lines of R&D

3. **Improvement in the Digitizer ENOB** by using **16 Bit FADC's (or beyond)**. This will allow **to enlarge the energy range** without endangering the energy resolution, specially in the high gain section that might go easily to an 8 MeV range. **(Sliding Scale implementation)**
4. Possibility of increasing the ENOB **using more complex pre-processing algorithms on the evaluation of the baseline**.
5. Possibility of **higher integration in the Digitizer control Card** for remote settings of the Digitizing cards. **(Included)**
6. Pre-Processing improvements: considering the **possibility to integrate the pre-processing of a full cluster in a single card. (Discarded)**
7. Study of the **possibility to locate Digitizer an pre-processing electronics together in the neighbourhood of the AGATA Clusters**, using short links and avoiding long optical fibers. **(Included)**

Guidelines for the R&D

Lines of R&D cont'd

8. **Improvements in the GTS protocol** increasing the **number of leaves** in the tree and possibly defining **"qualifier bytes"** for complex triggers. **(Not at this stage)**
9. Development of the **Hardware and Software trigger processor** able to cope with the necessities of AGATA and all complementary instrumentation beyond Phase 1. **(Bases settled)**
10. Exploring the **possibility of using Ethernet capacity** to transfer data from experimental hall to the computer room **avoiding dedicated interfaces**. **(Included)**
11. **Explore if some high level processing algorithm can be moved** from the FPGA to computer farm. **(Contemplated)**

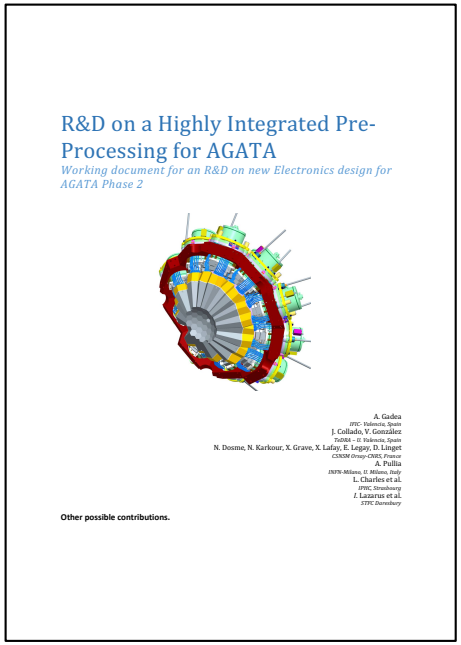
After **January 2016** Town Meeting on R&D for AGATA Electronics, the **AMB and ASC encouraged the development of a medium term solution for processing an ATC and with Ethernet readout**, while **long term developments with ASIC (Digital Pre-amplifiers)** shows technical difficulties that **need further development**.

On going Technical Proposal(*)

Proposal objective: to build a scalable and stable Back End Electronics and DAQ (Electronic Data Acquisition) system for AGATA beyond phase 1 and track the best technical solutions for the full 4π array

Important issues

- Interface between front end electronics and servers should **not rely on any specific hardware interface**.
- Simplified and autonomous electronic modules to **ease maintenance** and **minimize impact of possible rework due to obsolete components** in future.
- **Highly integrated solution** to ease the installation in experimental area.
- **Readout** based on **high bandwidth network technology** (up to 10 Gb/s per crystal).
- **Stable and scalable architecture** of the AGATA BEE&DAQ architecture (for which the necessary performances must be fulfilled from 45 up to 180 crystals)


R&D on a Highly Integrated Pre-Processing for AGATA

Working document for an R&D on new Electronics design for AGATA Phase 2

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CSNSM Orsay-CNRS, France
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IPHC, Strasbourg
I. Lazarus et al.
STFC Daresbury

Other possible contributions.

(*) Information from the working document for the R&D on electronics for AGATA Phase 2.

On going Technical Proposal

Important issues (cont'd)

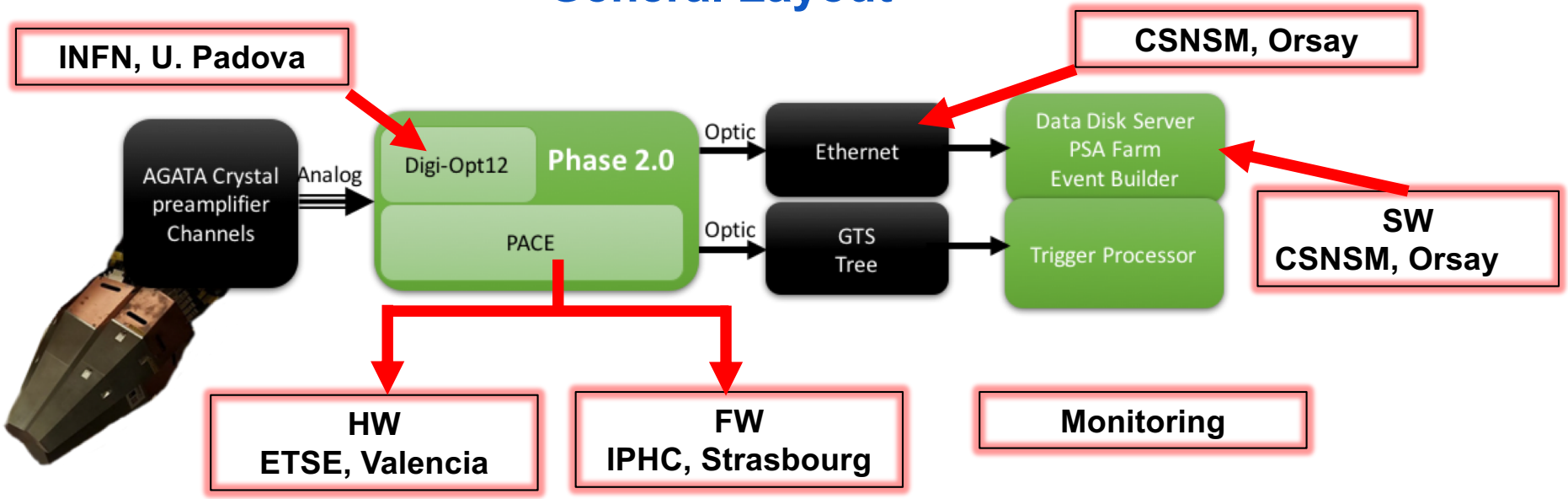
- **Modularity** to allow for the use of new technologies when available and suitable for the objectives of cost reduction and higher integration.
- **Maintenance** of the system **by external companies highly recommended** to insure it through the life of the experiment independently of man power fluctuations in the collaboration.
- **Possibility to have a portable version** to install them in Scanning area, Acceptance Test labs, Host labs for detector maintenance labs so that results can be compared using the same instrumentation between experimental area and labs.
- **Built-in self tests and built in embedded software** so that the system can work **without network access to servers and complicated infrastructure**.

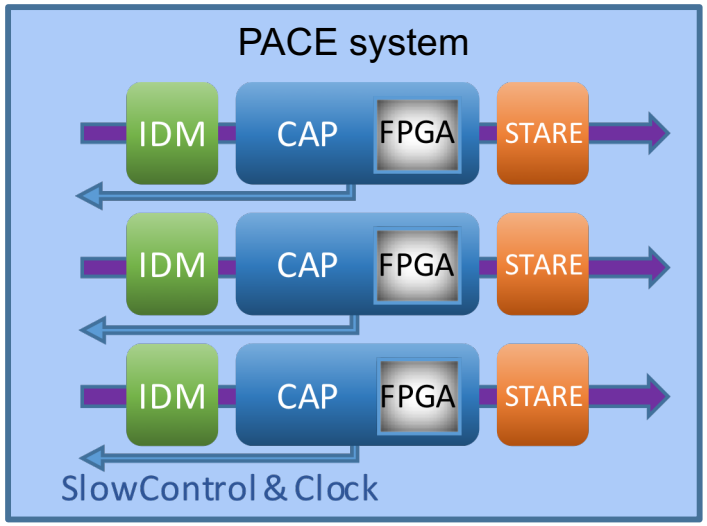
Version evolution

- **2.0:** new architecture with same functionalities as AdvPh1.
- **2.1:** new functionalities to the system
- **2.2:** R&D on the improvement of ADC quality, new trigger/sync systems, Digital Pre-amplifier, …

On going Technical Proposal

General Layout





PACE: Processing and Control over Ethernet
IDM: Input Data Mezzanine
Aggregates data to reduce the number of connections from DigiOpt12 to CAP
CAP: Control and Processing
Integrates the Control Card and GGP functionalities
STARE: Serial Transfer Acquisition Readout over Ethernet
Possible 10 Gb/s Ethernet connection mezzanine. Otherwise integrated in CAP.
GTSO: GTS Output
GTS leaf mezzanine

On going Technical Proposal

Documentation

- **All the work** should be **well documented** and available for future needs
- All this information, including user manuals, repairing manuals, technical descriptions, CAD files, VHDL codes, software, should be **placed in a computer space publicly accessible to all members of the collaboration**

Management

- General Coordination (temporally): A. Gadea (IFIC, Valencia)
- Hardware Coordination: V. González (TeDRA-ETSE, Valencia)
- Firmware Coordination: L. Charles (IPHC, Strasbourg)
- Software Coordination: E. Legay (CSNSM, Orsay)

Chronogram

- **Hardware/Firmware**
  - Proof of concept v2.0 by 1Q 2019
  - V2.1 by 2Q 2019

Thank you for your attention