

## Résultats des tests du Circuit Conf Column (C3) et du prototype RD53A

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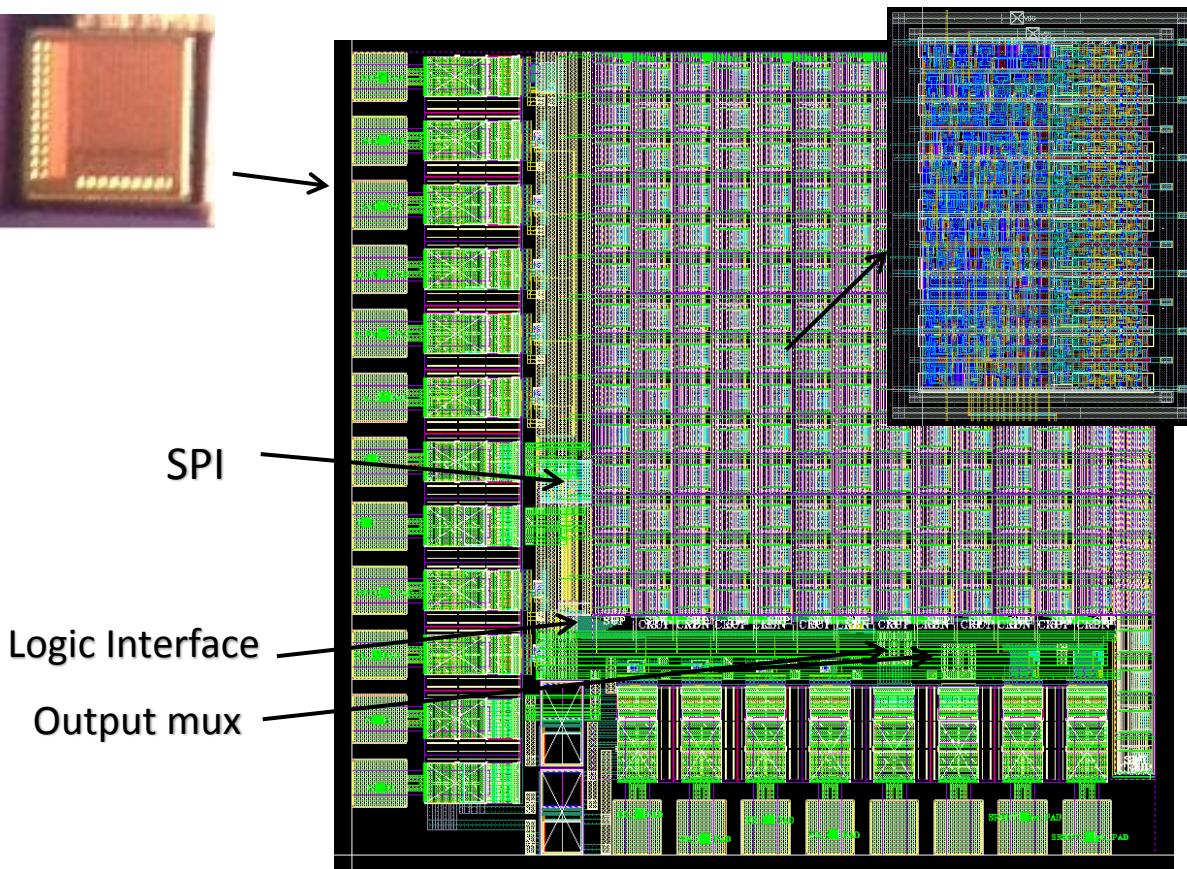
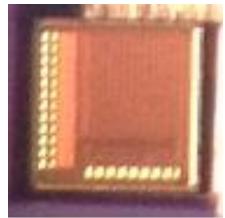
Kostiantyn Sakhatskyi, Vasyl Drozd, Thibault Lédjam (InternShip at LAL)  
RD53a With CERN/IN2P3 collaboration.

# Introduction

- **C3 (configuration Column Chip)**
  - **C3 DAQ**
  - **Software d'acquisition**
  - **Tests en radiation**
- **RD53a**
  - **Système YARR (CERN)**
  - **Système BDAQ53 (BONN)**
  - **Tests des Ring-Oscillator**

# C3 (Configuration Column Chip)

C3



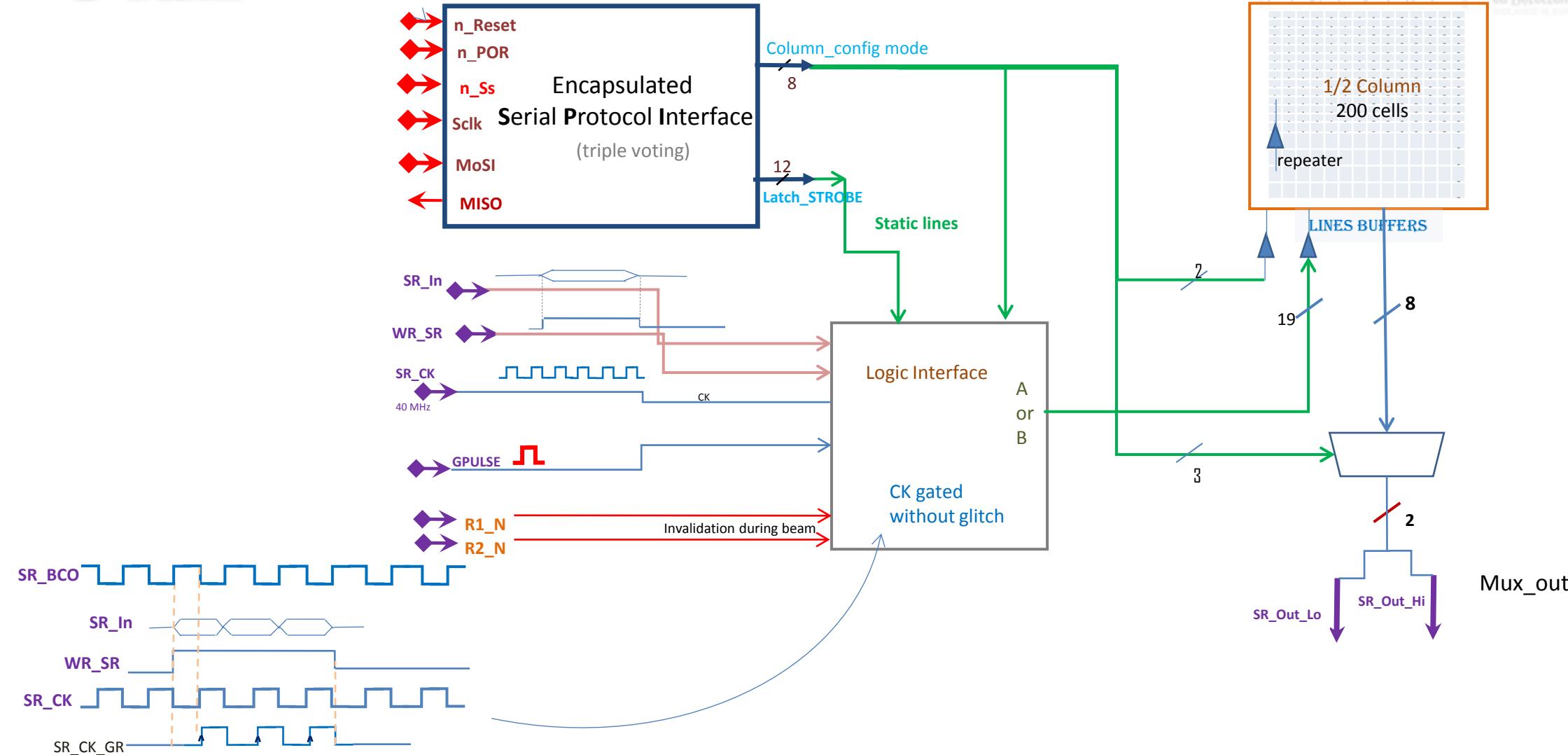
Premier Circuit numeric designé en TSMC 65nm au Lal

C3 = 200 cells-”pixels”  
Cell = 12 radhard latches  
Latch = stores 1 or 0

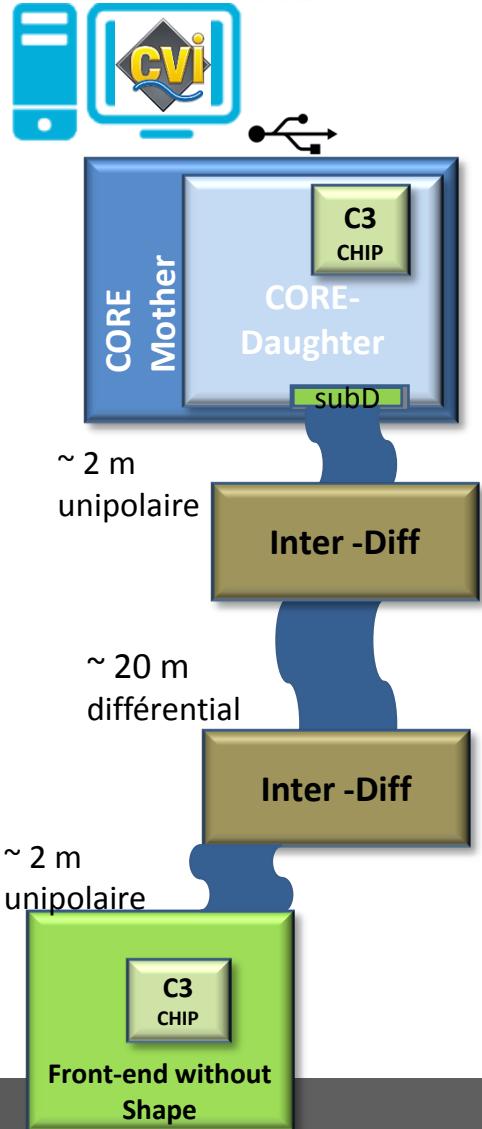
Cells with latches: normal ■ ; enclosed ■  
Enclosed latches have additional guard rings

13	14	41	42	69	70	97	98	125	126	153	154	181	182
12	15	40	43	68	71	96	99	124	127	152	155	180	183
11	16	39	44	67	72	95	100	123	128	151	156	179	184
10	17	38	45	66	73	94	101	122	129	150	157	178	185
9	18	37	46	65	74	93	102	121	130	149	158	177	186
8	19	36	47	64	75	92	103	120	131	148	159	176	187
7	20	35	48	63	76	91	104	119	132	147	160	175	188
6	21	34	49	62	77	90	105	118	133	146	161	174	189
5	22	33	50	61	78	89	106	117	134	145	162	173	190
4	23	32	51	60	79	88	107	116	135	144	163	172	191
3	24	31	52	59	80	87	108	115	136	143	164	171	192
2	25	30	53	58	81	86	109	114	137	142	165	170	193
1	26	29	54	57	82	85	110	113	138	141	166	169	194
<b>0</b>	27	<b>28</b>	55	<b>56</b>	83	<b>84</b>	111	<b>112</b>	139	<b>140</b>	167	<b>168</b>	195
													196
													197
													198
													<b>199</b>

# Block diagram Conf Column Chip & I/O



# C3 DAQ



Ce système d'acquisition est basé sur une carte mère développé au LAL et comprends:

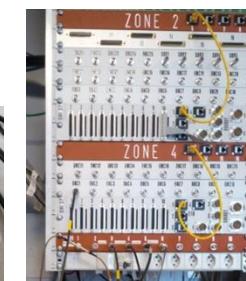
- le contrôle & lecture des données **USB/Ethernet/ Optical fiber**
- la configuration du SPI écriture et lecture des données.
- des Librairies disponibles en C.(LAL-ML protocol).

Ce développement du LAL est utilisé dans diverses expériences.

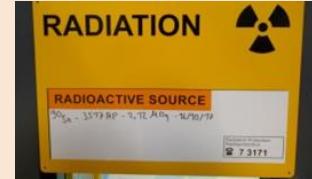
CORE MOTHER (D.BRETON)



CORE DAUGHTER



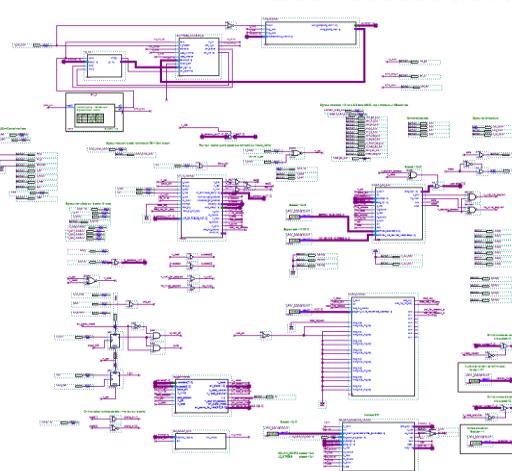
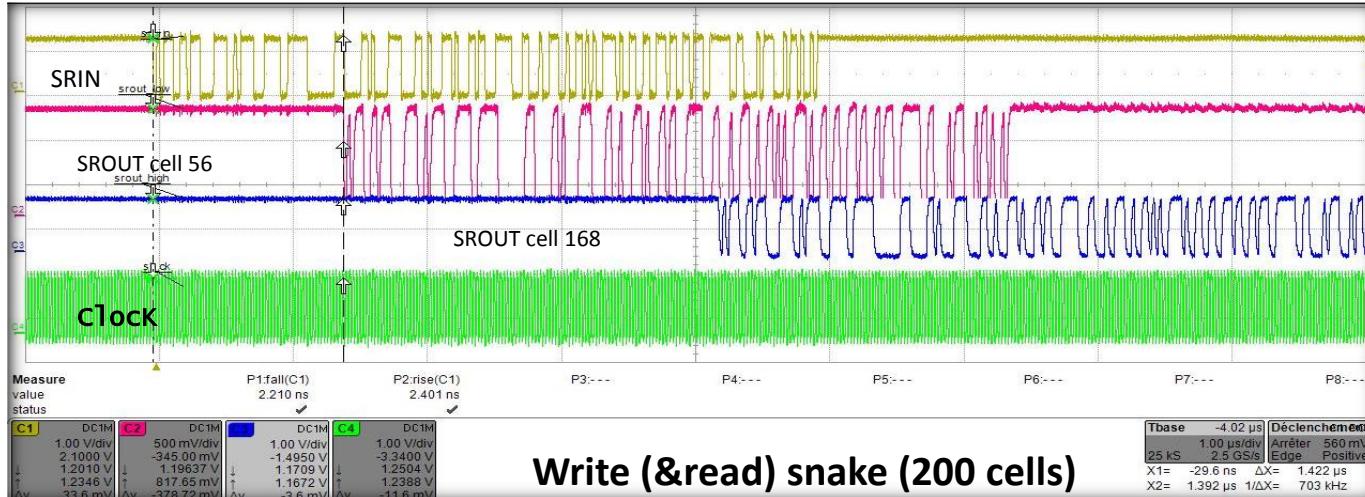
Patch Panel



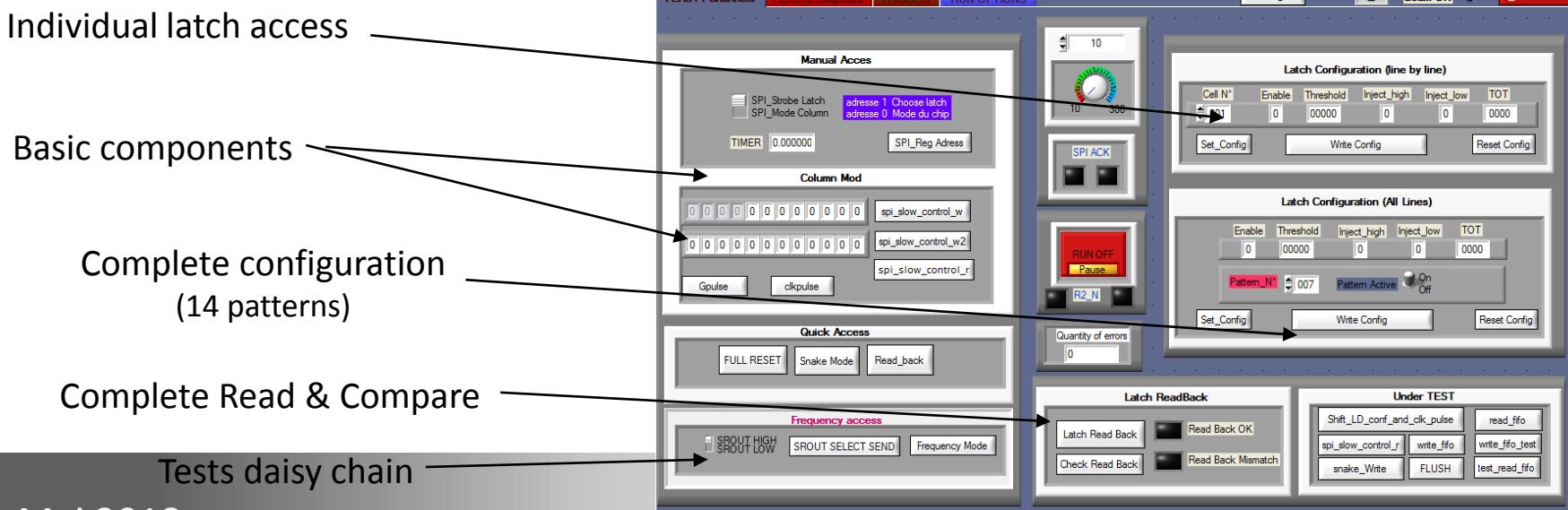
Inter-Diff (C.Sylvia)



# C3 Software & firmware



Firmware Quartus  
(Verilog & VHDL)



Software  
(Labwindows CVI)

## Test en radiation au CERN

C3 a été irradié au Proton Synchrotron du CERN  
IRRAD 13 zone 2

Proton energy: 24 GeV

Fluence:  $9.84 \times 10^{15} \pm 6.9 \times 10^{14}$   $\frac{p}{cm^2}$

One spill fluence:  $1.17 \times 10^{11} \frac{p}{cm^2}$

Beam size: 5 mm x 5 mm

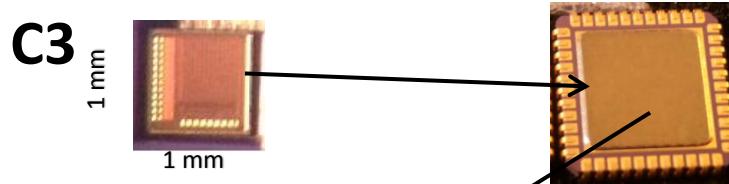
Irradiation time: 8 - 22 November 2017

8 -17 November - with software tests

17-22 November – *after all* software tests

TSMC 65nm  
**C3**  
1 mm  
1 mm

JLCC44 encapsulated



## Chip configuration cycle

Write - 1<sup>st</sup> Read - 2<sup>nd</sup> Read

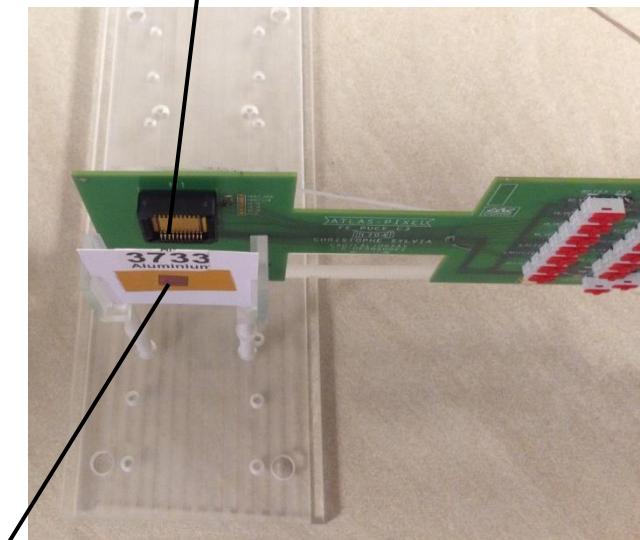
Write some data (1 or 0)  
in each C3 latch

Delay few seconds after write,  
readback from each C3 latch and  
compare with write configuration,  
errors from Single Event Upset

Instantly readback from  
each C3 latch and compare  
with write configuration,  
errors from Integrated Dose influence



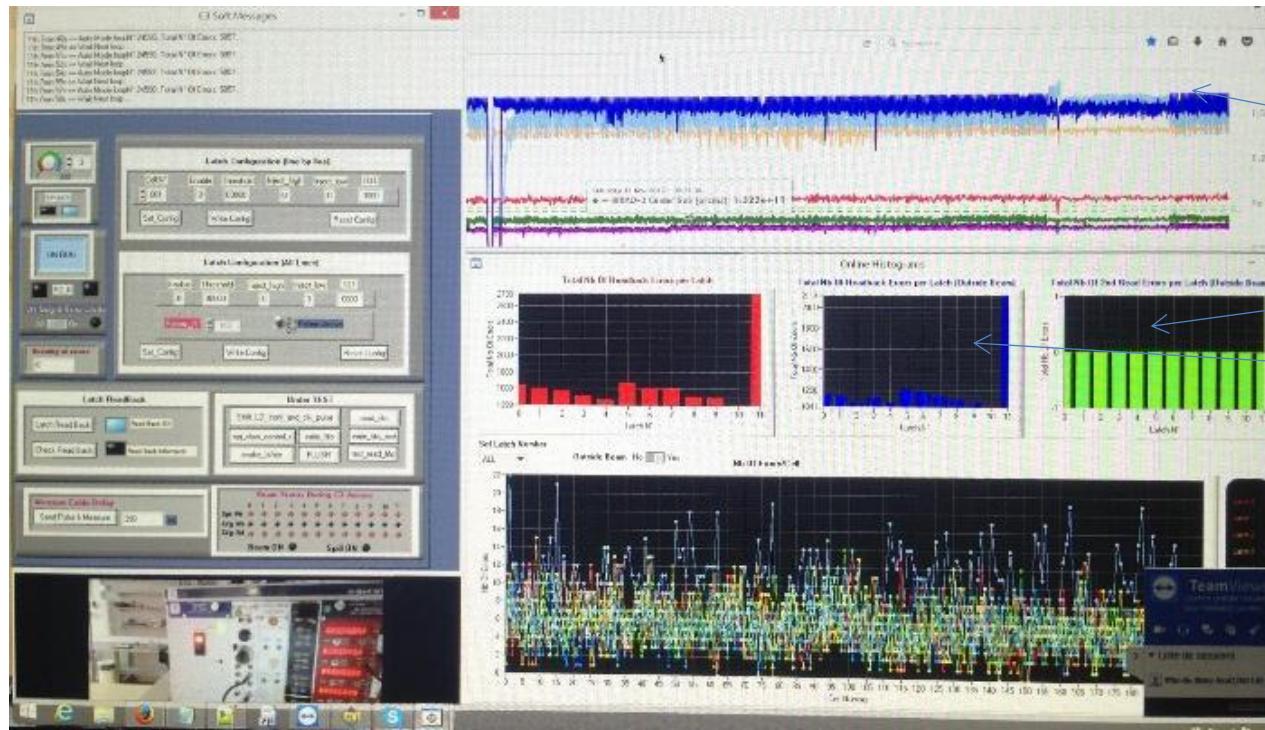
C3  
(Errors count and time)



Dosimeter  
(Integrated dose)

Another CERN dosimeter – Spill counter  
(Fluence count and time)

# Test en radiation au CERN



Flux  $3e^8$  protons/cm<sup>2</sup>

## Labwindow CVI:

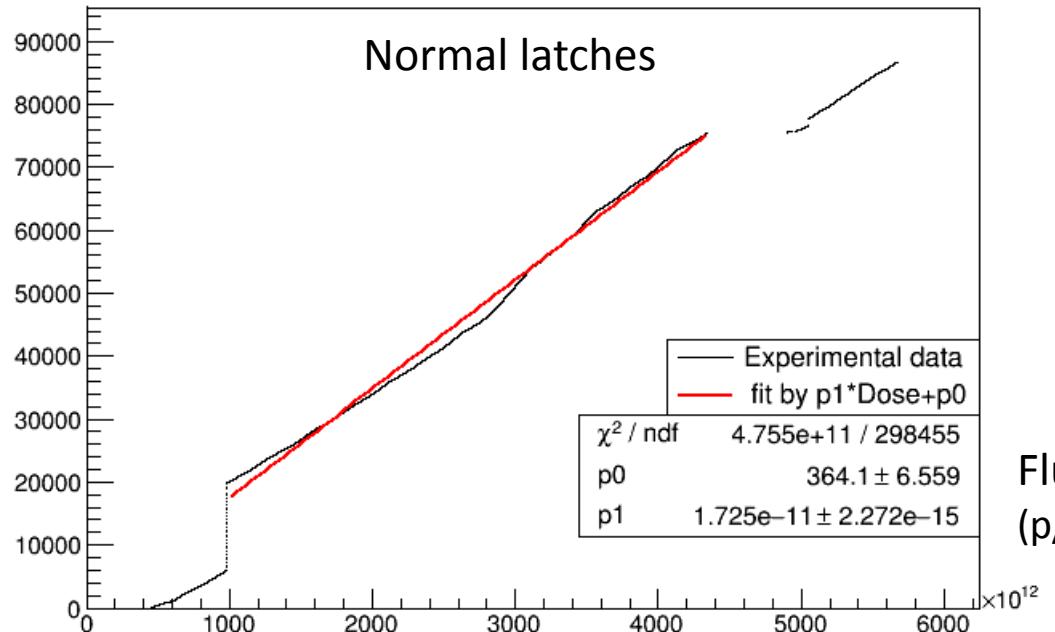
- Control & Readout
- Full Automatic Aquisition
- Latch error monitoring
- Radiation Monitoring CERN
- Post Analysis on ROOT
- Spill counter (start,end,spill on)

Erreurs RadHard latches :  
*Dose intégrée 1 ere lecture*  
*Single Event Upset 2eme lecture*



Errors

Graph



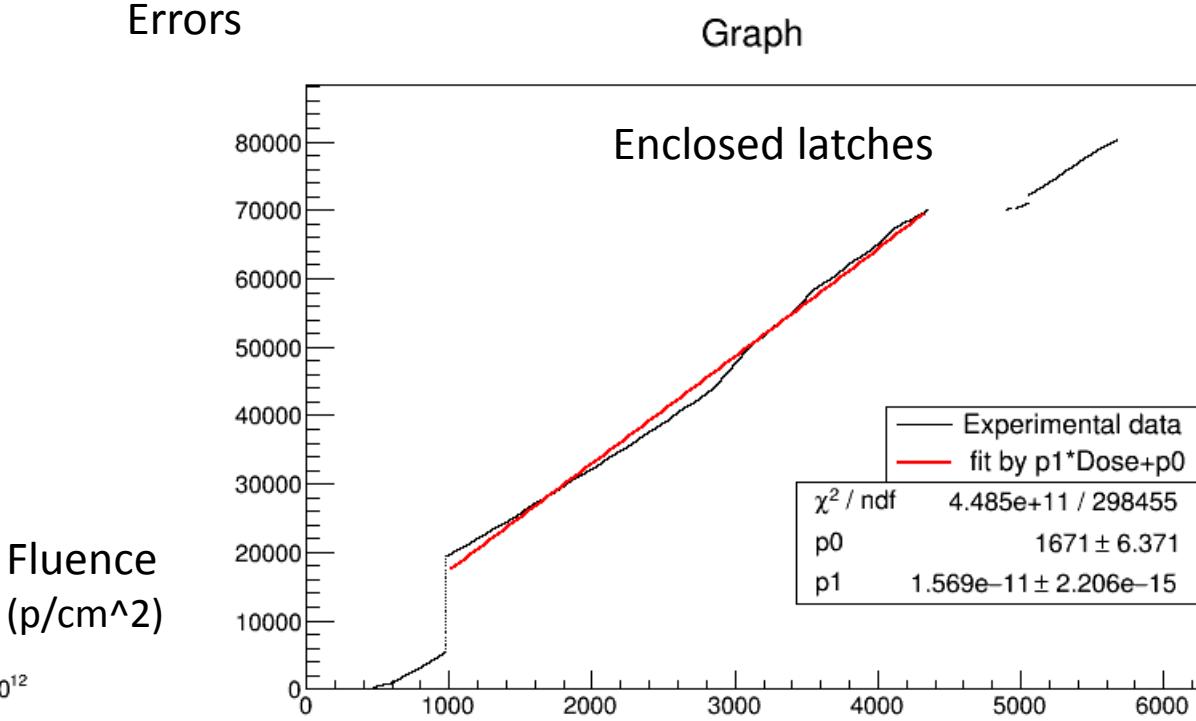
Slopes relation

$$\frac{(p_1)_{normal}}{(p_1)_{enclosed}} = 1.099$$

Errors

Graph

Fluence  
( $p/cm^2$ )



Fluence  
( $p/cm^2$ )

SEU cross-section estimation

$$\frac{p_1}{N_{latches}} \approx \sigma_{SEU}$$

$$\sigma_{normal} \approx 1.598 \times 10^{-14} cm^{-2}$$

$$\sigma_{standart} \approx 2.8 \times 10^{-14} cm^{-2}$$

$$\sigma_{enclosed} \approx 1.452 \times 10^{-14} cm^{-2}$$

$$\sigma_{DICE} \approx 5.6 \times 10^{-15} cm^{-2}$$

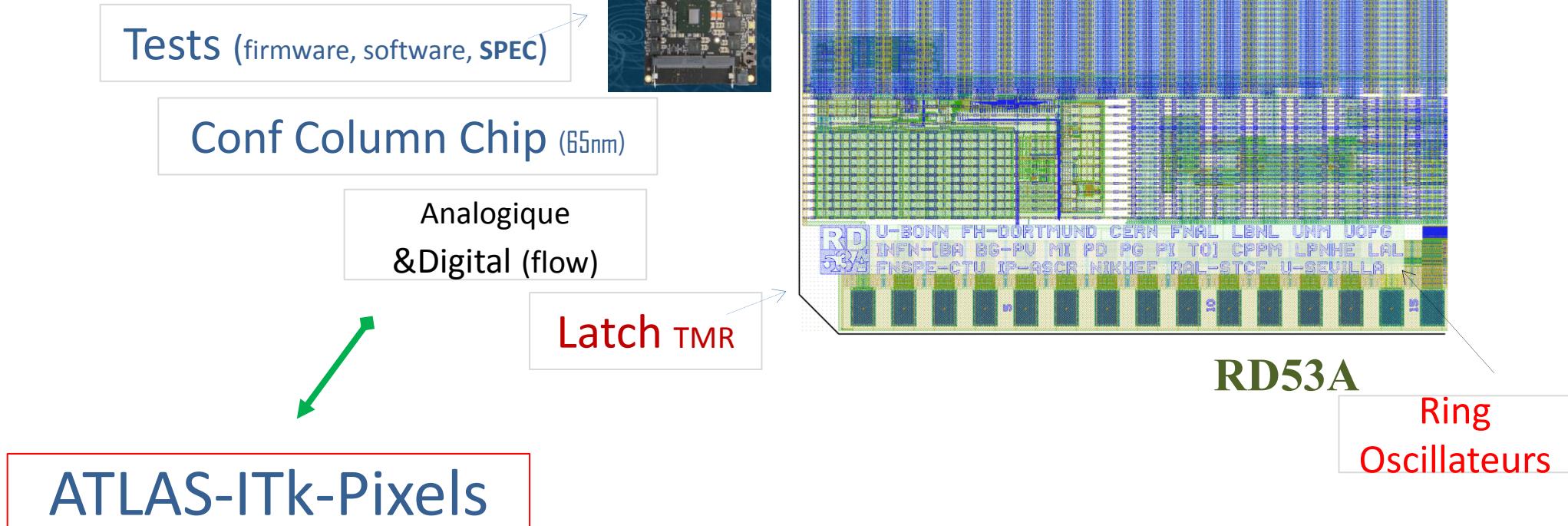
Kostiantyn Sakhatskyi

Jimmy Jeglot

VLSI - Mai 2018

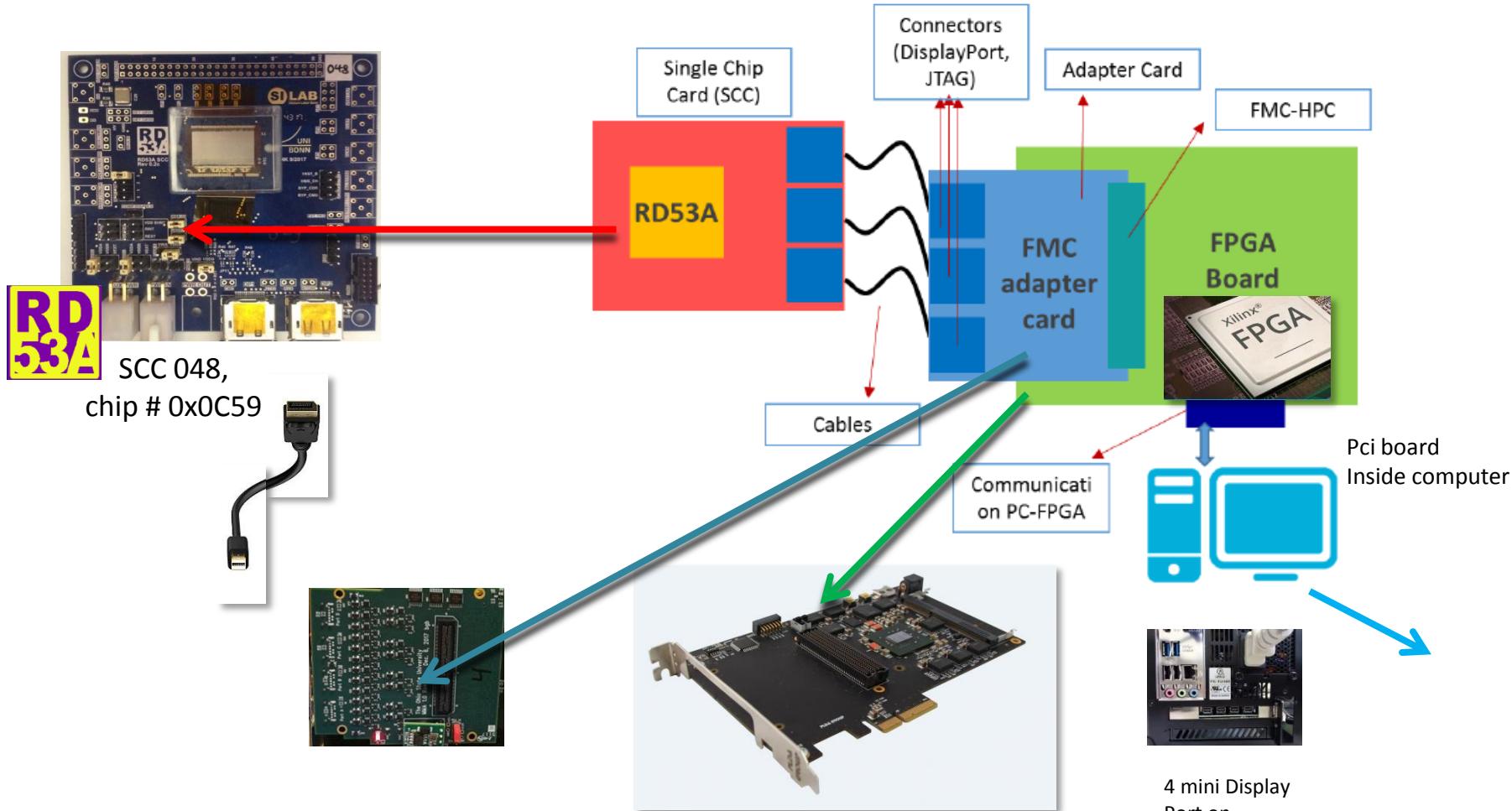
## ATLAS Itk RD53a

Collaboration IN2P3 FRANCE / CERN



- Testing RD53A
- Prototype ITk

# RD53a système YARR



Rd53 testing France : CPPM,LAL,LAPP,LPNHE

- Xpressk7 k325
- Fmc Ohio
- Mini display port
- SCC for RD53A
- CentOS
- Gitlab

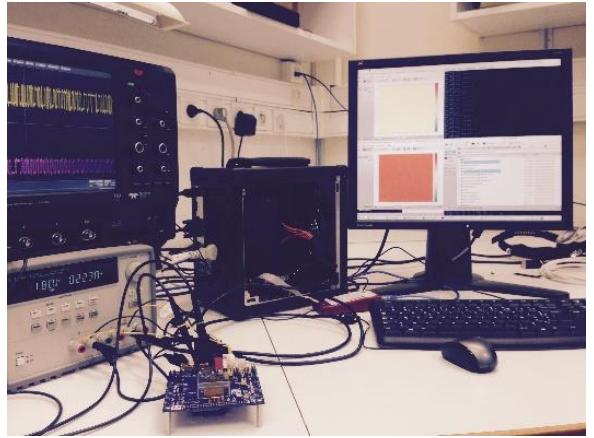


CentOS

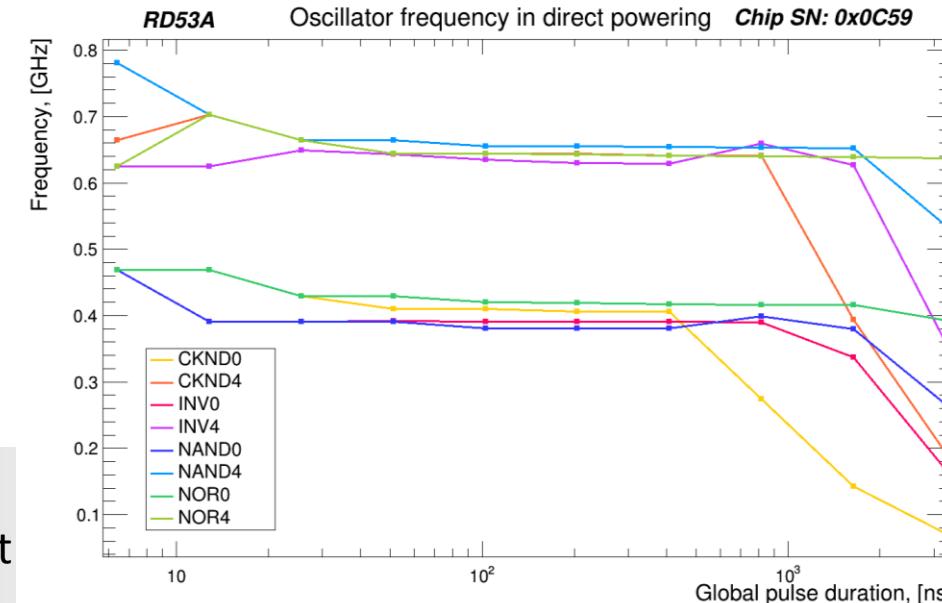
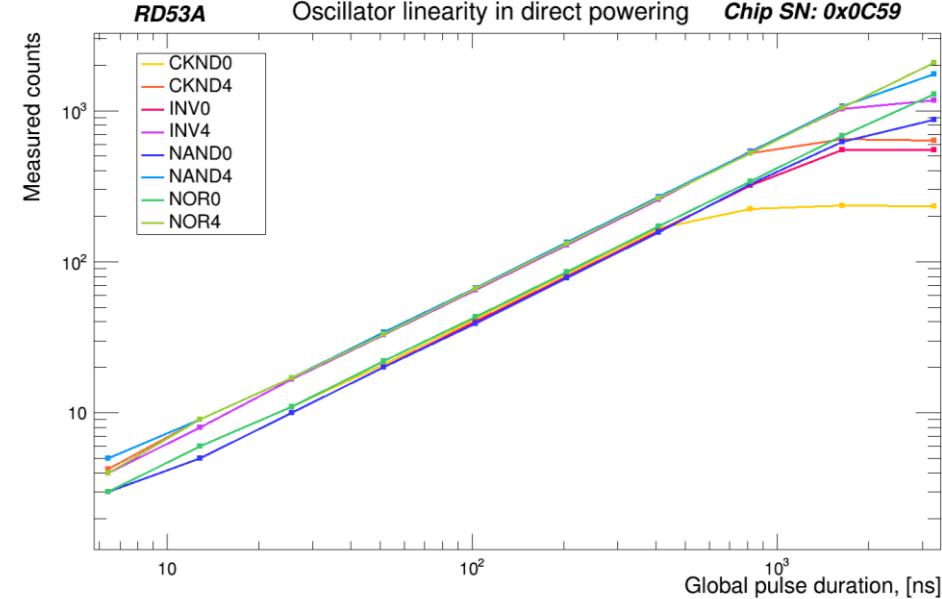
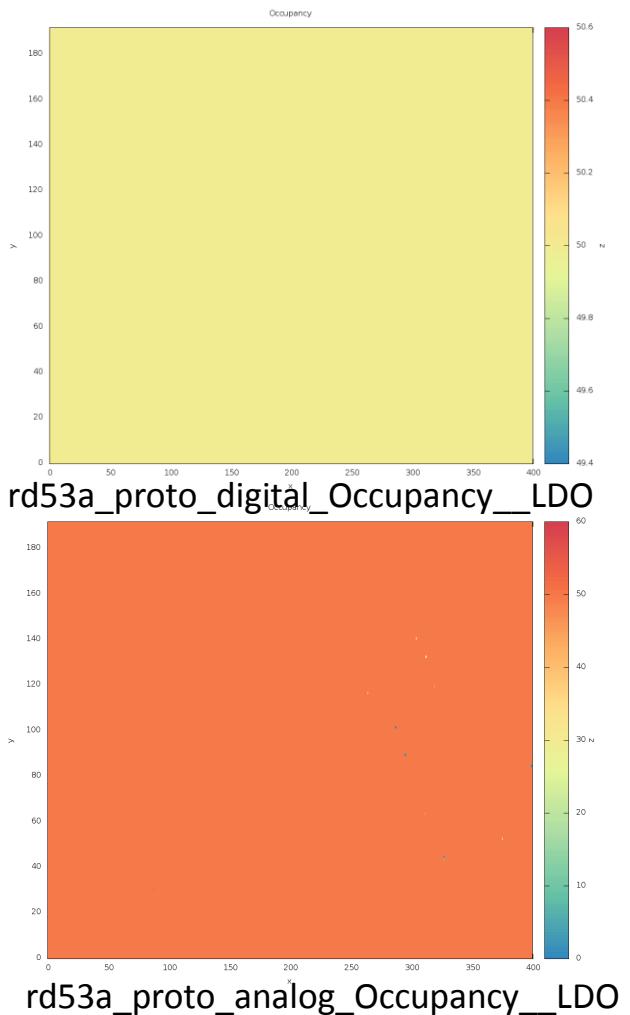


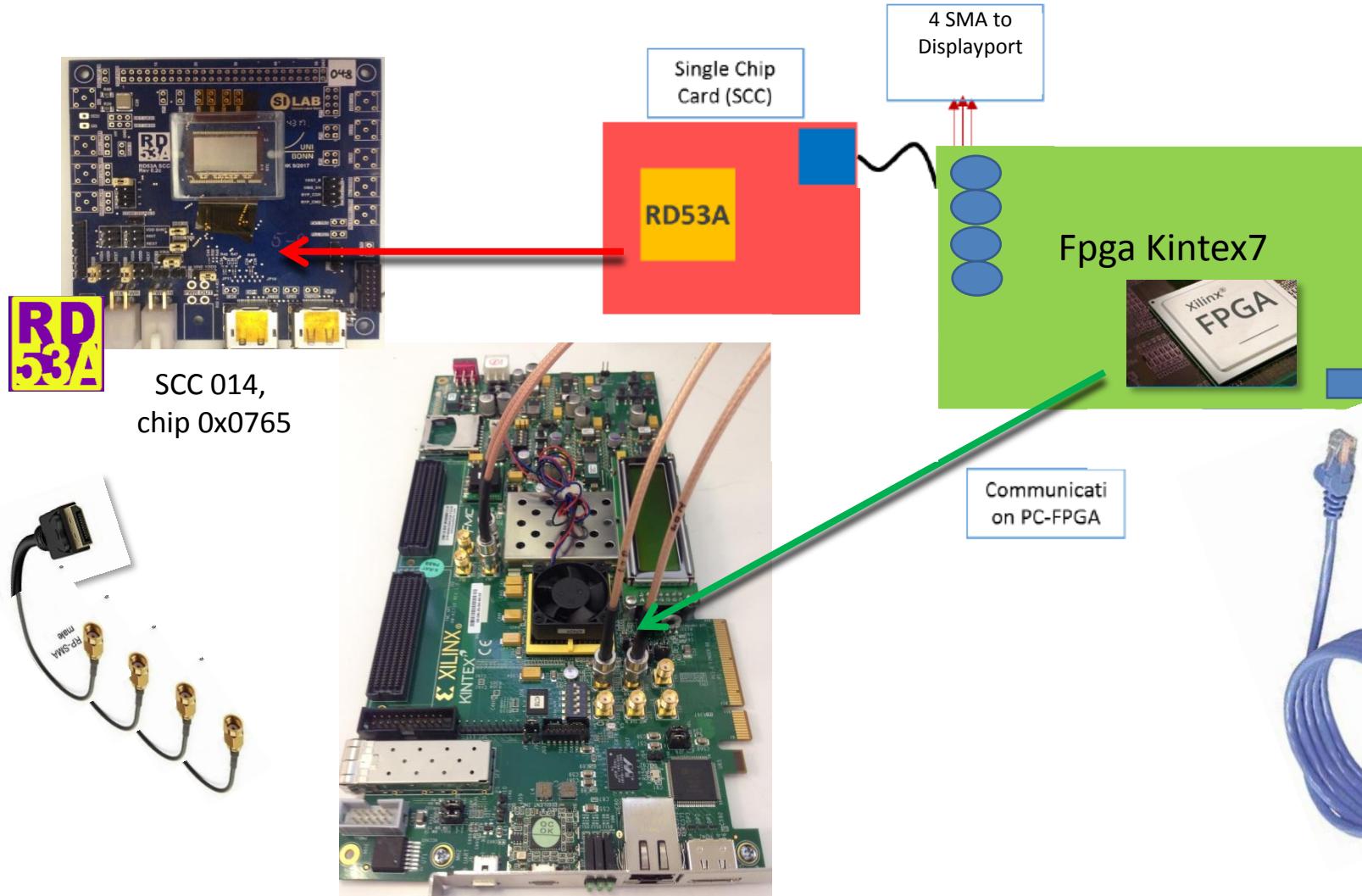
GitLab

# Résultats RO : YARR



ASUS H1 10I-PLUS dedicated computer for RD53 YARR setup



RD53A système BDAQ53 – kc705  
(1,28Gbps )

- KC705
- SMA to display port
- SCC for RD53A
- CentOS
- BDAQ53

<https://gitlab.cern.ch/silab/bdaq53>



No dedicated computer necessary for RD53 bdaq53 setup



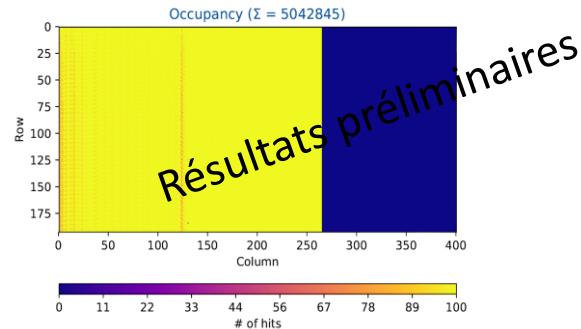
CentOS

GitLab

# Résultats RO : BDAQ 53

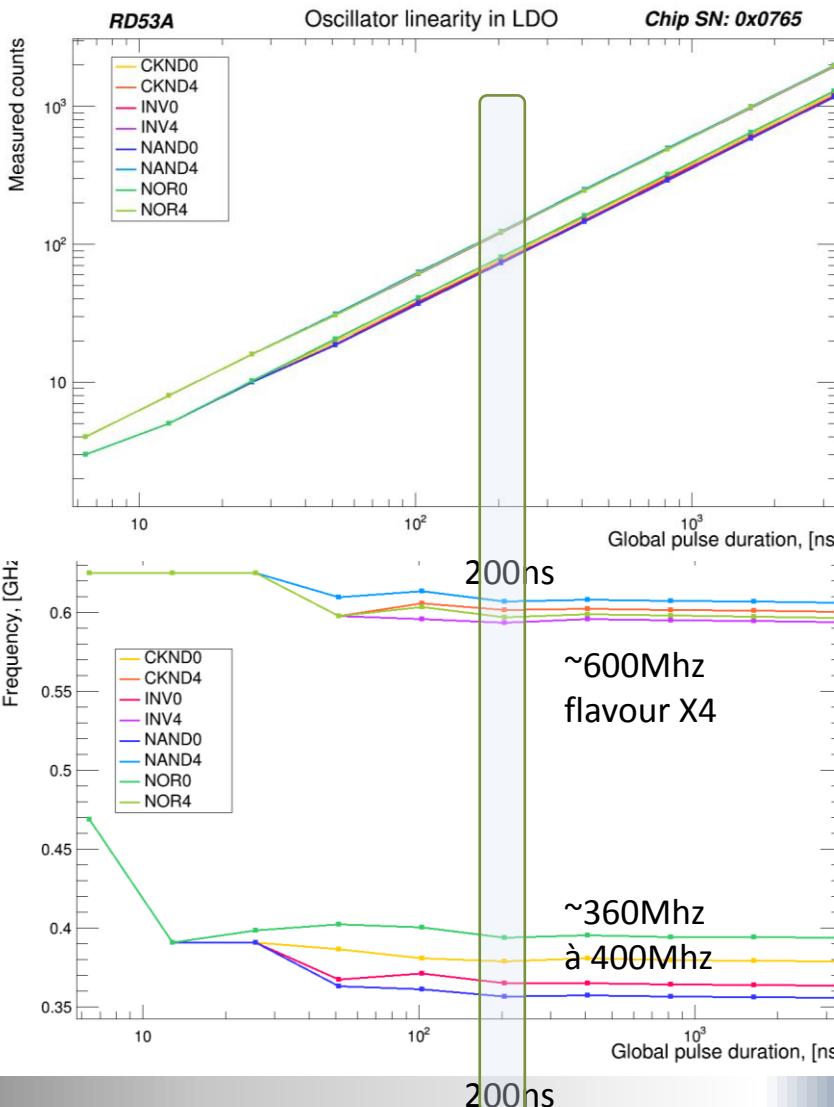


- Activation des ring oscillators;
- Paramétrage et envoi du global pulse par registre:  
(`GLOBAL_PULSE_ROUTE`)  
démarrage des compteurs
- Lecture des registres des ring oscillator:  
(`RING_OSC_0 - RING_OSC_7`)
- Analyse et génération des courbes de linéarité



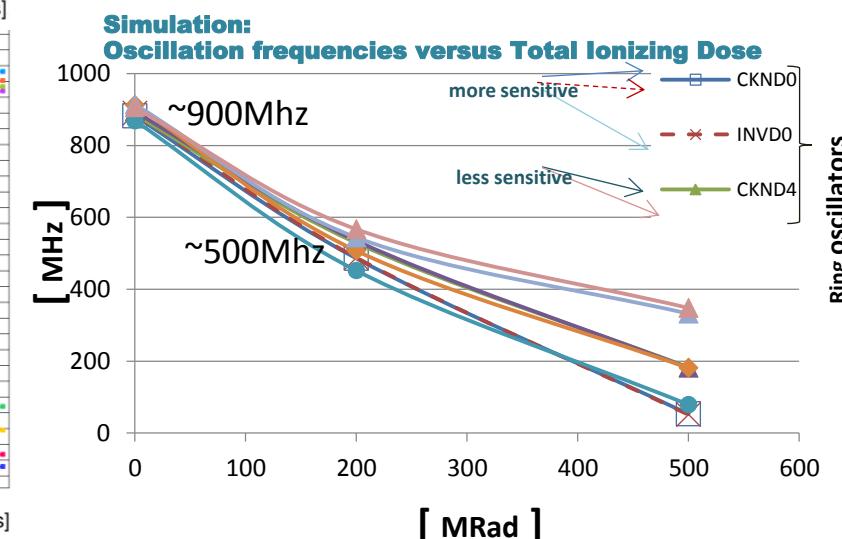
rd53a\_proto\_analog\_Occupancy\_LDO

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Jimmy Jeglot

Enable adress	Ring flavor
110	CKND0
111	CKND4
112	INV0
113	INV4
114	NAND0
115	NAND4
116	NOR0
117	NOR4



# Conclusion

- Le premier prototype C3 est fonctionnel et montre une bonne tenue aux radiations à 250Mrad.
  - Le système distant de pilotage et de lecture (SPI développé au LAL) du circuit C3 en 65nm fonctionne à 10Mhz en zone contrôlée (20 mètres).
- Le ring oscillateur intégré dans le prototype RD53a pour la collaboration ATLAS montre de bons résultats avec le système BDAQ53.  
Quelques points d'interrogation dans la gestion du pulse global dans le système YARR sont à éclaircir.
- Tests en radiation aux rayons X en cours au CERN avec le système BDAQ53.

# Merci à toutes et tous !!!!

Des question ??

PIX\_DIGI\_RD53  
(65nm)

S1	S0	SR_D_A
0	0	SRIN_A
0	1	1
1	0	0
1	1	RdBackOut

**Configurator**

$$V0 \text{ (C3) } 19 \times 18 = 342 \mu\text{m}^2$$

**RTL estimation:**

- v1 = 269um<sup>2</sup> (without clear)
- v2 = 231 um<sup>2</sup> (**only 1 Dff**)
- v3 = **224 um<sup>2</sup>** (without S1)

nets  
121um<sup>2</sup>  
30 cells  
224um<sup>2</sup>

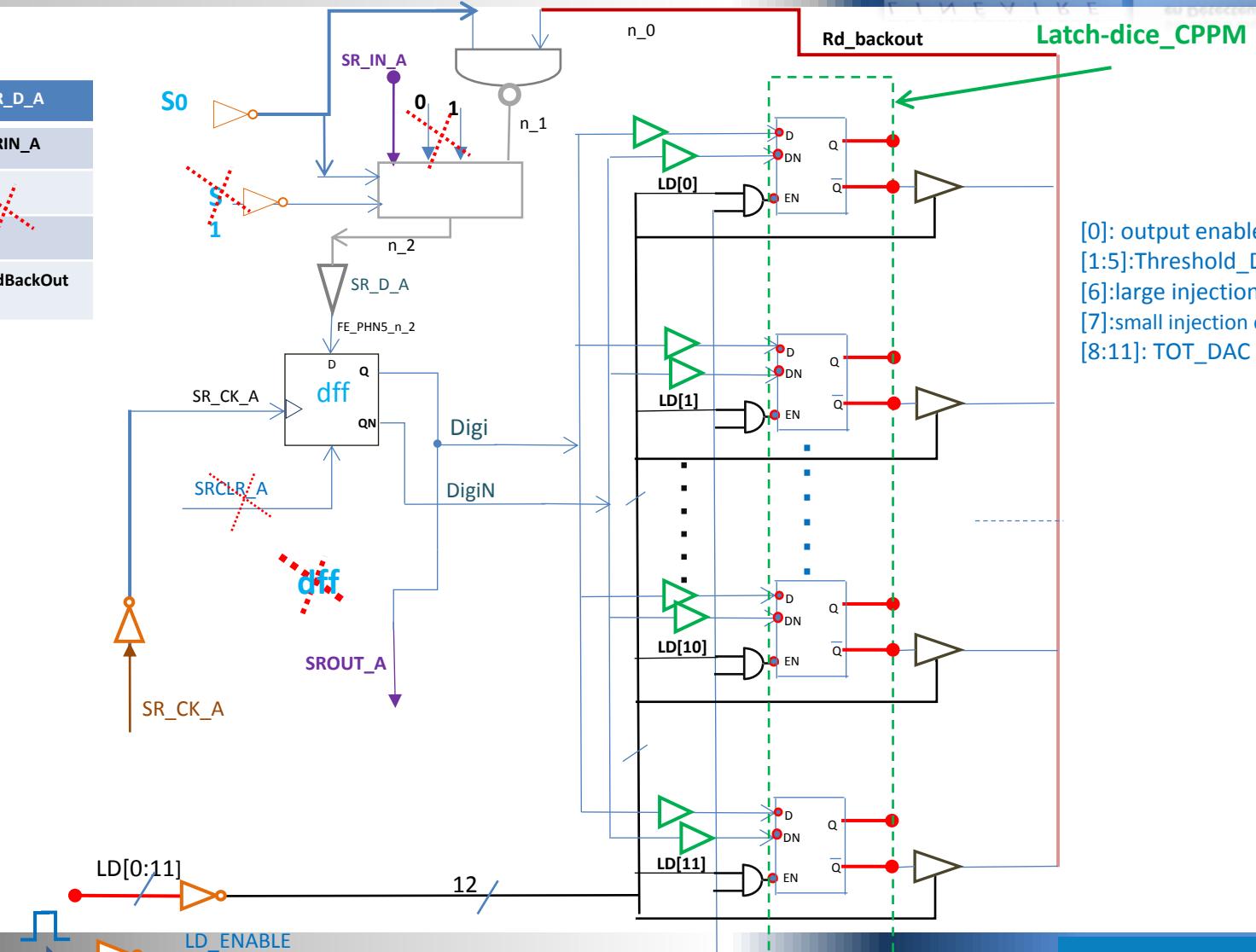
Configurator (V3) (Encounter)

$$8,3 \times 21.93 = 182,02 \mu\text{m}^2 (*)$$



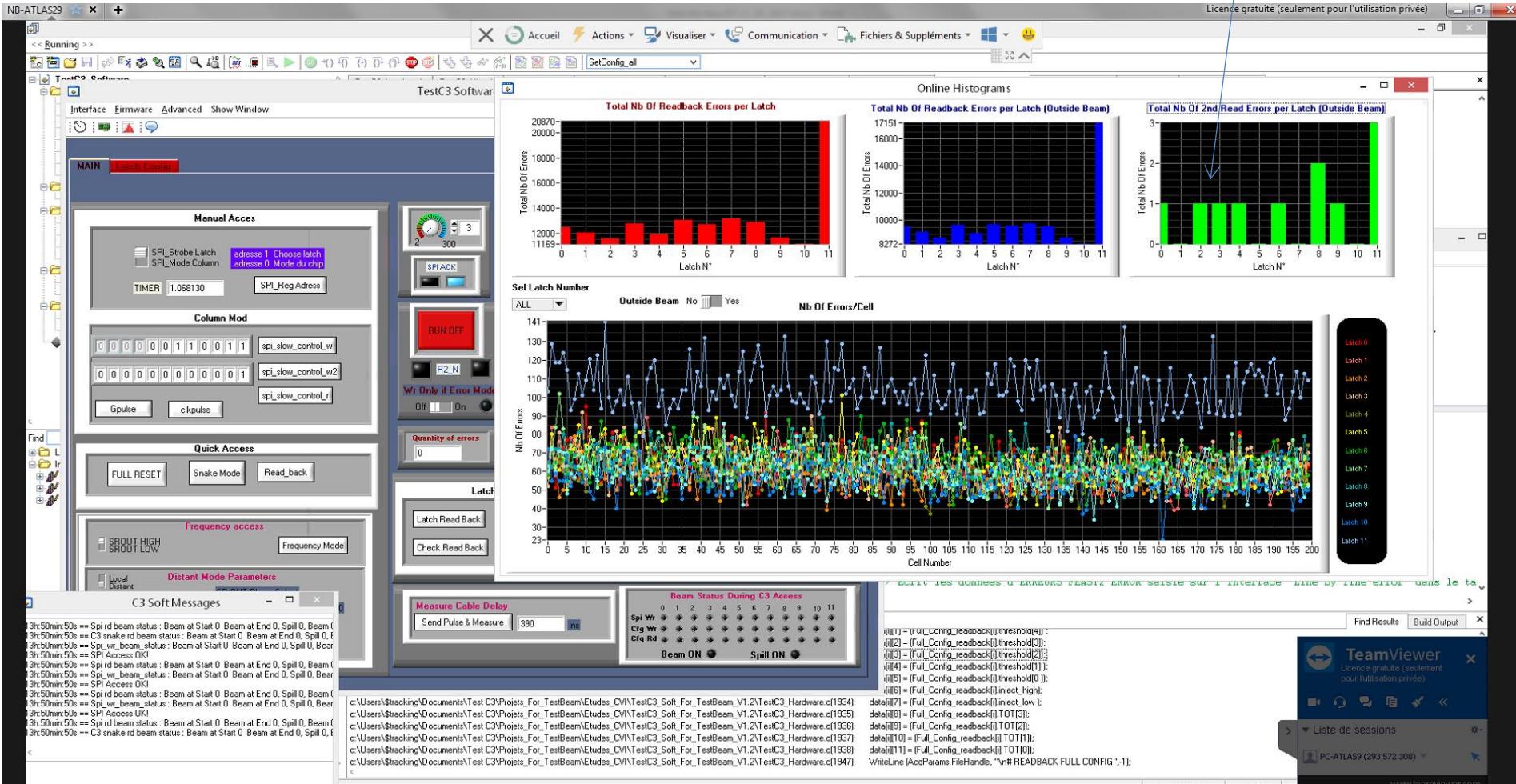
To reduce line capacitance

(From GPLUSE)

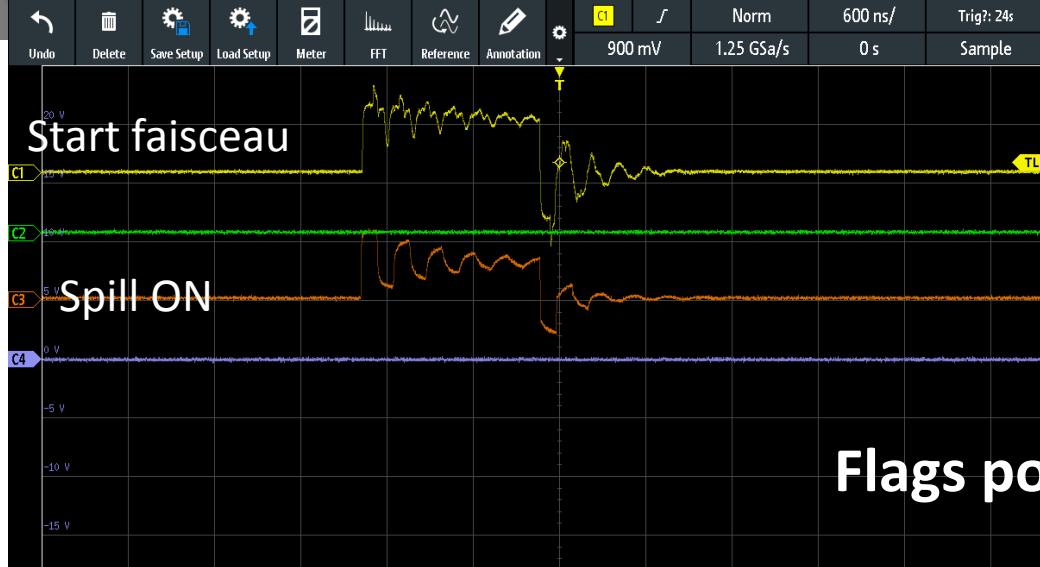


EN  
= 1 active  
= 0 locked

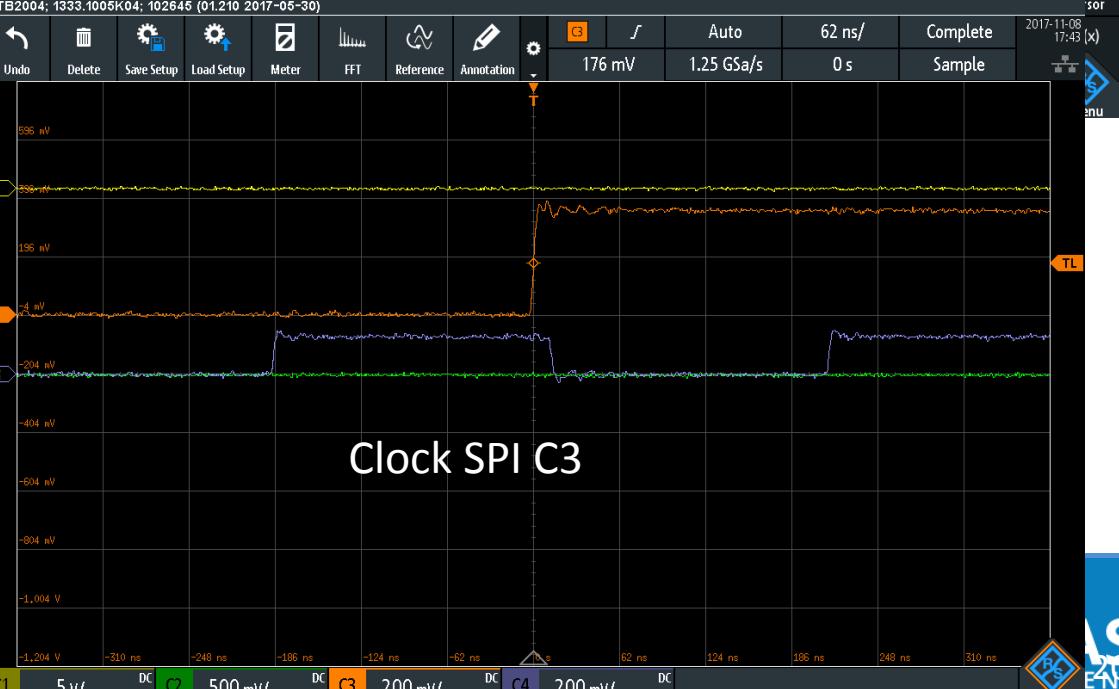
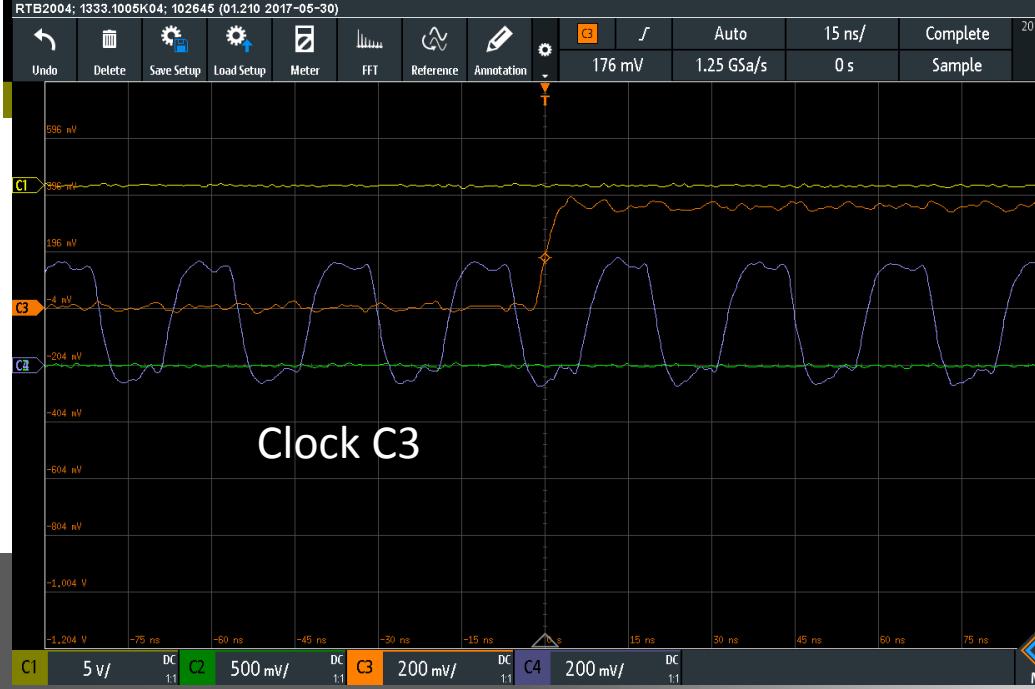
## Control distant du LAL



Quelques erreurs en dose intégrée



## Flags pour les datas au PS du CERN



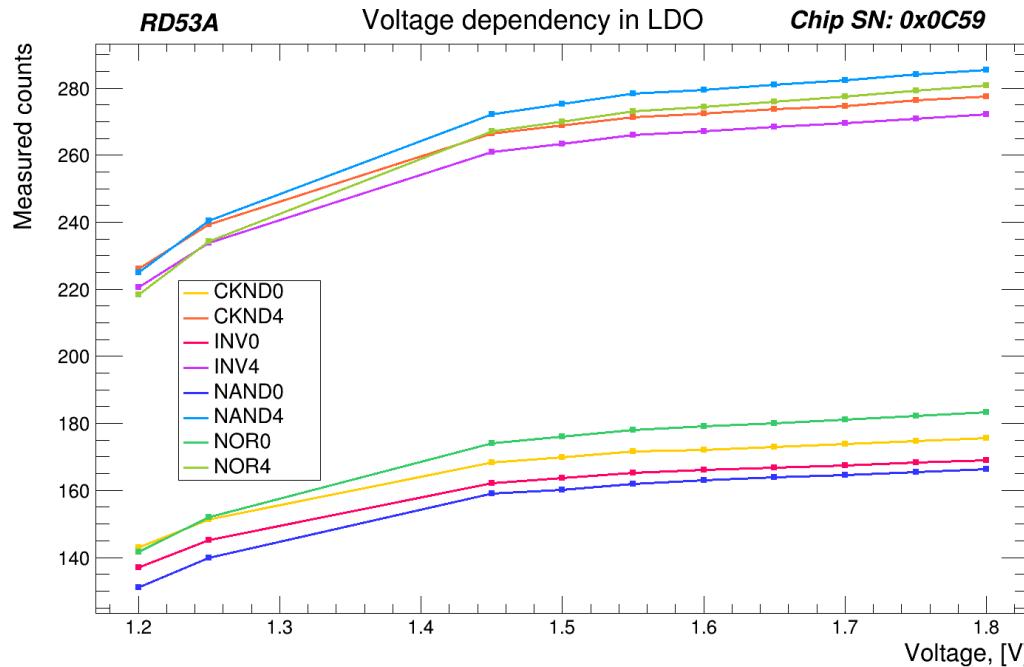
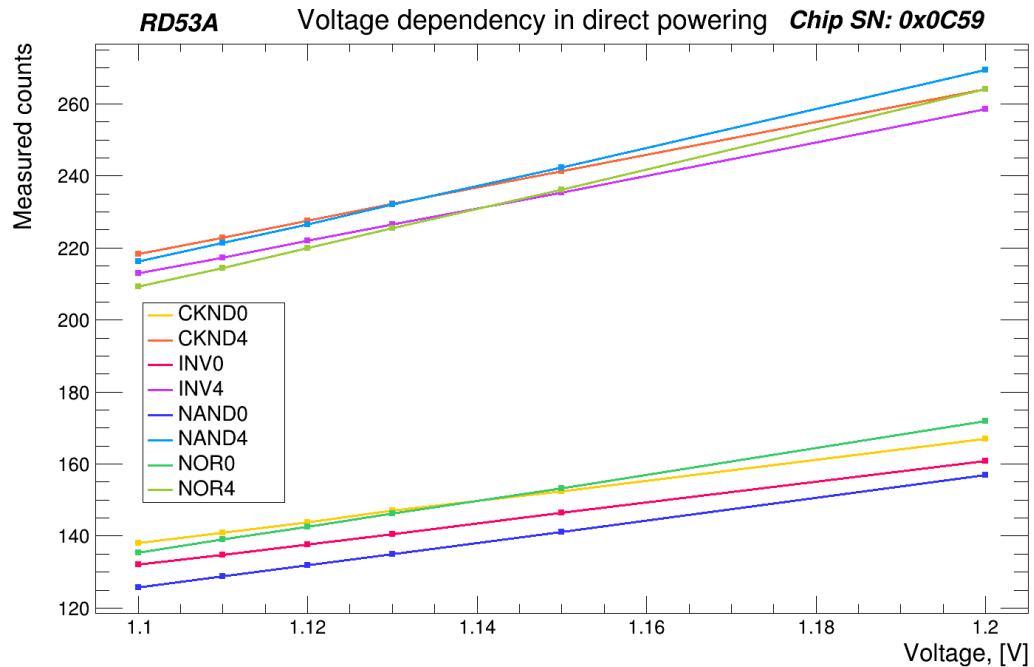
# Rd53a Simulation

tcbn65lp library

Number of cells	Cells	.LIB TT_RFRES_SA: Typical model				.LIB SS_RFRES_SA: Slow corner model		
		$T_{osc}$ [nsec]	$f_{osc}$ [MHz]	Start/stop_N total Max width [μsec]	$T_{osc}$ [nsec]	$f_{osc}$ [MHz]	Start/stop_N total Max width [μsec]	
55	CKND0	<b>1.13</b>	887	4.7	<b>1.45</b>	690	5.9	
51	CKND4	<b>1.13</b>	889	4.6	<b>1.40</b>	714	5.7	
55	INV0D0	<b>1.12</b>	895	4.6	<b>1.42</b>	704	5.8	
51	INV0D4	<b>1.12</b>	897	4.6	<b>1.38</b>	724	5.7	
19	NAND4D0	<b>1.15</b>	869	4.7	<b>1.55</b>	646	6.3	
19	NAND4D4	<b>1.09</b>	914	4.5	<b>1.38</b>	726	4.6	
19	NOR4D0	<b>1.10</b>	912	4.5	<b>1.44</b>	695	5.9	
19	NOR4D4	<b>1.10</b>	906	4.5	<b>1.39</b>	719	5.7	

Cadence Spectre simulator

## ATLAS Itk RD53 Testing



<https://gitlab.cern.ch/RD53-Testing/RD53A/issues/21>